

One-Way or Two-Way Audio Communications using the CC1110 or CC2510 and the TLV320AIC26 Codec

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Keywords

- CC1110
- CC2510
- TLV320AIC26
- Codec
- Two-Way Audio
- One-Way Audio
- Frequency Hopping
- Wireless Microphone

1 Introduction

This application note describes a versatile design that implements a one-way or two-way audio communications link between a 'Master' and a 'Slave', based on the Texas Instruments CC1110 or CC2510 System-on-Chip Low Power RF Transceiver ([1] and [2]) and the TLV320AIC26 Codec [5]. Full 16 bit ADC resolution is provided. Optionally, u-Law compression (to 8 bits) and expansion using a hardware implemented algorithm can be used.

The Codec EVM card is designed to accept a standard CC1110 EM card [4] or CC2510 EM card [3]. Alternate transceiver cards include a CC1110 and a LNA (Low Noise Amplifier) combination ("CC1110 LNA for Codec"), a CC1110 and a PA (Power Amplifier) combination ("CC1110

PA Codec"), and a CC2510 plus CC2590 'range extender' card (CC2510_CC2590 EM).

The Codec EVM demonstration card described in this note consists of a TLV320AIC26 Codec, a TPA6011A4 audio amplifier [6], connectors for an external CC1110 or CC2510 EM, a microphone, and an internal speaker. Schematic diagrams, PC layout ('Gerber') files, and example software are available from Texas Instruments. While this document describes the software for a 'Two Way' link operating at an audio sample rate of 8 kHz, software supporting many other one and two way options is available.

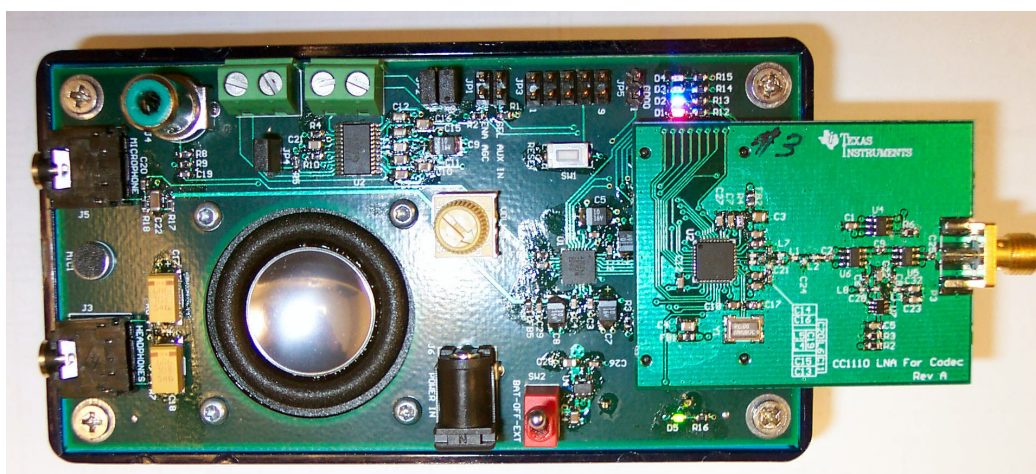


Figure 1. Two-Way Audio Transceiver with Codec (Rev B) shown with CC1110 LNA for Codec (Rev A)

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2 Abbreviations

ADC	Analog to Digital Converter	LED	Light Emitting Diode
AGC	Automatic Gain Control	LRCLK	Left\Right Clock
AUX	Auxiliary (Input)	MAC	Message Authentication Code
BCLK	Bit Clock	MCLK	Master Clock
CD	Compact Disk	MHz	Megahertz
Codec	Compressor-decompressor	MICIN	Microphone Input
CRC	Cyclic Redundancy Check	MPU	Micro Processor Unit
DAC	Digital to Analog Converter	ms	Milliseconds
dB	Decibel	mW	MilliWatt
dBm	Decibel (referenced to one) milliwatt	PGA	Programmable Gain Amplifier
DC	Direct Current	PLL	Phase Locked Loop
DMA	Direct Memory Access	PSRR	Power Supply Rejection Ratio
EB	Evaluation Board	RF	Radio Frequency
EM	Evaluation Module	RX	Receiver
EVM	Evaluation Module	SFD	SYNC Field Detected
FCC	Federal Communications Commission	SoC	Silicon on Chip
GFSK	Gaussian Frequency Shift Keying	SPI	Serial Peripheral Interface Bus
I2S	Inter-IC Sound Bus	TX	Transmitter
kbps	kilobits per second	µs	Microseconds

3 Brief Description – Two Way Link at an 8 KHz Sample Rate

Audio data is sampled at an 8 kHz rate (one 16 bit sample every 125 μ s), compressed to 8 bits using the CC1110s (CC2510s) built in μ -Law compression/expansion hardware, and sent in 'packets' of 54 samples. A 'packet' is sent every $54 \cdot 0.125 = 6.75$ ms. The code loaded into the CC1110 or CC2510 establishes the unit as either a 'Master' or a 'Slave'. The 'Master' unconditionally sends a packet every 6.75 ms, and listens for a response from the 'Slave'. The 'Slave' listens for a packet from the 'Master', and replies with a packet if a packet was received.

The Codec EVM card contains both a microphone and a speaker. Optionally, a headset that contains both a condenser microphone and a headphone, such as the Sennheiser PC131, can be used.

4 Detailed Description

Refer to the block diagram, Figure 5. The TLV320AIC26 Codec is connected to the external CC1110 or CC2510 via two busses; an I2S bus for audio data, and a SPI bus used to load the control registers. ADC samples are sent to and from the TLV320AIC26 over an I2S bus. MCLK has a frequency of 13.000 MHz, and is derived from the CC1110 (CC2510)'s 26.0 MHz crystal using Timer 4. BCLK clocks at 16 bits per word * 2 words * 8 kHz (the sample rate), or 256 kHz. LRCLK is low while the Left Channel data is being sent (received), and high while the Right Channel data is being sent (received). Note that the CC1110 (CC2510) is set up as the I2S bus master, and that mono mode is enabled. In mono mode, the CC1110 (CC2510) repeats the audio sample data in both the left and right channels. Details on how to set up and use the CC1110s (CC2510s) I2S bus are available in [9].

The Codec's control registers are set up over the SPI bus. The CC1110/CC2510 is the SPI bus Master. In this application, the Codec's PLL is set to generate a $f_{s_{ref}}$ frequency of 48 kHz. The ADC and DAC external sample rate is set for 8 kHz, although internal to the Codec the ADC and DAC are sampling at the $f_{s_{ref}}$ frequency (48 kHz). Refer to the TLV320AIC26 data sheet [5] for more details.

An internal condenser microphone is installed on the card, and connects to the Codec's 'MICIN' input. Alternatively, an external condenser microphone (e.g., a headset or a lapel style) may be used by plugging the microphone into the 'Microphone' jack. The RCA jack provides a means to connect a high level signal (e.g., a CD player) to the Codec's 'AUX' input. The AUX input is selected by installing a jumper across the pins 3 and 4 of JP1 ("SEL AUX IN"). When the microphone (either internal or external) is in use, the ADC PGA gain is set to 26 dB. The PGA gain is reduced to 0 dB when the AUX Input is selected. By default, the Codec AGC is disabled; it may be enabled by installing a jumper across the pins 1 and 2 of JP1 ("ENA AGC"). When using the AUX input, disabling the AGC is recommended.

The TPS6011A4 [6] is a class AB audio amplifier that can produce approximately 1 watt per channel into 8 ohm loads. A unique feature of this amplifier is that its gain (volume) is controlled by a DC voltage; this eliminates the need for a conventional 'pot' in the audio path, thereby reducing RF noise 'pickup'. As connected, the headphones are driven by both the left and right amplifiers, while the internal speaker is driven by only the left amplifier. One or two external speakers can be connected, using the terminal blocks.

The card may be powered from either the three AAA batteries installed in the back of the card or from an external 5 volt DC power source. A TPS73033 [8] low-noise, high PSRR, RF 200-mA low-dropout linear regulator is used to obtain the 3.3 volts required by the CC1110 (CC2510). In addition, a TPS73018 [7] Low-Dropout linear regulator is used to generate the 1.8 volt logic supply required by the TLV320AIC26 Codec.

In addition to a green 'POWER ON' LED, four LEDs are included on the card. The four LEDs have the following functions:

- Blue: Heartbeat. Flashes twice per second as long as the CC1110 (CC2510) program is running.
- Green: Paired. Lit when the 'Master' and 'Slave' are in communications.
- Red: Lost Packet. No data was received from the Slave (Master) or from the Master (Slave).
- Yellow (Slave only): Searching for Beacon. Waiting to 'hear' the Master's Beacon signal.

5 CC1110 (CC2510) Programming

The CC1110 or CC2510 can be programmed using a SmartRF04EB, either by plugging the EVM card directly into the SmartRF04EB (connectors P1 and P2), or while plugged into the Codec EVM card. In the later case, a short 10 pin cable must be installed between a System-on-Chip Debug Plug-In board (SOC_DEM) installed in the SmartRF04EB and JP100 of the Codec EVM card. See section 9.3 of the CC1110-CC1111DK, CC2510-CC2511DK Users Manual [12] for details. IAR workspaces are available from Texas Instruments for this and many other configurations.

6 Use of the DMA Channels

The CC1110 and CC2510 contain five DMA channels. These provide a means to transfer ADC and DAC sample data to and from the Codec directly into memory, without MPU intervention. The CC1110 and CC2510 also include μ -Law compression and expansion hardware. Sixteen bits ADC samples are received over the I2S bus, compressed to 8 bits, and transferred to memory using DMA channel 4. Similarly, 8 bits DAC samples are taken from memory, expanded to 16 bits and transferred to the Codec over the I2S bus using DMA channel 3. See Figure 2, below.

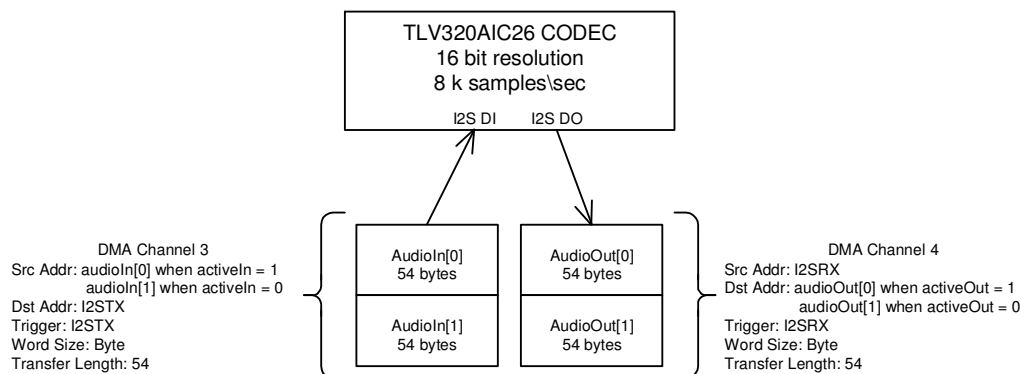


Figure 2. DMA Channel Allocation

Since an audio sample arrives every 125 μ s and a RF data packet is sent every 54 samples, 'double buffering' of the audio data is required. Audio samples are sent from the Codec to the AudioOut buffer. Every 54 samples, the FrameReady flag is set, the active buffer indicator (activeOut) is toggled, and the DMA destination address is set to the 'non active' buffer. The activeOut indicator therefore indicates the currently usable buffer (containing valid data). Similarly, audio samples are sent from the AudioIn buffer to the Codec. Every 54 samples, the active buffer indicator (activeIn) is toggled, and the DMA source address is set to the 'non active' buffer. The activeIn indicator therefore indicates the currently available buffer – samples from the 'non active' buffer are being sent to the Codec.

DMA channel 1 is used to transfer from the receiver to the rxData buffer. DMA channel 2 is used to transfer data from the txData buffer into the transmitter.

7 Detailed Description - Software

Due to the time critical nature of streaming audio, the supporting software code used for this project is application specific; that is, it is not based on any standard protocol.

Figure 6 is a flow chart of the Master's main program loop. Note that the 'AudioFrame Ready' flag is set by the Channel 4 DMA interrupt handler, and is set after 54 audio samples have been received from the Codec (i.e., every 6.75 ms). PLL calibration requires 721 μ s to complete, during which time the radio cannot be used. Use is made of this time by organizing the program such that audio samples from the Codec (Audio Out buffer) are loaded into the TX buffer while the PLL is calibrating. After transmitting a packet, the Master will listen for a packet from the slave. If no packet is received (Timeout Error), the red 'Lost Packet' LED is lit, the 'lost packets' count incremented, and the Audio In buffer is filled with a value that produces zero volts. If more than four consecutive packets have been lost, the Green 'paired' LED is extinguished. If a packet is successfully received, the data is copied into the Audio In buffer and will be transferred into the Codec via DMA channel 3. The red 'lost packet' LED is extinguished and the green 'Paired' LED is lit. If a packet is received but contains a CRC error, the Audio In buffer is filled with a value that produces zero volts.

Figure 7 is a flow chart of the Slave's main program loop. Its timing is based on a 'Frame Timer' (T2). This is a 'count down' timer, which is initialized to a value of 237 tics, corresponding to a period of 7.00 ms, after a packet is received from the Master. Two variations of a 'Receive A Packet' subroutine are used. Subroutine 'ListenforMaster' is used while in 'waiting for beacon' mode, and will return immediately after receiving a packet or after the specified 'timeout' period (27 ms) if no packet is received. Subroutine 'rfReceivepacket' is used in 'paired' mode, and will return after the specified time period (1255 μ s) if a packet is not received. If, after the specified time period a packet is being received (sync word was detected), the subroutine will not return until the entire packet has been received. Note that the Slave will transmit its Codec data only if a packet is received from the Master.

Unlike the Master, the clocking of the Slaves Codec is asynchronous to the RF packet timing. This is because the Slaves RF packet timing is synced to that of the Master. The Master's RF timing is synced to its Codec via the 'AudioFrameReady' flag. This can result in the Slave main program writing to or reading from the 'wrong' audio buffer, because the Master and Slave clocking frequencies (26 MHz) are not precisely matched. Recall that both the audioOut and audiIn samples are 'double buffered', and that the Codec determines which buffer is 'active' (see Section 6). To avoid this problem, the Slaves Codec BCLK (bit clock) frequency is adjusted (increased) should the RF packet arrive in the so called 'danger zone'. Experimentally, the 'danger zone' is determined to be when the Frame Timer tic count ('frametime') is between 128 and 156. Variable 'frametime' contains the 'Frame Timer' tic count when the 'activeIn' index is switched in the Channel 3 DMA interrupt service routine. The BCLK frequency is reset to 256 kHz when variable 'frametime' is between 16 and 95. This is shown in an expansion on the Slave flow chart.

8 Frequency Hopping\FCC Compliance

In the example software, frequency hopping is implemented using a table containing four channels (frequencies). Channels are selected on a rotating basis (every consecutive transmission is on a different frequency). When first turned on and after 4 consecutive packets have been lost, the Slave goes into a 'waiting for beacon' mode, continuously listening on the first channel in the table.

FCC compliance places additional restrictions on data rate, modulation format, and power output – refer to Application Note AN069 "Low Cost Long Range One Way Audio

Application Note AN082

Communications at 900 MHz” and Design Note DN006 “CC11xx Settings for FCC15.247 Solutions” for further information.

9 Lost Packets\Latency

There are several ways in which a 'lost packet' can be handled, including both simple (mute the audio during the duration of the lost packet) and complex (e.g., interleaving data across three consecutive packets). The idea behind the interleaved data approach is that should a packet be lost, the missing data can be re-created via interpolation, based on correctly received samples in other packets.

Experimental results suggest that a simple muting approach is the least audibly objectionable alternative. If a packet is lost, the audio is simply muted for the duration of the packet. Interpolation of missing data using any practical algorithm invariably leads to audible 'clicks' and 'pops'. A further advantage of this simple approach is that latency (the time delay between when audio is sampled by the ADC and when that sample is 'played back') is minimized. For this implementation, latency is 13.5 ms, short enough that it is not audibly annoying.

10 System Timing

The ADC data must be sent in 'packets'. Every packet contains some fixed overhead, including a preamble field (4 to 12 bytes, 8 bytes in this application), sync field (2 to 4 bytes, usually 4 bytes as in this application), CRC field (2 bytes), a packet length specifier (1 byte), and a MAC address (1 byte). In addition, the CC1110 (CC2510) requires 88.4 μ s to transition from the IDLE state to either the RX or TX state, and 721 μ s to calibrate the PLL.

Packet overhead can be minimized by maximizing packet length. However, 'long' packets are more likely to be corrupted during transmission than 'short' packets. Additionally, audio latency and the length of the 'blank out' period (if a packet is lost) increase with increasing packet length. A timing diagram of the Master is shown in Figure 3, below.

- Audio samples per packet: 54
- Audio Sampling Rate: 8 kHz
- Audio data rate: 64 kbps in each direction (voice quality)
- Radio Data Rate: 250 kbps
- Preamble Bytes : 8
- Sync Bytes: 4
- Packet Length (excluding preamble, sync, and CRC fields): 57 bytes
- Total Packet Length (including preamble, sync, and CRC fields): 71 bytes
- IDLE to TX and IDLE to RX: 89 μ s.

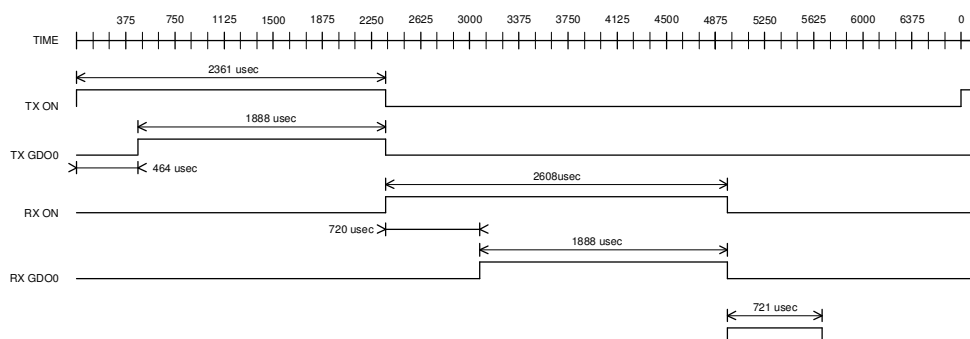


Figure 3. Master Timing

In Figure 3, "TX ON" and "RX ON" include the time required to change the radio from the IDLE state to the RX or TX state. "GDO0" refers to a signal available on pin 34 of the CC1110 or CC2510 (P1_5). It asserts when the sync word has been sent/received, and de-

asserts at the end of the packet. 1255 μ s after enabling the receiver bit 3 ("SFD") of the PKTSTATUS register is checked to see if it is asserted. This bit is set when the sync word is found and reset after a packet is received. If the bit is not set, it is assumed that the expected packet has been lost, the receiver is shut off, and the packet is marked as 'lost'.

Figure 4 shows a timing diagram for the Slave.

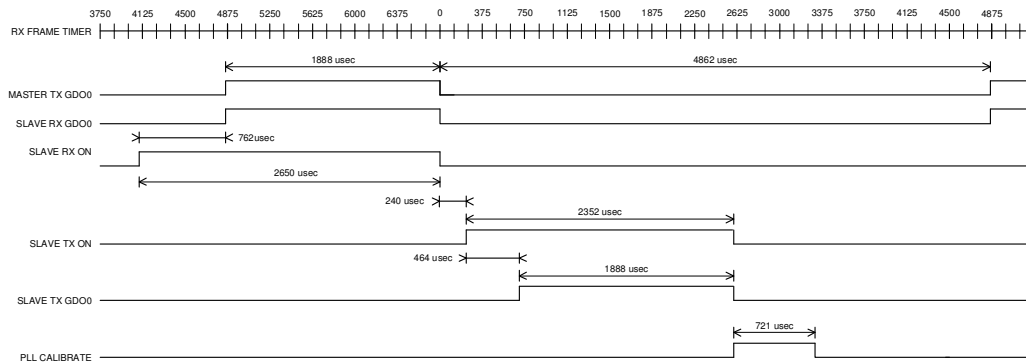


Figure 4: Slave Timing

Note that the Frame Timer is reset immediately after a packet is received from the Master and that the receiver is turned on approximately 2650 μ s before the timer 'times out'.

11 Other Sample Rates

Sampling rates other than 8 kHz are possible as is increased sample resolution (by disabling compression). However, the resulting audio and RF bit rates must be within the limitations of the CC1110's (CC2510's) maximum data rate (500 kbps) and maximum packet length (255 bytes). Table 1 lists some allowable ADC sample rates and resolutions.

Mode	ADC Sample Rate [kHz]	μ -Law Compressed?	Audio Bit Rate [kbps]	RF Bit Rate [kbps]	Code Available?
Two Way	8	Y	64	200	CC1110
Two Way	7.125	N	114	300	CC1110
Two Way	16	Y	128	500	
One Way	8	Y	64	100	
One Way	8	N	128	250	
One Way	12	N	192	300	CC1110 CC2510
One Way	16	Y	128	250	
One Way	16	N	256	500	
One Way	24	Y	192	300	
One Way	24	N	384	500	CC2510

Table 1. Sample Rates and Resolutions

Sample code is available from Texas Instruments for some of these configurations, as indicated in the above table.

12 Additional Specifications

- Resolution: 16 bits, compressed to 8 bits using μ -Law algorithm
- Spread Spectrum Technique: Frequency hopping (2 or 4 channels)
- Hop Rate: 148 hops/sec
- Modulation: GFSK
- RF Output Power:
 - 0 dBm (1 mW) maximum using CC2510 EVM (2400 - 2483.5 MHz)
 - 12 dBm (15.8 mW) maximum using CC2510_CC2590EM (2400 - 2483.5 MHz)
 - 10 dBm (10 mW) maximum using CC1110 EVM (868 - 928 MHz)
 - 20 dBm (100 mW) maximum using CC1110 + PA EVM (868 - 928 MHz)

Warning: When using the "CC1101 LNA for Codec" card, do not use radio frequencies that are within 500 kHz of an integer multiple of 13 MHz (e.g. 910 MHz). This is because the MCLK line to the TLV320AIC26 is clocking at 13 MHz. With the increased sensitivity provided by the LNA, even very high harmonics (e.g., the 70th) of this frequency can interfere with low level signals (-95 dBm and lower).

13 Default Codec Settings

The TLV320AIC26 Codec includes many features, the characteristics of which are controlled via register settings. These are explained in the TLV320AIC26 data sheet [5].

Table 2 lists default Codec register settings.

Application Note AN082

Codec Register	Field	Default Setting
Audio Control 1	Codec Word Length	16 bits
	DAC Sampling Rate	8 kHz
	ADC Sampling Rate	8 kHz
	ADC Input	Single-ended MIC ¹
ADC Gain Control	ADC PGA Gain	26 dB ¹
	AGC target Level	-5.5 dB
	AGC Time Constant	Attack 8 ms, Decay 100 ms
	AGC Enable	AGC Disabled ²²
DAC Gain Control	Left Channel Volume Control	0 dB, Not Muted
	Left Channel Volume Control	0 dB, Not Muted
Sidetone Control	Analog Sidetone Mute Control	Muted
	Digital Sidetone Mute Control	Muted
Audio Control 3	Reference Sampling rate	44.1 kHz
	DAC Maximum Output Swing And Common Mode Voltage	Output swing = 2.402 Volts $V_{CM} = 1.62$ Volts
PLL Programmability Fsref = 13000 · 7.5618 / 2048 = 47.999707 kHz	PLL Enable	Enabled
	Q Value	2
	P value	1
	J value	7
	D value	5618

Table 2. Default Codec Register Settings

14 Features

- Frequency Hopping (4 channels)
- Uses the Texas Instruments TLV320AIC26 Codec, which includes a programmable gain microphone amplifier, an AGC (Automatic Gain Control), and many other features.
- Low external component count.
- Manual Volume Control (Speaker): The card uses a Texas Instruments TPA6011A4 stereo power amplifier [6]. Volume is controlled via a one-turn potentiometer.

15 Conclusion

This document describes a set of cards and software that demonstrate telephone quality audio over a 900 MHz or 2400 MHz two-way, full duplex link, using the CC1110 or CC2510 SoC transceiver and the TLV320AIC26 Codec. With modification to the software, many other combinations of sample rate and resolution are possible, as well as one way (simplex) audio communications.

¹ Pins 3 and 4 of JP1 ("SEL AUX IN") open. When the jumper is installed, ADC Input is set to "Single-ended AUX" and the ADC PGA Gain is set to 0 dB.

² Pins 1 and 2 of JP1 ("ENA AGC") open. When the jumper is installed, the AGC is enabled.

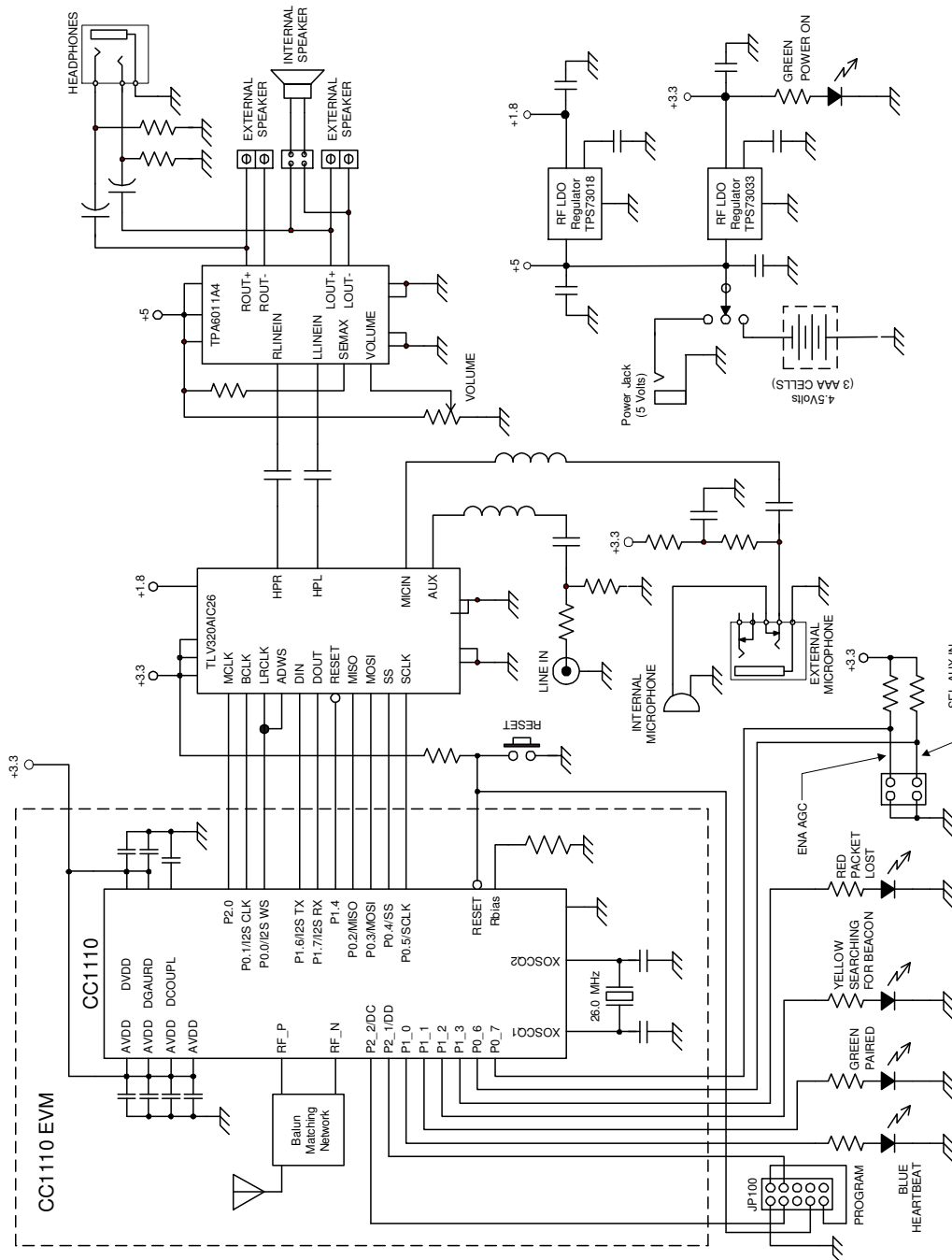


Figure 5. Codec EVM Card Block Diagram

Application Note AN082

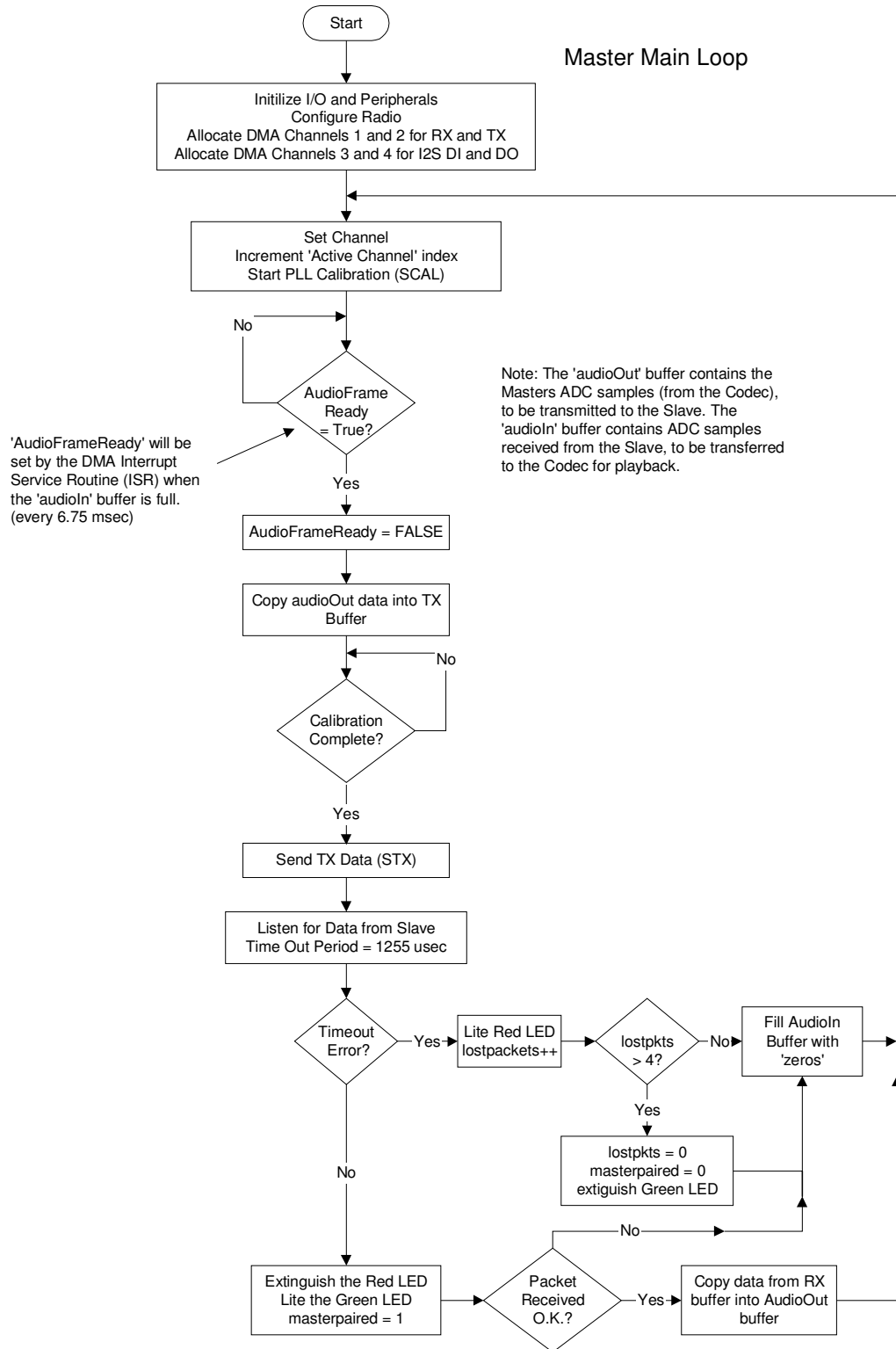


Figure 6: Master Flow Chart

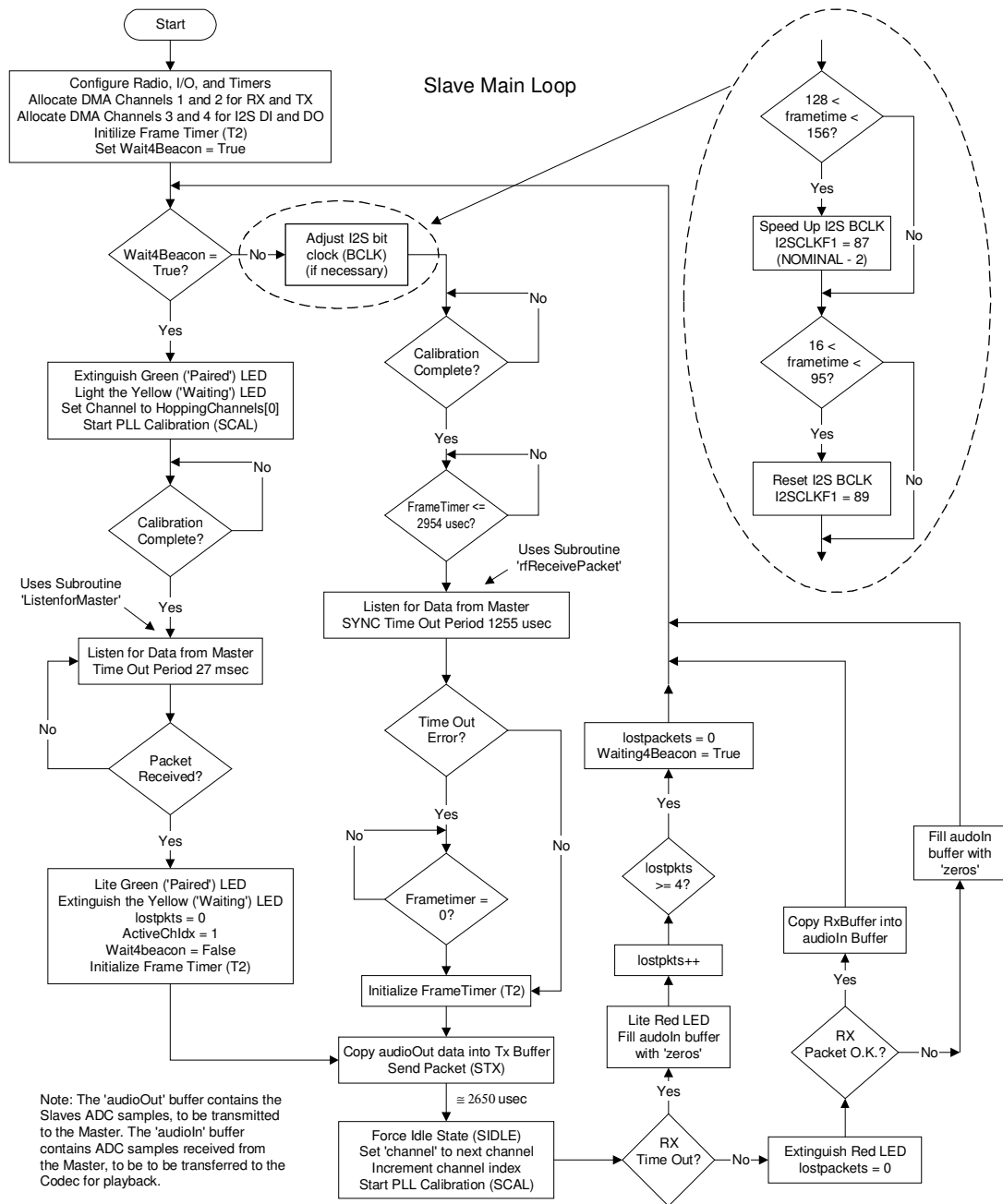


Figure 7. Slave Flow Chart

16 References

- [1] CC1110Fx/CC1111Fx Low-Power Sub-1 GHz RF System-on-Chip (SoC) with MCU, Memory, Transceiver, and USB Controller ([cc1110f32.pdf](#))
- [2] CC2510Fx/CC2511Fx Low-Power SoC (System-on-Chip) with MCU, Memory, 2.4 GHz RF Transceiver, and USB Controller ([cc2510f32.pdf](#))
- [3] CC2510EM Reference Design ([swrr035.zip](#))
- [4] CC1110EM 868 and 915MHz Reference Design ([swrr048.zip](#))
- [5] TLV320AIC26 Low Power Stereo Audio Codec w/Headphone/Speaker Amp & 12-Bit Batt/Temp/Aux ADC ([TLV320AIC26.pdf](#))
- [6] TPA6011A4 3-W Stereo Audio Power Amplifier with Advanced DC Volume Control ([TPA6011A4.pdf](#))
- [7] TPS73018 Low-Noise, High PSRR, RF 200-mA Low-Dropout Linear Regulators ([TPS730xx.pdf](#))
- [8] TPS73033 Low-Noise, High PSRR, RF 200-mA Low-Dropout Linear Regulators ([TPS730xx.pdf](#))
- [9] DN109 Using I2S in CC111xFx and CC251xFx ([swra183.pdf](#))
- [10] AN069 -- Low Cost Long Range One Way Audio Communications at 900 MHz (Rev. B) ([swra237b](#))
- [11] DN006 CC11xx Settings for FCC 15.247 Solutions ([swra123a.pdf](#))
- [12] CC1110-CC1111DK, CC2510-CC2511DK Users Manual ([swru134a.pdf](#))

17 Document History

Revision	Date	Description/Changes
SWRA295	2009.06.17	Initial release.
SWRA205a	2010.10.11	Update

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