MODEL 3700D

EDIT CODE MASTER

INSTRUCTION MANUAL

Revision 1.1, September 1989

WARNING

This equipment generates and uses radio frequency energy, and if not installed and used in strict accordance with the instruction manual, may cause harmful interference to radio communications. It has been designed to comply with the limits for a Class A computing device pursuant to sub-part J or part 15 of FCC rules, which were designed to provide reasonable protection against radio interference when operated in a commercial environment.

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Thanks for your help!

REVISION HISTORY

REVISION	DESCRIPTION	DATE
1.0	Original issue - preliminary release	10/84
1.1	Update of complete manual	09/89

INDEX

1. INTRODUCTION

The Model 3700D uses the latest state of the art technology, combined with our extra intelligent firmware, to offer you the ultimate in performance, reliability, and adaptability. The Model 3700D is a true dual standard NTSC/PAL Generator/Reader combination in an attractive one rack unit high package. The code generator can be preset to lock to its SYNC LOCK input source either by simple frame locking as per EIA standard RS-170 , or where a stable RS-170-A source is available, it will colour lock in accordance with the 4 field NTSC colour sequence. In the PAL standard, either the 4 field or 8 field sequence may be observed. See Appendix II for the SMPTE/EBU standards regarding colour framing.

When switching between standards, hardware, as well as software parameters are changed in order to meet the strict requirements set for the NTSC system by the SMPTE, and for the the PAL system by the EBU.[1] Some of the affected parameters concern the line and frame rates, subcarrier frequency, code bit rates, bit edge rise and fall times, and flag bit assignments. See Appendix I for SMPTE/EBU time code specifications.

The Model 3700D is a combination generator, and high speed reader for SMPTE/EBU Longitudinal Time Code (LTC), and contains a high resolution character generator (VCG) which can be delegated to either the reader or the generator. Thus, the generator will produce uninterrupted time code while the reader may be used to recover time code from another tape without interfering with the generator function.

In NTSC colour systems operation, with a frame rate of 29.97002618 Hz where the time of day is used for indexing, the generator may be operated in the drop frame mode. A D.F. status indicator will light up if the reader data is in the drop frame format.

Two jam sync modes allow regeneration of poor, frequently interrupted or discontinuous time code. In the continuous jam sync mode, the generator is slaved to the reader. The generator may be momentarily synchronized to the reader using MOM JAM.

The recovery of recorded time code at other than play speed has always presented some degree of difficulty. Due mainly to limitations imposed by magnetic head and audio frequency amplifiers, the reproduced code waveform at sub-playspeeds often suffers from severe distortion, particularly with low end 3/4 inch recorders lacking a separate time code track. The high speed reader in the 3700D employs sophisticated input conditioning and clock/data separator circuits to reliably recover time code over the full shuttle and wind speed range of most VTR's. You'll appreciate the silk-smooth reader display update.

Both the generator and reader are capable of working with the unassigned user bits. Several modes of operation are possible. The generator may be preset to insert decimal values for each group in the generated code, and the reader will read decimal values for each binary group. In addition, the user may select the transfer of either reader time or reader user bits into the generator user bits, thus, allowing pre-edit frame addresses to be preserved when new continuous time code is laid down. This mode may also be useful for synchronizing audio and video tracks or recording film footage numbers in a film to tape transfer.

The 3700D is also able to insert strings of ASCII characters into the generator user bits from a computer or terminal. Several formats including full screen and caption modes are available. The reader decodes the alpha-numeric user bits recorded in this format and displays them on the built-in character generator.

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1 References to EBU standards appear in brackets following references to SMPTE standards throughout this manual.

The Model 3700D is equipped with a high resolution character generator which provides white characters keyed into a black background. The character display may be delegated to either the generator or reader time or user bit data. Horizontal and vertical positioning and selection of 1 of 2 sizes are controllable from the front panel. Characters may be keyed into the picture to which the generator is locked, or a separate program input.

The 3700D provides BCD data output from the Reader using an 8 bit wide multiplexed parallel port. Remote control of the commonly used functions may be accomplished using the parallel key matrix interface. Full computer control, including alpha-numeric user bit entry and reading is possible using the RS-232-C serial port.

2. INSTALLATION

2.1 MOUNTING

The standard unit is equipped with rack mounting angles and fits into a standard 19 inch by 1 3/4 inch (483mm x 45mm) rack space. The mounting angles may be removed if rack mounting is not desired.

2.2 POWER

Power requirements are 115 or 230 volts AC at 50 or 60 Hz, switch selectable at the rear panel. Before connecting the line power, be sure to select the proper line voltage. Also, check that the line fuse is rated for the correct value. Never replace with a fuse of greater value.

2.3 GENERATOR SYNC LOCK

For proper frame/address synchronization in video tape applications, the generator must be locked to a stable 1 volt p-p composite video or colour black source, applied to the generator input video loop. The internal sync separator has a high impedance input tapped off the loop through, therefore, the video signal must be properly terminated at the end of the line. The front panel standards switch must be set for the video standard connected. (NTSC or PAL)

When colour frame synchronization is desired, the sync to subcarrier (Sc-H) phase relationship of the video source must conform to the NTSC RS-170-A or the PAL 8 field specification. (See Appendix II for information regarding colour framing specifications.) Selection of the colour framed or non colour framed mode is accomplished from the front panel. (See Section 3.1.) When the video source does not meet the colour frame specifications, the non colour frame mode must be selected to insure a proper generator lock condition. An audible alarm indicates loss of gen-lock condition. (See Section 3.1 ALRM.)

2.4 CHARACTER GENERATOR

The program source for the character generator may be selected as the video to which the generator is locked, or a separate video source. When a separate video source is used for off line time code burn-ins, it should be vertically synchronized to the generator input video for proper operation. Separate character generator outputs are provided to drive a monitor and a video recorder. Figure 2-1 shows proper connection of the generator lock input and character generator input and outputs.

When the VCG program source is used to lock the generator, connect the program source to the VCG input loop, and place the switch in the up position. This connects the two input loops together and also provides an internal 75 ohm termination. If external termination is desired, resistor R1 located beside the switch on the video input board, should be removed.

When using separate VCG program and generator lock sources, connect them to the appropriate input loop and place the switch in the down position. External termination must be provided.

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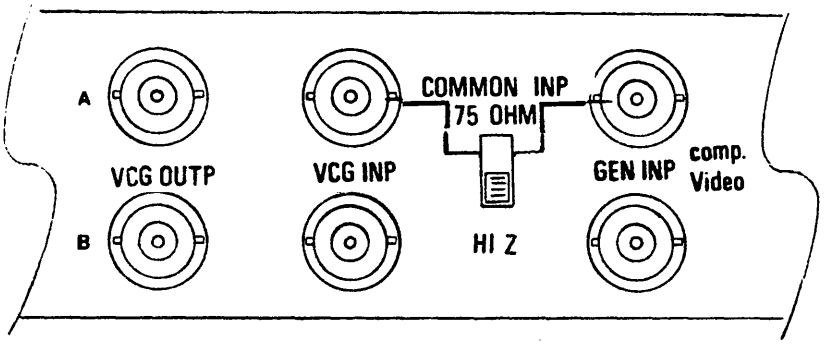


Figure 2-1 - Video Connections

2.5 LONGITUDINAL TIME CODE IN/OUT

The generator code output is available on two XLR connectors at the rear panel. Output level is adjustable from -12 dBm to +6 dBm into a 600 ohm load using the level adjustment located on the rear panel. The generator code output should be connected to the record input of the time code channel or audio track 2 of your video recorder. (audio track 3 for 1" VTR's)

The reader input connects to your head pre-amplifier output. When using an unbalanced input to the reader, the signal should be applied to pin 3 of the reader input connector. Normally, the unused input, (pin 2) should be connected to ground (pin 1).

2.6 PARALLEL DATA OUTPUT/REMOTE CONTROL

2.6.1 Parallel Reader Data Output

Reader time and user bit data are multiplexed on 10 parallel output lines at the 25 pin connector (See Section 2.8 for pin assignments) as follows:

> The clear to send (BCDCTS) line is brought low at the beginning of the sequence. Then, 4 bit BCD address is output on lines BCD0 thru BCD3 along with a positive going strobe (BCDSTB). Eight bits of data are then output in a packed BCD format on lines BCD0 thru BCD7 along with a negative going strobe. This cycle is repeated for each of the 8 digit pairs listed below. When the output sequence is complete, the BCDCTS line returns high. The sequence of data outputs is presented once per frame.

ADDRESS	DIGIT PAIR
0000	Frames
0001	Seconds
0010	Minutes
0011	Hours
0100	1st & 2nd Binary Groups
0101	3rd & 4th Binary Groups
0110	5th & 6th Binary Groups
0111	7th & 8th Binary Groups

Flag bits are output along with the time information as follows:

POSITION	BIT #	NTSC	PAL
Frames Bit 6	10	Drop Frame	Unassigned
Frames Bit 7	11	Colour Flag	Colour Flag
Seconds Bit 7	27	Phase Parity Bit	Binary Group #1
Minutes Bit 7	43	Binary Group #1	Binary Group #2
Hours Bit 6	58	Binary Group #2	Unassigned
Hours Bit 7	59	Unassigned	Phase Parity Bit

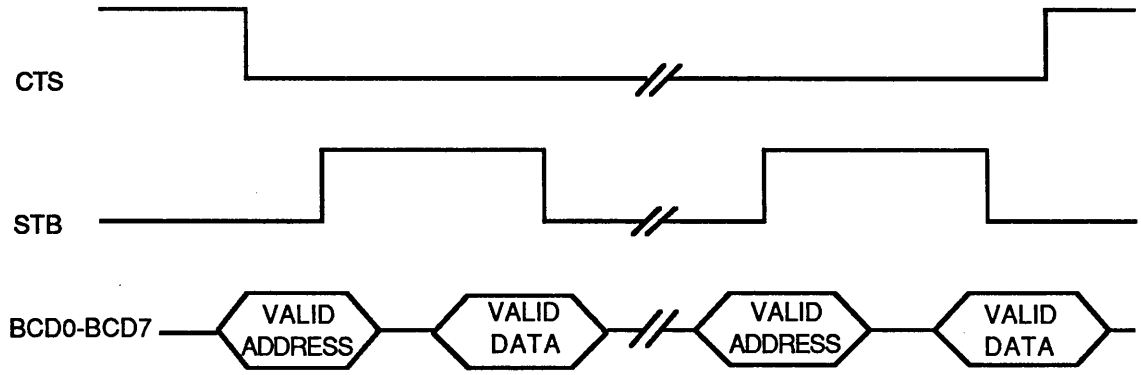


Figure 2-2 - BCD Output Waveforms

2.6.2 Parallel Remote Control

The remote control interface permits control from one or more remote locations. Any or all of the front panel keys can be remoted. Eight pins from the 25 pin connector (See Section 2.8 for pin assignments) are used by the remote control interface. The keypad is arranged in a matrix consisting of 4 rows by 4 columns. Connection of any row with any column by a momentary contact switch uniquely identifies one of the key functions. For multiple locations several momentary contact switches may be wired in parallel. The table below shows the position of each key function in the keypad matrix.

ROW NO.	COLUMN 1	2	3	4
1	GEN U.B	TRNS U.B.	MODE	RDR U.B.
2	CONT	GEN	RD'R	FRZ
3	MOM	H POS	SET	not used
4	BLNK	V POS	CLR	not used

Note: Static electricity can destroy CMOS device connected to remote control interface cable. USE CAUTION WHEN HANDLING.

2.7 RS-232-C SERIAL PORT

The 3700D provides an RS-232-C interface for remote control, and alpha-numeric user bit input and output. The 3700D is configured to make the serial port appear as a Data Communication Equipment (DCE) device. In this configuration, the 3700D expects an external Data Terminal Equipment (DTE) device to be connected to its serial port. See Sections 3.7 and 3.8 for a description of the alpha-numeric user bit and remote control functions. Section 2.8 outlines the pin assignments for the serial port. The following explanations of the serial port signals are given to aid the user in connecting the port properly.

The external computer (DTE) must be set to communicate at 4800 baud, with one start bit, 7 data bits, one parity which is set to zero (zero parity), and one stop bit.

A "communications protocol" is a convention whereby the 3700D tells the DTE device, (computer or terminal) to stop transmitting characters while those already received by the 3700D are being processed, and when to resume transmitting. A communications protocol is necessary when a computer sends data at a rate of more than approximately 30 characters per second. If no communications protocol is used by your computer, the 3700D input buffer will overflow and data will be lost. The two protocols supported by the 3700D are described more fully below.

2.7.1 RTS/CTS Protocol

The simplest protocol, RTS/CTS is implemented by connecting the RTS and CTS connections on the RS-232-C connector. To use this protocol, your computer device must stop sending characters when the 3700D brings its CTS line low, and resume transmitting when the CTS line goes high again. Usually, this involves connecting the serial port as shown below.

Computer End			3700D end		
2	(TXD)	---------->	2	(RXD)	Data input to 3700D
3	(RXD)	<----------	3	(TXD)	Data Output from 3700D
4	(RTS)	---------->	4	(RTS)	Must be high always
5	(CTS)	<----------	5	(CTS)	High when 3700D is ready to receive
6	(DSR)	----			
20	(DTR)	----|			
7	(GND)	----------	7	(GND)	Signal Ground

Note:
1. On some computers pins 6 and 20 may have to be strapped together in the connector at the computer end of the cable, without running them to the other end.
2. The RXD and TXD connections may be reversed on some computers.

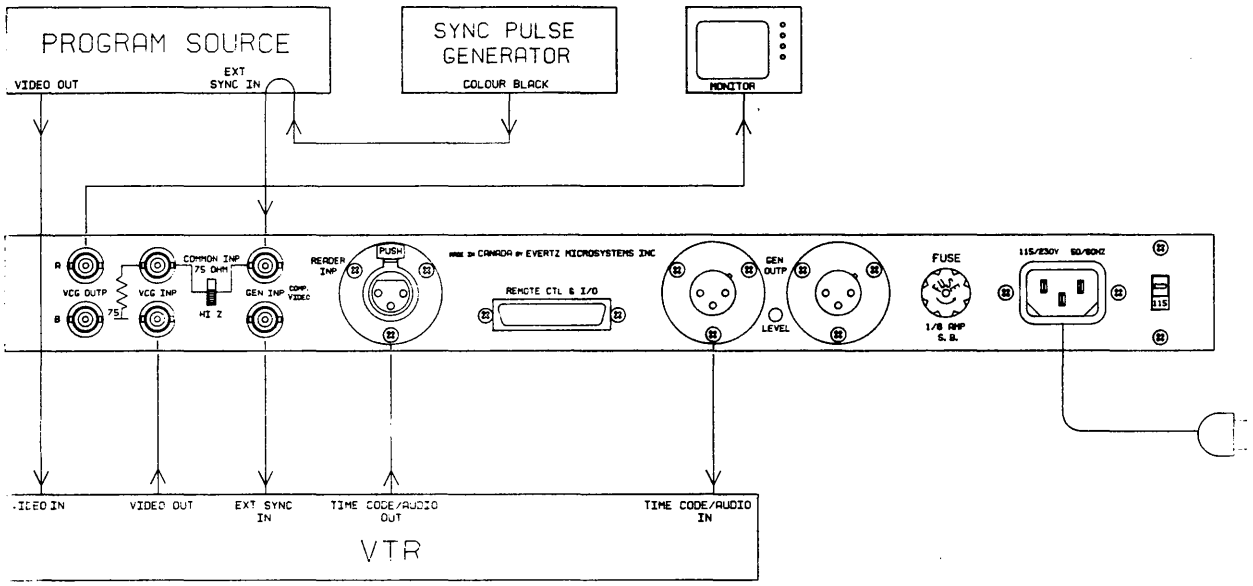
2.7.2 XON/XOFF Protocol

Under this protocol, the 3700D transmits an "XOFF" character (DC3 decimal ASCII 19) to the computer when the computer should stop transmitting characters, then transmits an "XON" character (DC1 decimal ASCII 17) when transmission may resume. Connection of the serial port is the same as for the RTS/CTS protocol, except that the CTS line may be left disconnected.

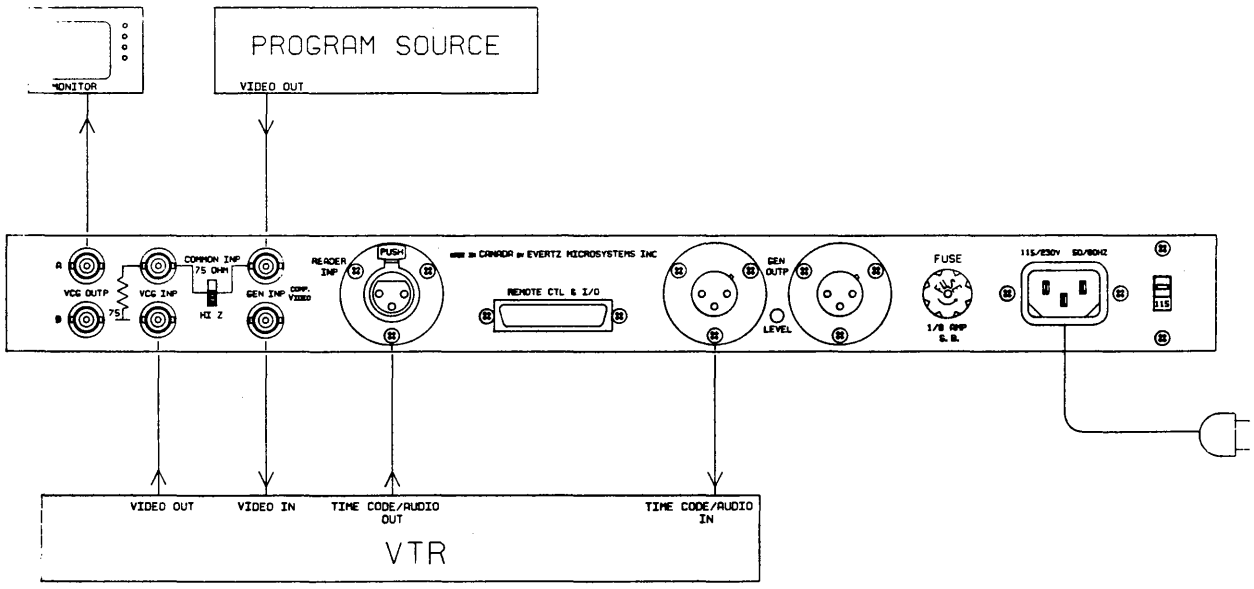
2.8 SAMPLE CONFIGURATIONS

Several sample installation set-ups are diagrammed below to aid the user in properly connecting the Model 3700D into his system. Contact us for other applications.

Figure 2-3a illustrates the preferred set-up for generating code. The house reference black signal is used to gen-lock the 3700D, the program source, and the VTR. When operating the 3700D in the colour frame mode, the program source video must have the same Sc-H (See Appendix II) as the reference black. When playing back the tape, the time code numbers will be read and displayed in the monitor video. Figure 2-3b illustrates an alternate set-up for generating code. The program video is used to gen-lock the 3700D directly. The program video must have a stable Sc-H for the colour frame mode to be utilized.

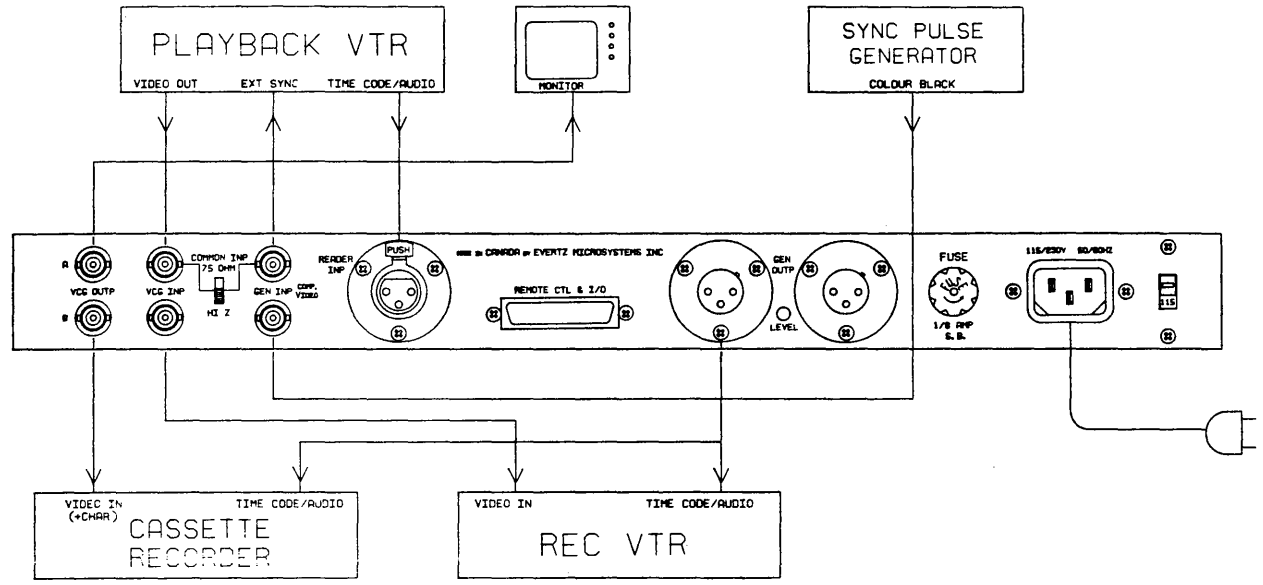


(a) Locking to an External Source

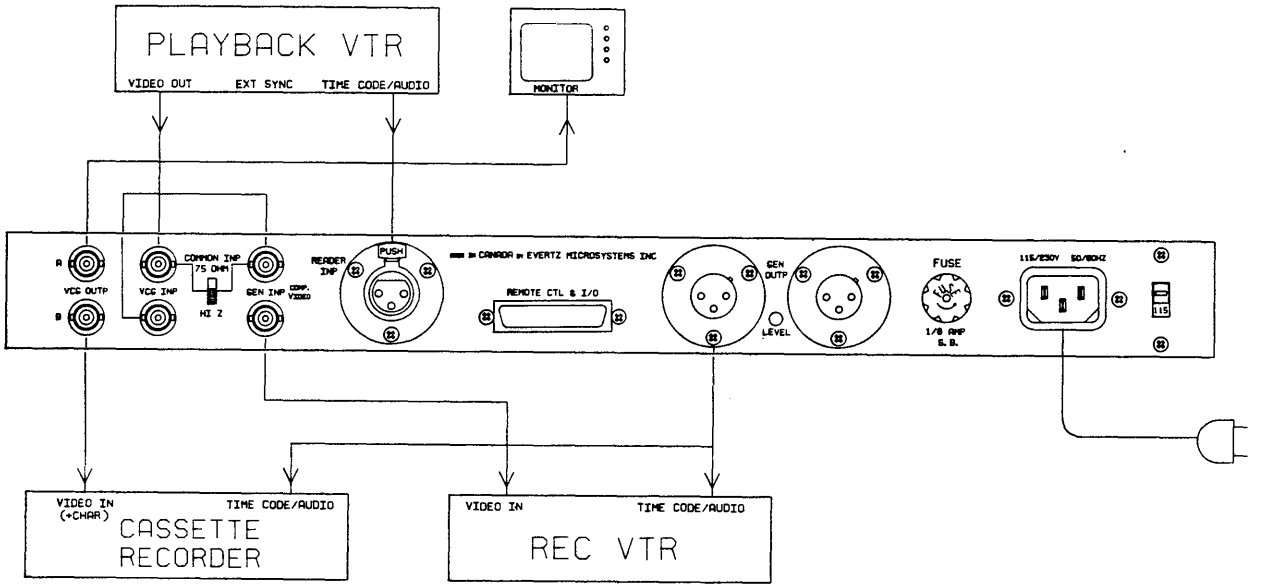


(b) Locking to Program Video

Figure 2-3 - Basic Generator/Reader Configuration



(a) Locking to an External Source



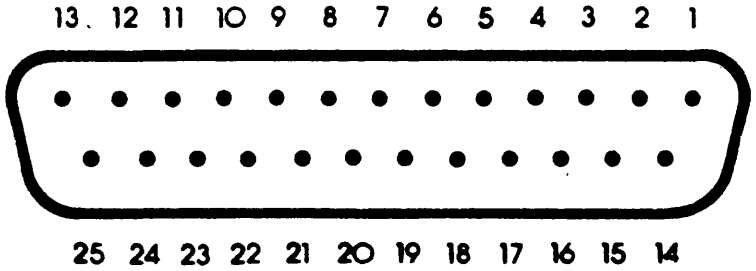
(b) Locking to Program Video

Figure 2-4 Dubbing and Off-Line Character Burn In

Figure 2-4a illustrates the preferred set-up for dubbing code from one tape to another, and for making off-line cassettes with character burn-ins. The house reference black signal is used to gen-lock both the 3700D and the playback VTR, thus ensuring that the playback video is synchronous to the 3700D's gen-lock input. Time code is read from the playback VTR and is regenerated by using the continuous jam sync mode of the 3700D. This re-times the code back to the reference video, and reshapes it to the original specifications. (See Appendix I.) Dropouts or unreadable sections of the source code are fixed up by the error by-pass of the 3700D. (See Section 3.4 for more information on Jam Sync.) In the alternate set-up in Figure 2-4b the program video is used to gen-lock the 3700D and as a source for the character inserter. If the program video does not have a stable Sc-H, the non-colour frame mode of the 3700D should be selected.

2.9 I/O CONNECTOR PIN ASSIGNMENTS

Note: To avoid conflict, connect only the pins required for your application.
Pins 2 thru 7 refer to RS-232-C serial port.
Pins 10 thru 13, and 22 thru 25 refer to the remote control interface.
Pins 8, 9, and 14 thru 21 refer to the Parallel BCD data output.



Pin	Name	Description
1	GND	Signal Ground
2	RXD	Received Data 4800 BAUD Zero Parity
3	TX	Transmitted Data 7 Data Bits, 1 Stop Bit
4	RTS	Must be high for 3700D to transmit
5	CTS	High when 3700D ready to receive characters
6	- -	Not Used
7	GND	Signal Ground
8	BCDSTB	Address / Data Strobe
9	BCDCTS	BCD Clear to Send
10	R4	Parallel BCD Output bit 5
11	R3	Remote control Row 4
12	R2	Remote control Row 3
13	R1	Remote control Row 2
14	BCD7	Parallel BCD Output bit 7
15	BCD6	Parallel BCD Output bit 6
16	BCD5	Parallel BCD Output bit 5
17	BCD4	Parallel BCD Output bit 4
18	BCD3	Parallel BCD Output bit 3
19	BCD2	Parallel BCD Output bit 2
20	BCD1	Parallel BCD Output bit 1
21	BCD0	Parallel BCD Output bit 0
22	C4	Remote control Column 4
23	C3	Remote control Column 3
24	C2	Remote control Column 2
25	C1	Remote control Column 1

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3. OPERATING INSTRUCTIONS

The Model 3700D provides a display of time or user bits information for the generator and reader using two 8 digit LED displays, or using characters keyed into the VCG program input video. Operational control is handled by 14 front panel keys. A FORMAT DIP switch permits certain parameters and operating modes to be preset to adapt the unit to your particular operating methods. Eight LED's provide operational status at a glance.

Since all functions are entirely under microprocessor control, certain modifications may have been supplied to meet your particular requirements, and may conflict with the descriptions below.

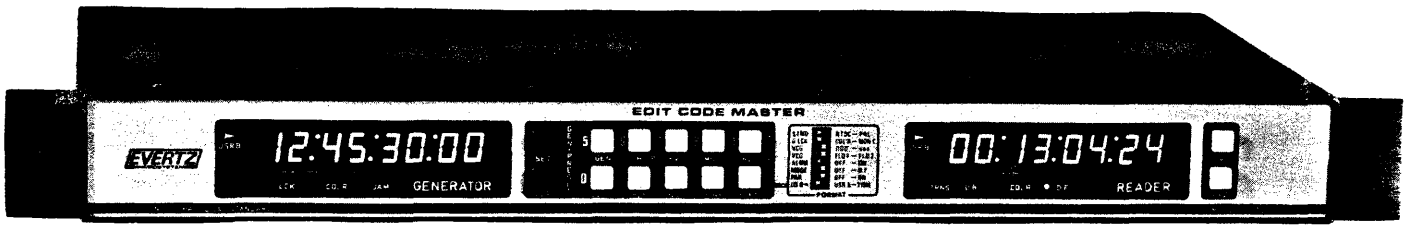

Figure 3-1 - Front Panel Layout

3.1 FORMAT FUNCTIONS

An 8 position DIP switch, located near the centre of the front panel, is used to configure the following operational modes. The unit will operate in these modes until they are altered using a small screwdriver or other pointed device. Some of the remote control commands (See Section 3.7) may overwrite the format switch settings.

STND Selects the video standard used as NTSC or PAL.

GLCK When the standard switch is set to NTSC, selects whether the generator will lock to an NTSC RS-170 source (NON C) or where available, the newer NTSC RS-170-A source (COL'R).

When the standard switch is set to PAL, selects whether the generator will lock to a 4 field PAL source (NON C) or where available, the newer 8 field PAL source (COL'R).

Note: When in the continuous jam sync mode, the colour frame status of the reader overrides the formatted colour frame mode.

VCG Two switches control the size and update time of the character generator.

OO-oo: selects a 16 line per field or 32 line per field character size for the character generator. The small size should be selected when displaying alpha-numeric user bits.

FLD1-FLD2 : Selects whether the VCG characters will be "on time" (FLD1) or 1 field late (FLD2). This latter mode is useful where edits will be performed on field 2, and the character burn-in must correspond to the actual edit point. For most uses, this switch should be set to "FLD1". Special indicators between the seconds and frames digits indicate the field in which the VCG update is occuring. (See Section 3.5.1)

ALRM When ON is selected, the audible alarm indicates the loss of the generator lock condition. The alarm may be temporarily turned off using the CLR button, allowing the user to correct the problem. The alarm will be re-activated if LCK status is achieved and lost again. When OFF is selected, the alarm is totally disabled.

MODE When D.F. is selected, the generator operates in the drop frame mode to provide accurate time of day when locked to NTSC colour sync with a frame rate of 29.97002618 Hz. This mode drops the first 2 frame counts (0,1) at the start of each minute except minute 0,10,20,30,40 and 50, compensating for an approximate timing error of 4 seconds per hour. A special drop frame flag bit is set in the generated code, and a status LED is turned on to signal this operating mode. When OFF is selected, the generator includes all frame counts. When the PAL standard is selected, the setting of the D.F. mode switch is ignored.

Note: When in the continuous jam sync mode, the drop frame status of the reader overrides the formatted drop frame mode.

PAR The purpose of the phase correction parity bit is to compensate for phase reversals in the LTC bi-phase mark modulation that could occur when code inserts are performed. Use of the bi-phase mark parity bit is optional as some readers may not recognize its presence. When PAR is ON, the bi-phase mark parity bit will be put in a state where every 80 bit word will contain an even number of logic zeros, in order that the magnetization transient between bit cell 79 of one word and bit cell zero of the next shall always be in the same direction. The parity bit will be always set to zero if PAR is OFF.

TRNS U.B. Selects either the reader time or user bits as sources for a transfer to the generator user bits to occur when the user bit transfer function is initiated. (See Section 3.4)

Transferring reader time (TIME) is useful when it is desired to record new continuous time code numbers and still retain the original time code numbers for future reference. When synchronizing audio tape machines to video recorders, the audio tape time code may be transferred to the user bits in the new video time code.

Transferring the reader user bits (USR'B) is used when reader time data previously transferred to user bits as above, or other user bit information must be retained when recording new code. When used in conjunction with the continuous Jam Sync mode, both the time and user bits will be transferred to the new tape.

3.2 DISPLAY CONTROL FUNCTIONS

3.2.1 Generator

Two keys located in the bottom row of the numeric key group provide control of the information being displayed in the generator LED display.

GEN U.B. Alternately displays the time or user bit information in the generator LED display. A status LED in the upper left corner of the display indicates when user bits are being displayed. Also, the colons of the display are blanked when user bits are displayed.

BLNK Blanks the frames of the generator and reader LED and character displays. Alternate action of this key restores the normal display mode.

3.2.2 Reader

Two keys located to the extreme right of the front panel provide control of the information being displayed in the reader LED display.

U.B. Alternately displays the time or user bit information in the reader LED display. A status LED in the upper left corner of the display indicates when user bits are being displayed. Also, the colons of the display are blanked when user bits are displayed.

FRZ Freezes the reader LED and character displays. Alternate action of this key restores the normal display mode.

3.3 PRESETTING THE GENERATOR

Twelve keys in the GEN PRESET key group are used to enter time or user bit data into the generator when it is selected for display.

SET When pressed the first time, it initiates a data entry mode that allows presetting of either the time or user bits of the generator, whichever is currently displayed. Dual functioned (white) keys are changed to their numeric values. Depressing any numeric key now will enter the value into the display starting at the left. Unentered digits default to zero if entering the time, or to the previous value if entering user bits. After the required number of digits have been entered, press SET again to complete the data entry mode. Pressing CLR exits from the data entry mode without presetting the time or user bits. Attempts to make illegal entries, ie. 65 minutes will be ignored and the invalid digits will be blanked. Re-enter these digits and press SET to complete the data entry. After the entry mode has been terminated by either SET or CLR the generator display will return to display the generator time, and the numeric keys will return to their control values.

CLR Terminates the data entry and the continuous jam sync modes, returns the display to the generator time, and temporarily disables the audible alarm if it has been activated.

3.4 JAM SYNC CONTROLS

MOM Momentarily jams reader data into the generator.

CONT Continuously jams reader data into the generator. The JAM indicator is turned on to indicate the continuous jam sync mode. The generator and reader times are compared with each other during each frame, automatically compensating for the frame decoding offset. If for any reason they are not equal, the jam is bypassed, the next frame address is substituted by the generator and the JAM LED is blinked. If the number of jam sync errors exceeds 5, the last valid reader time will be jammed into the generator again. In the absence of valid reader code, the generator will be preset to the last valid reader time and will not increment until valid reader code resumes, or the jam sync mode is cancelled by pressing the CLR button.

When the NTSC standard is selected, and the continuous jam sync mode is entered, the generator is set to the drop frame mode that the reader data is recorded in. When the continuous jam sync mode is exited, the formatted generator drop frame mode is restored.

3.5.1 Special Indicators

The following special indicators are used between the seconds and frames digits in the character generator to identify non drop frame and drop frame code (NTSC only) and whether the character generator is updating on time or 1 field late. (determined by the VCG FLD1-FLD2 switch setting-See Section 3.1)

	FLD1	FLD2
Non Drop Frame	Colon (:)	Semi-colon (;)
Drop Frame (NTSC)	Period (.)	Comma (,)

3.6 STATUS INDICATORS

3.6.1 Generator

There are 4 status indicators located beside and under the generator LED display which show operational status of the generator at a glance.

USR'B Indicates user bits being displayed.

LCK Indicates that the generator is properly locked to a composite video or colour black signal.

COL'R Indicates that the unit is operating in the colour frame mode.

NTSC Standard: The unit is properly locked to an NTSC RS-170A video source and the 4 field NTSC sequence is being properly decoded. Frames containing field 1 of the sequence are being assigned an even frame number.

PAL Standard: The unit is properly locked to an 8 field PAL video source and the 8 field PAL sequence is being properly decoded. The EBU specified relationship between the frame address and the television field is being used in assignment of the generator frame numbers. (See Appendix II)

When the generator is operated in the continuous jam sync mode, and the reader data was not recorded in the colour frame format, the COL'R LED will not be illuminated. The generator frame numbers will be slaved to the reader frames.

JAM Indicates the unit is operating in the continuous jam sync mode. When the JAM indicator is blinking, it indicates a variety of problems in the jam sync process. If it is blinking on an irregular basis, the reader could be receiving bad code, there may be a discontinuity in the code, or the code was recorded in a different standard than the 3700D is locked to. If it is blinking on a regular basis, and the reader COL'R LED is on, the reader code may be colour framed to a different field of the colour field sequence.

3.6.2 Reader

There are 4 status indicators located beside and under the reader LED display which show operational status of the reader at a glance.

USR'B Indicates user bits being displayed.

COL'R Indicates that the data being read was recorded in the colour frame mode; ie. the correct relationship between frame address and colour burst phase was adhered to.

D.F. Indicates that the data being read is in the SMPTE drop frame format.

TRNS U.B. Indicates reader time or user bit data is being transferred to the generator user bits.

3.7 RS-232-C REMOTE CONTROL INTERFACE

The remote control features of the 3700D provide the user with the capability to fully control the Edit Code Master with a computer communicating directly to the internal microcontroller. In order to invoke a remote function from software, it is necessary to precede the specific function code with a lead-in code. The lead-in code, ASCII ESC (decimal 27) alerts the 3700D that a special function follows. The lead-in code and the command following it will be interpreted with special meaning, invoking one of the remote control functions. If the code following the lead-in is not one of the valid remote control commands, that code will be ignored.

NOTE:

1. The command code must immediately follow the lead-in code without any intervening characters. (including NULL characters).
2. Some commands require a group of one or more data characters following the command code.
3. All command sequences must be terminated by a carriage return (decimal 13) character. The command will only be acted upon when the carriage return is received.

Once the command sequence has been received, and executed, an acknowledge ASCII ACK character (decimal 6) will be issued by the 3700D, signalling the computer that the command was received, and executed. If the command cannot be executed for some reason, ie. invalid command code, invalid data field, etc., the 3700D will issue a negative acknowledge ASCII NAK character (decimal 21).

The command for generating alpha-numeric user bits uses a slight variance of this format, and will be dealt with in more detail in Section 3.8. Appendix IV summarizes the remote commands described below; the ASCII code chart is shown in Appendix III.

3.7.1 Set Generator Time Source

On receipt of the SET TIME SRC command (ASCII space decimal 32) the 3700D selects the source for the generator clock as defined by the SRC data character. The SRC data can take only the following values:

1 = Free run the Generator clock
2 = Continuous Jam to Reader time
3.= Momentary Jam to Reader time

3.7.2 Set User Bit Source

On receipt of the SET UB SRC command (ASCII ! decimal 33) the 3700D selects the source for the generator user bits as defined by the SRC data character. The SRC data can take only the following values:

0 = Numeric entry from keyboard or using SET GEN UB command
1 = Transfer Reader User Bits
2 = Transfer Reader Time

3.7.3 Set Generator Mode

On receipt of the SET GEN STAT command (ASCII " decimal 34) the 3700D selects various operational modes for the generator as defined by the MODE data character. The mode command overrides the formatted DIP switch settings (See Section 3.1) and allow presetting of the colour frame, drop frame (NTSC standard only) and parity operational modes. Using a mode reset data character (ASCII a decimal 97) returns the 3700D to the operational modes established by the Format DIP switch. The MODE data character can take only the following values:

ASCII	DECIMAL VALUE	DEFAULT	PARITY	COLOUR FRAME	DROP FRAME
@	64	Off	Off	Off	Off
A	65	Off	Off	Off	On
B	66	Off	Off	On	Off
C	67	Off	Off	On	On
P	80	Off	On	Off	Off
Q	81	Off	On	Off	On
R	82	Off	On	On	Off
S	83	Off	On	On	On
a	97	On	As per switch settings		

3.7.4 Set Generator Time

On receipt of the SET GEN TIME command (ASCII (decimal 40) the 3700D sets the generator time to the values defined by the following 8 data characters. The time format is 'HHMMSSFF'. Only valid times in the 24 hour format will be accepted.

3.7.5 Set Generator User Bits

On receipt of the SET GEN UB command (ASCII) decimal 41) the 3700D sets the generator user bits to the values defined by the following 8 data characters. The first data character will be placed in binary group 8 (10 x hours position), etc. Only valid hexadecimal digits (0-9, A-F) will be accepted.

3.7.6 Generate Alpha-User Bits - Full page TEXT mode

On receipt of the GEN ALPHA TEXT command (ASCII , decimal 44) the 3700D initializes the generator to place alpha-numeric text into the generator user bits in the full page mode. All characters received after the <CR> character will be interpreted as text data to be inserted into the user bits. See Section 3.8.1 for a full description of the alpha-numeric text generating mode.

3.7.7 Generate Alpha-User Bits - Two line CAPT mode

On receipt of the GEN ALPHA CAPT command (ASCII . decimal 46) the 3700D initializes the generator to place alpha-numeric text into the generator user bits in the two line caption mode. All characters received after the <CR> character will be interpreted as text data to be inserted into the user bits. See Section 3.8.1 for a full description of the alpha-numeric text generating mode.

3.7.8 Read Generator Time Source

On receipt of the READ TIME SRC command (ASCII 0 decimal 48) the 3700D sends back the selected source for the generator clock as defined below.

1 = Generator clock free running
2 = Continuous Jam to Reader time

3.7.9 Read User Bit Source

On receipt of the READ UB SRC command (ASCII 1 decimal 49) the 3700D sends back the selected source for the generator user bits as defined below.

0 = Numeric entry
1 = Reader User Bits
2 = Reader Time

3.7.10 Read Generator Status

On receipt of the READ GEN STAT command (ASCII 2 decimal 50) the 3700D sends back the status of the generator flag bits as defined below.

ASCII	DECIMAL VALUE	PARITY	BINARY GROUP 2	BINARY GROUP 1	COLOUR FRAME	DROP FRAME
@	64	OFF	OFF	OFF	OFF	OFF
A	65	OFF	OFF	OFF	OFF	ON
B	66	OFF	OFF	OFF	ON	OFF
C	67	OFF	OFF	OFF	ON	ON
D	68	OFF	OFF	ON	OFF	OFF
E	69	OFF	OFF	ON	OFF	ON
F	70	OFF	OFF	ON	ON	OFF
G	71	OFF	OFF	ON	ON	ON
H	72	OFF	ON	OFF	OFF	OFF
I	73	OFF	ON	OFF	OFF	ON
J	74	OFF	ON	OFF	ON	OFF
K	75	OFF	ON	OFF	ON	ON
L	76	OFF	ON	ON	OFF	OFF
M	77	OFF	ON	ON	OFF	ON

ASCII	DECIMAL VALUE	PARITY	BINARY GROUP 2	BINARY GROUP 1	COLOUR FRAME	DROP FRAME
N	78	OFF	ON	ON	ON	OFF
O	79	OFF	ON	ON	ON	ON
P	80	ON	OFF	OFF	OFF	OFF
Q	81	ON	OFF	OFF	OFF	ON
R	82	ON	OFF	OFF	ON	OFF
S	83	ON	OFF	OFF	ON	ON
T	84	ON	OFF	ON	OFF	OFF
U	85	ON	OFF	ON	OFF	ON
V	86	ON	OFF	ON	ON	OFF
W	87	ON	OFF	ON	ON	ON
X	88	ON	ON	OFF	OFF	OFF
Y	89	ON	ON	OFF	OFF	ON
Z	90	ON	ON	OFF	ON	OFF
[	91	ON	ON	OFF	ON	ON
\	92	ON	ON	ON	OFF	OFF
]	93	ON	ON	ON	OFF	ON
^	94	ON	ON	ON	ON	OFF
_	95	ON	ON	ON	ON	ON

3.7.11 Read Generator Time

On receipt of the READ GEN TIME command (ASCII 8 decimal 56) the 3700D sends back the generator time in the format 'HHMMSSFF'.

3.7.12 Read Generator User Bits

On receipt of the READ GEN UB command (ASCII 9 decimal 57) the 3700D sends back the generator user bits. The first character corresponds to the binary group 8 (10 x hours position), etc.

3.7.13 Read Reader Status

On receipt of the READ RDR STAT command (ASCII B decimal 66) the 3700D sends back the status of the reader flag bits. (See table of values in section 3.7.10)

3.7.14 Read Reader Time

On receipt of the READ RDR TIME command (ASCII H decimal 72) the 3700D sends back the reader time in the format 'HHMMSSFF'.

3.7.15 Read Reader User Bits

On receipt of the READ RDR UB command (ASCII I decimal 73) the 3700D sends back the Reader user bits. The first character corresponds to the binary group 8 (10 x hours position), etc.

3.7.16 Read Alpha-numeric User Bits

On receipt of the READ ALPHA UB command (ASCII L decimal 76) the 3700D sends back the alpha-numeric user bits data stored on the two pages of VCG screen memory. See Section 3.8.2 for a fuller description.

3.8 ALPHA-NUMERIC USER BIT CONTROLS

3.8.1 Generating

When generating code with alpha-numeric user bits, connect an RS-232-C computer or terminal to the serial I/O port on the rear panel. (See Section 2.8 for description of serial I/O port pin assignments and I/O format.) The user bit transfer mode should be turned off. (See Section 3.4 U.B. TRNS)

Issuing a GEN ALPHA TEXT or GEN ALPHA CAPT command to the 3700D via the serial port (see Section 3.7.7 and 3.7.8 above) signals the 3700D to enter the 'generate alpha-numerics' mode. All subsequent characters, (after the <CR> that terminated the command sequence) are interpreted as text to be entered into the user bits. The text characters are inserted into the edit code being generated according to the SMPTE/EBU specified format. A special alpha-numeric flag bit is set to indicate alpha-numeric data is present in the user bits. Two characters plus the mode control and character position are inserted into the code each frame. For data security, this data is repeated in two consecutive frames, thus the effective data rate is one character per frame. This permits reliable recovery of the data during tape dropouts, and when the tape is not running exactly at play speed.

The following control keys are used to issue commands controlling the format the text will be displayed in upon reading the code back. (A 'control key' is issued by depressing the <CTRL> key on the keyboard and striking that character.)

CTL-P Transmits a special control character which commands the edit code reader to turn off the alpha-numeric mode and to clear its screen.

CTL-D Terminates the alpha-numeric entry mode, issues an end-of text control sequence in the user bits and returns to await another remote control command.

ESC Terminates the alpha-numeric mode without issuing an end-of-text sequence.

When initialized to either the full screen or caption modes, upper case displayable characters ie. any ASCII character with decimal codes from 32 through 90 inclusive may be inserted into the generator user bits and will appear on the screen if the generator VCG is enabled. See Section 3.5 for VCG controls and Appendix III for ASCII codes.

The character position will advance once for each character entered. When the bottom of the page is reached, the next page will be automatically formatted.

3.8.2 Reading

When reading code with alpha numeric user bits, the reader character generator is used to display up to 2 pages of 14 (16 for EBU) lines of 32 characters each as they are received. (The reader VCG must be turned on to enable alpha-numeric user bit display - See Section 3.5) At least the first 2 frames of user bits received with the alpha flag bit set must contain either a CTL-A or CTL-C characters which are used to configure the screen for full screen mode or caption mode respectively. Successive characters are displayed as they are received. The Reader time is displayed in the bottom left corner for full screen mode and in the top left corner for caption mode. If the recovered data overwrites the reader time, then it will be disabled until the next page is formatted.

Pressing the V POS key views the next page of alpha-numeric data that was read and stored in the screen buffer. Pressing the V POS key again will return to the original page.

Receiving special control characters (issued by the CTL-P command above) turns off the alpha mode and restores the screen to its normal operation. Turning the reader character generator off using the RD'R VCG key on the front panel also terminates the alpha mode of the reader, and clears the screen.

When there is alpha-numeric data stored on the screen, a READ ALPHA UB command sends the screen data out to a computer via the serial port, as it is shown on the screen.

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4. TECHNICAL DESCRIPTION

The Model 3700D is a microprocessor based system functionally divided into the following major hardware subsystems:

1. Microcomputer and Display/Keypad
2. LTC Generator
3. High Speed Reader
4. Video Character Generator

See Drawing 3600-30 for a functional block diagram.

4.1 MICROCOMPUTER

At the heart of the model 3700D is an 8039 microcomputer,(MCU),U20. Its two 8 bit bi-directional ports and 8 bit bus provide peripheral interfacing to the rest of the circuit. Scratch pad and data RAM are provided internally by the MCU, and only the external VCG RAM is required. The MCU and program memory PROM are located on a separate sub-module 8750.

An onboard oscillator, also part of the MCU is crystal controlled. Its 10.08 MHz is internally divided by 15, resulting in an operating frequency (ALE) of 672 KHz. The processor frequency must be properly calibrated for proper generator locking to occur. It can be measured at TP-29, (ALE) and may be adjusted using VC1.

Serial I/O is accomplished using an 8251 USART, U23. RS-232-C driver U21, and receiver U22 provide the necessary level translation. Baud rate oscillator U27 runs at 16 times the baud rate (76,800 Hz) can be measured at TP-27.

4.1.1 Display/Keypad Interface (Dwg. #3700-35)

Two 8 digit displays, an 8 position DIP Format switch, and a 15 button keypad contained on a separate circuit card (3700-02) interface to the MCU via a 20 conductor ribbon cable. The 8 digit displays and status LED's are multiplexed; that is segment information for each digit is presented in coincidence with a digit enable pulse to the appropriate digit. The 14 keys and DIP switch are arranged in a 4 x 6 matrix. Data from 4 keys or one half of the DIP switch is latched into U5 at the time of the digit enable pulse, thus scanning the total array.

4.2 GENERATOR

4.2.1 LTC Bit Rate Generator (Dwg. #3600-31)

The MCU system clock, (ALE, TP-29) is divided down by U45, U30a and associated components to provide a clock of approximately 168 KHz to the T1 input of the MCU. The MCU divides this internally and generates the time code edge for edge on P10. This output is shaped by U24 and amplified by U1 and U2 to provide the adjustable code output level.

4.2.2 Sync Separator (Dwg. #3600-32)

Composite video is buffered by Q7 and Q6 and AC coupled into U40b. Immediately following each horizontal sync pulse a sample pulse is generated at U40c which allows U40a to compare the actual DC level of the video to ground potential. If they are not equal, U40a generates an error signal which adjusts the bias point of Q7 thus ensuring proper operation of the video keyer with varying video and sync levels. Comparator U39 switches when the negative sync tip goes below its half amplitude point, producing composite SYNC. (Measured at TP-12) Composite SYNC is integrated by U24f to derive vertical sync (VSYNC) which sets flip flop U30b, enabling sync pulse counters U31 and U32. The next sync pulse (the first vertical serration) generates an output on U31 pin 7 which, when ORed with 3/4 H from U35a and SYNC clocks on U36a, generating a frame pulse interrupt (FRM INT, TP-19) to the MCU.

4.2.3 Colour Frame Detector (Dwg. #3600-32)

Monostable U37a is triggered by the leading edge of SYNC and times out about 6µsec later. U37b is triggered by the trailing edge of U37a, generating a burst sample window (BSAMPLE) at the mid point of the burst. The length of BSAMPLE is slightly less than one half of one cycle of subcarrier (approx 90 nsec) for colour frame operation and slightly more than one subcarrier cycle (approx 250 nsec) for non colour frame operation.

Burst, extracted from the video by U26e is ORed with count 11 (9 for PAL) of sync counter U32 and fed to the clock input of phase discriminator U36b. If a positive going transition of burst occurs during the burst sample window, in the first field of the frame, then U36b is clocked on, generating a COL'R SYNC input to the MCU. (TP-17)

Calibration of the colour frame detector is accomplished by adjusting the exact position of BSAMPLE with respect to SYNC using VR2 (VR3 for PAL). All units are calibrated for both standards at our plant. If it becomes necessary to recalibrate for either standard, the following procedure must be followed closely. You will need a Sync pulse generator (SPG) which conforms to the RS-170-A (8 field PAL) standard, and which provides a colour field identification pulse output. You will also need a dual trace oscilloscope.

1. Connect the generator input loop to the SPG and properly terminate it. Set the COL'R/NON C switch to COL'R, and ensure that you have set the NTSC/PAL switch for the video standard in use.

2. Display the colour field #1 identification pulse from your sync generator on channel A of your scope. Set up the time base to show two pulses.

3. Display COL'R FRM (TP-18) on channel B of your scope. COL'R FRM is an active high pulse.

4. Adjust VR2 (VR3 for PAL) slowly until COL'R FRM coincides with your sync generator field #1 identification pulse. Adjust VR2 (VR3) clockwise until COL'R FRM disappears or moves halfway between the two pulses on channel A. Mark this position of VR2 (VR3) with a pencil. Adjust VR2 (VR3) counterclockwise until COL'R FRM reappears coincident with your sync generator field #1 pulse and continue adjusting VR2 (VR3) until COL'R FRM disappears again. Mark the position of VR2 (VR3) with a pencil. Position VR2 (VR3) halfway between the two marks. The LCK indicator should be on.

4.3 HIGH SPEED READER (Dwg. #3600-31)

Incoming code is decoupled and amplified by U3, U4, U11 and associated components to provide a regenerated reader data signal at U11 pin 11. (TP-7) A series of timing pulses, generated by U9 and U10, is used to properly decode 0 and 1 bits of the incoming code. A constant amplitude ramp is generated by U5 and associated components. Three quarters of the peak ramp level is used as a reference on comparator U6 to decode the data from the clock transitions. If the next code bit is a 0, then the ramp will exceed the reference before the next transition. If the next bit is a 1, then an extra transition will occur before the ramp exceeds the reference, clocking flip flop U9a on. The LTC data (TP-4) is shifted through sync detector U12 and U14 into one half of shift register U16. Twelve consecutive 1 bits, detected by U13, clock flip flop U15a on, freezing the sync word data at the outputs of U12 and U14, and generating a LTC RDY signal (TP-9) to the MCU when it has received one frame of data. Direction information (FWD/REV, TP-10), derived from the last bit of the sync word is also fed to the MCU. A valid reader sync word toggles flip flop U15b enabling the other half of U16 to collect data from the next frame while the MCU is unloading data from the previous frame through switch U17.

4.4 VIDEO CHARACTER GENERATOR (Dwg. #3600-33)

The character display is formatted to allow 14 (16 for PAL) rows of 32 characters in the small size and 7 (8 for PAL) rows in the large size. Each of the character positions corresponds to one of 512 locations in RAMs U48 and U49. The MCU writes characters into specified locations of the RAM corresponding to the position of the characters on the screen. RAM locations are scanned during each television field. Valid characters address corresponding sections of the character PROM U56 and character data is shifted out from U57 and keyed into the video by U44. Data bit 7 from the RAM disables the keyer control flip flop U51a, allowing the program video to pass through at all other positions.

RAMENA is used to switch the address and data lines of the RAM from the scanning logic onto the MCU bus while new character data is being entered. Character output is blanked during RAM updates to avoid random character noise in the video.

4.4.1 Character Size and Positioning Adjustments

Horizontal size of the characters is adjusted by VR6. The starting position of the characters at the left of the screen is preset but may be altered by varying the value of R103.

4.4.2 VCG Keyer Setup

The VCG has its own video amplifier and sync separator. U41b and associated components extracts composite sync from the video. Immediately following each horizontal sync pulse a sample pulse is generated at U41c which allows U41a to compare the actual DC level of the video to ground potential. If they are not equal, U41a generates an error signal which adjusts the bias point of U42d, thus, ensuring proper operation of the video keyer with varying video and sync levels.

The keyer control signal from U51a switches U44c on and U44a and U44d off for program video and vice versa for characters. When U44d is on, character dots are added to the black level of the video generated at U44a.

To calibrate the video keyer, connect colour bars from your sync generator to the VCG input loop and to channel A of your scope, and terminate it. Connect the VCG output to channel B of your scope and terminate it. Adjust the GAIN trimpot (VR4) so that the output amplitude matches the input. Adjust the CHAR LEVEL trimpot (VR5) so that the inserted characters are slightly above peak white luminance level.

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APPENDIX I:

SMPTE/EBU TIME AND CONTROL CODE SPECIFICATIONS

INTRODUCTION

The SMPTE/EBU Time and Control Code is a digital code which is used for timing and control purposes on television tape machines and on associated audio tape machines, if any. The original code format, developed in the early 1970's, is recorded on a longitudinal track with audio characteristics, and is referred to as Longitudinal Time Code (LTC). Since then, new video recording formats have appeared which can be used at very slow tape speeds. A new version of the time code was developed which allows reliable recovery right down to still frame. This code, inserted in the field blanking interval of the video signal itself is referred to as Vertical Interval Time Code (VITC).

1. LONGITUDINAL TIME CODE

LTC is a digital signal comprised of 80 bits of information, numbered 0 through 79 inclusive, which are evenly spaced over an entire television frame. The modulation method is such that a transition occurs at the beginning of every bit period. A binary "one" is represented by a second transition one half bit period from the start of the bit. A "zero" bit is represented when there is no transition within the bit period. This system, known as bi-phase mark is illustrated below.

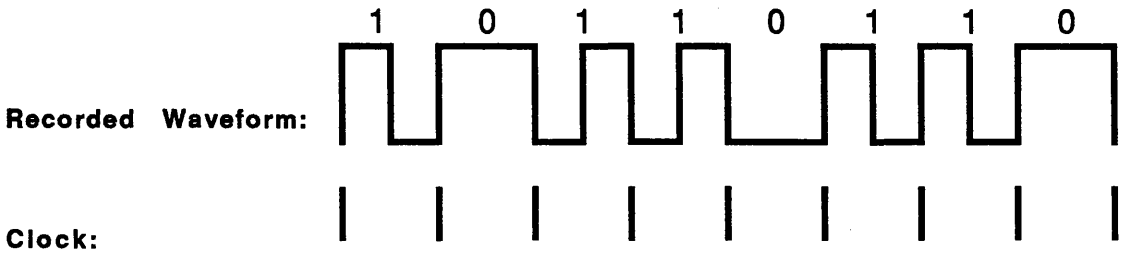


Figure I-1 Bi-Phase Mark Encoding Scheme

The nominal bit period is 80 times the television frame rate (30 Hz for NTSC 25 Hz for PAL). The clock edge before the first address bit (bit 0) occurs during the field synchronizing pulses at the start of field one of the television frame with which the code word is associated.

Each 80 bit code word is comprised of 26 time bits, 6 flag bits, 32 user bits and 16 sync bits. The basic structure of the time bits is based on the Binary coded decimal (BCD) system. In those cases where the count does not attain 9, only 2 or 3 bits are required, rather than the normal 4 bits. These six bits are used as flags to indicate various operational modes as follows:

Drop Frame (NTSC Only): If frame numbers (0,1) at the start of each minute except 0,10,20,30,40, and 50 are omitted from the count to resolve the difference between real time and colour time a "1" is set.

Colour Frame: If colour frame identification has been intentionally applied to the time numbers, a "1" is set.

Bi-phase Mark Phase Correction: This bit is put in a state such that every 80 bit word contains an even number of logic zeros.

Binary Group Flags: The 32 bits within the eight user bit (binary) groups may be assigned in any way if both binary group flags are zero. If an eight-bit ASCII character set is used for user bit data, then the first binary group flag is set to "1". At this time the second time binary group flag is always set to zero.

The following table shows the differences between SMPTE and EBU versions of the time and control code.

	SMPTE	EBU
T.V. Frame Rate	30 Hz	25 Hz
Code Bit Rate	2400 Hz	2000 Hz
Code Bit Period	416 µsec	500 µsec
Rise and Fall Times	25 µsec	50 µsec
Flag Bit 10	Drop Frame	Unassigned
Flag Bit 11	Colour Frame	Colour Frame
Flag Bit 27	Bi-phase parity	Binary Group 1
Flag Bit 43	Binary Group 1	Binary Group 2
Flag Bit 58	Unassigned	Bi-phase parity
Flag Bit 59	Binary Group 2	Unassigned

2. VERTICAL INTERVAL TIME CODE

VITC is a digital signal comprised of 90 bits of information, numbered 0 through 89 inclusive, which is recorded on two non-adjacent lines during the vertical blanking interval of each television field. The modulation method is such that each state of the signal corresponds to a binary state, and a transition occurs only when there is a change in the data contained in adjacent bit cells. This system, known as "non return to zero", (NRZ) is illustrated below
The nominal bit rate is 113.75 (116 for PAL) times the line frequency, resulting in a bit rate of 1.789 MHz for NTSC and 1.812 MHz for PAL. Each television frame is identified by a complete code word, which contains a "field mark bit" set in field 2 of each frame.

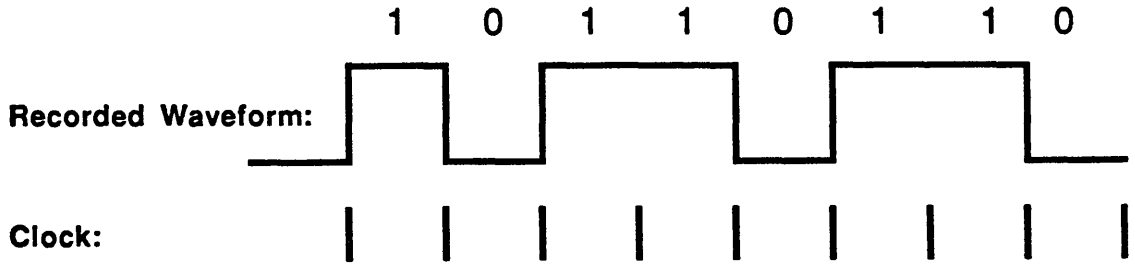
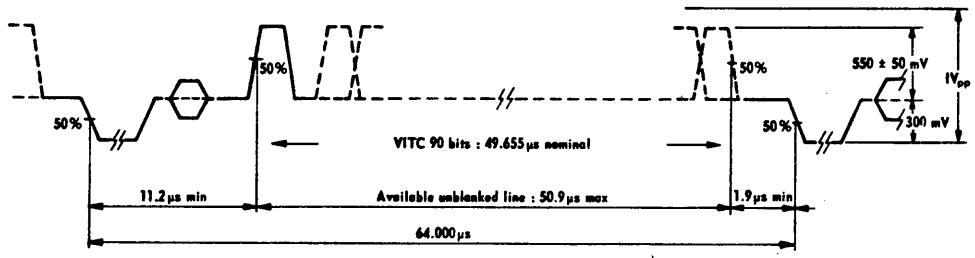
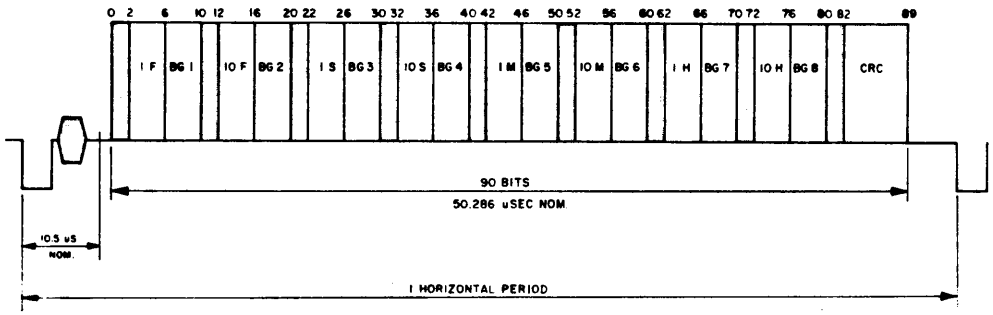


Figure I-2 Non Return to Zero Encoding Scheme



(a) EBU Specification



(b) SMPTE specification

Figure I-3 Position of VITC on the Line

The structure of the information is similar to the longitudinal time code with the following exceptions:

1. Nine sync bit pairs fixed as a "1" bit followed by a "0" bit are evenly spaced throughout the code to aid in the decoding process.

2. Eight bits are set aside at the end of the code word for error detection by means of cyclic redundancy checking. When the CRC is recalculated on recovery of the data, the result should be zero, if no errors are detected. The CRC also permits detection of bursts of errors such as can be encountered in magnetic recording.

3. The Bi-phase parity bit is used for field identification. The field mark is set to "1" during the second field of each television frame, and enables a VITC reader to identify odd and even numbered fields without reference to the field synchronizing signal.

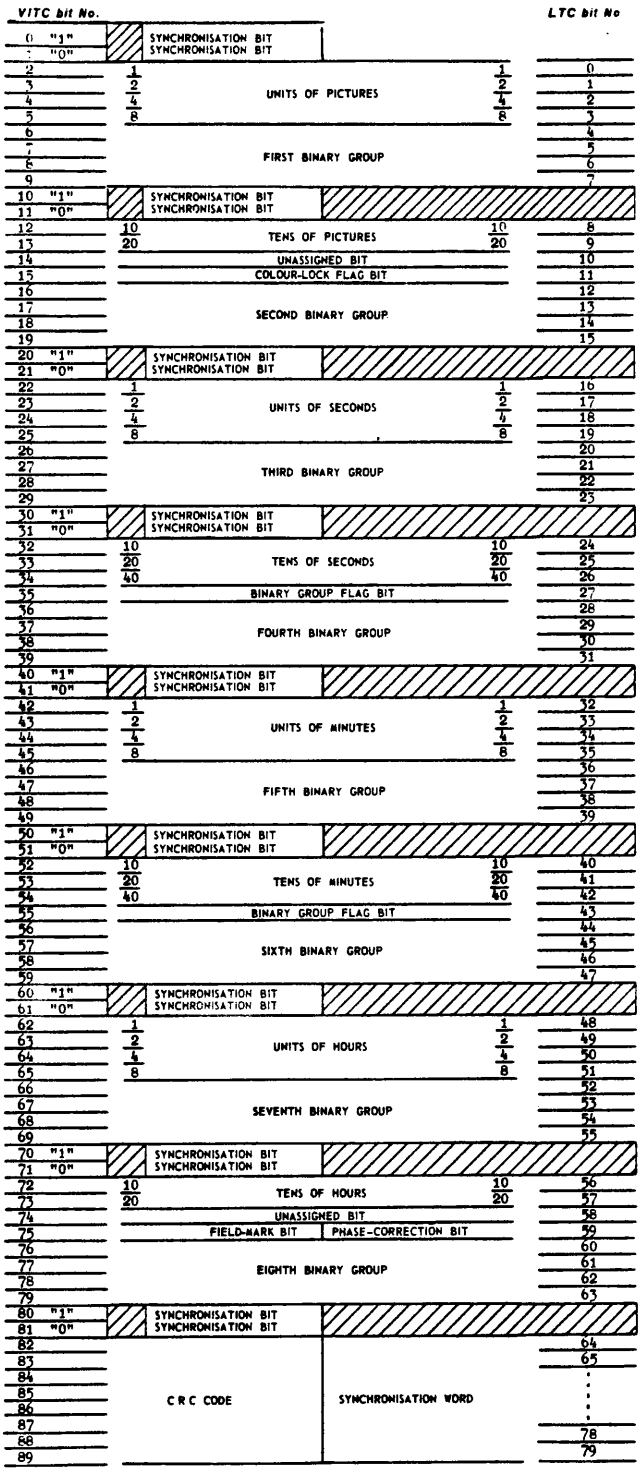


Figure I-4 Relationship between VITC and LTC (EBU)

APPENDIX B:

COLOUR FRAMING AND THE SMPTE/EBU CODE

DISCUSSION:

Operation of an editing system using SMPTE or EBU standard editing codes require a number of special parameters in the way the code is recorded, the operation and setup of the VTR's, and the way the editor is used. These parameters are listed below:

1. Synchronizing the time code to the video signal, as concerning field one/field two synchronization.

2. Synchronizing the time code to the video signal, as concerning 4-field (8-field PAL) colour framing.

3. The stability of the station sync generator to meet EIA RS-170-A (EBU PAL 8-field) specifications.

4. The setup of the VTR itself for proper 4-field (8-field PAL) colour identification and synchronization.

When all of the above parameters are met for use with direct, high band type VTR's, editing synchronization can be achieved.

1. Longitudinal SMPTE/EBU time code (LTC) is a digital reference code that is recorded along the length of an audio or cue track of a video tape. Each video frame is given a unique identifying number, which is formatted to include hours, minutes, seconds, and frames as well as other information.

   Vertical Interval Time Code (VITCode) is a digital reference signal recorded in the field blanking interval of the video signal. It identifies the video fields in addition to information in the LTC.

   Each frame is composed of two sequential fields of video called field 1 and field 2. Each of these two fields is uniquely identified and should always be sequential. SMPTE/EBU specifications call for LTC time code to start during the vertical serrations at the start of field one. The generator, therefore, must be connected to a stable synchronizing video or sync source, or the generated code will "free run" and will produce ambiguous identification of the video frames. Because VITCode is recorded on the program video, it always provides accurate field identification.

   In editing, if the recorded time code is not synchronized to the VTR video an "ABORT" may occur at the edit point. (The VTR's will be synchronized as pertaining to vertical sync, but the time codes would not.)

2. The NTSC television standard used a chroma subcarrier frequency of 3579545 Hz, of which 227.5 complete cycles fit into one horizontal line. With 525 horizontal lines in one frame, this produces

   227.5sc cycles/hor line x 525 hor lines/frame
   = 119,437.5 subcarrier cycles per frame.

   After one frame, there is an additional .5 subcarrier left over. In this manner, it takes 2 frames (4 fields) to return to a nonfractional subcarrier cycle count.

The PAL television standard uses a chroma subcarrier frequency of 4433618.75 Hz of which 283.7516 cycles fit into one horizontal line. With 625 horizontal lines in one frame, this produces

283.7516 cycles/hor line x 625 hor lines/frame
= 177,344.75 subcarrier cycles per frame.

Therefore, it takes 4 frames (8 fields) to return to a non-fractional subcarrier cycle count.

Before the development of time-base correction techniques, a part cycle displacement at the beginning of each field did not cause any problems. With time-base correcting, a sudden shift of a part cycle (as at an edit point for example) will cause a shift of the entire picture horizontally to match up the subcarrier cycles into proper sequence.

To eliminate such problems, most high band, direct-recording VTR's detect and synchronize the playback video with the incoming video so that the subcarrier cycles are matched. When this is done, a video edit will produce a proper sequence of the subcarrier. As discussed above, it requires 2 (4 PAL) frames of video before the proper sequence occurs. If two edit points (one for record VTR, one for source) are selected that do not maintain the proper colour sequence, the editing computer will attempt to synchronize the two VTR's to match an improper colour sequence. If the record VTR contains its own colour framing correction circuit, a conflict occurs: the record VTR will attempt to synchronize for proper colour sequence, and the edit controller will attempt to synchronize for proper selected edit point.

If the specific fields of the colour sequence are defined when the time code is recorded on all tapes used in an edit session, then edit points may be easily chosen which will observe the correct colour field sequence. It is imperative that such colour framed time code be used when editing with colour framing VTR's. A colour flag bit is set in the code to indicate colour frame address assignments.

The SMPTE specification regarding colour frame addresses states:

> "If colour field identification in the code is required, then the even units of frame numbers shall identify frame A and the odd units of frame numbers shall identify frame B as defined in EIA standard RS-170-A."

The EBU specification regarding colour frame addresses and the associated eight fields of the PAL video signal states:

"When the time code is displayed in decimal numbers, S and P designating the number of seconds and pictures respectively, then:

a) S+P is odd for fields 1 and 2 and fields 5 and 6
S+P is even for fields 3 and 4 and fields 7 and 8

b) The remainder after dividing S+P by 4 is:

0 for fields 7 and 8
1 for fields 1 and 2
2 for fields 3 and 4
3 for fields 5 and 6

3. Since the subcarrier to horizontal sync (Sc-H) relationship has become an important part of today's technology in video tape recording, new standards have been adopted which outline the 4 (8 PAL) colour fields and set up tighter specifications in subcarrier to horizontal sync (Sc-H) drift.

   For NTSC colour systems, colour field 1 is that field with positive going subcarrier zero-crossings most nearly coincident with the half-amplitude point of the leading edges of even numbered horizontal sync pulses. The tolerance in this coincidence is +/- 40° of reference subcarrier. (See Figure II-2)

   For PAL colour systems, the Sc-H phase is defined as the phase of the Eu component of the colour burst extrapolated to the half amplitude point of the leading edge of the synchronizing pulse of line 1 of field #1. Colour field 1 of the 8 field sequence is defined as that field where the preferred Sc-H phase is 0°. For maximum protection against picture disturbances at edit points, the EBU recommends Sc-H values 0 +/- 20° for colour field 1. (See Figure II-1)

4. On many of the 1" VTR's presently in use, the colour frame identification is switched on or off when the tape is first recorded. A special colour frame pulse is recorded on the control track to identify a special colour field (15 Hz NTSC, 6.25 Hz PAL). When the full colour frame mode is used, all of the above parameters must be met, in order for a proper edit sequence of the colour fields. It should be understood that although the VTR itself is capable of synchronizing to full colour field synchronization, the sync source must be capable of meeting the new Sc-H specifications. (A portable camera used in a remote location may not meet this spec.)

   With all the aforementioned variables met, proper colour field editing and edit control synchronization can be achieved with minimal problems. It can be concluded that time code edit synchronization can be achieved by:

   1. Proper recording of time code and video synchronized to a sync generator using new Sc-H tolerances.

   2. Using a time code generator capable of synchronizing to the 4-field (8-field PAL) colour sequence.

   3. Proper set up of all VTR's and TBC's for correct colour sequencing.

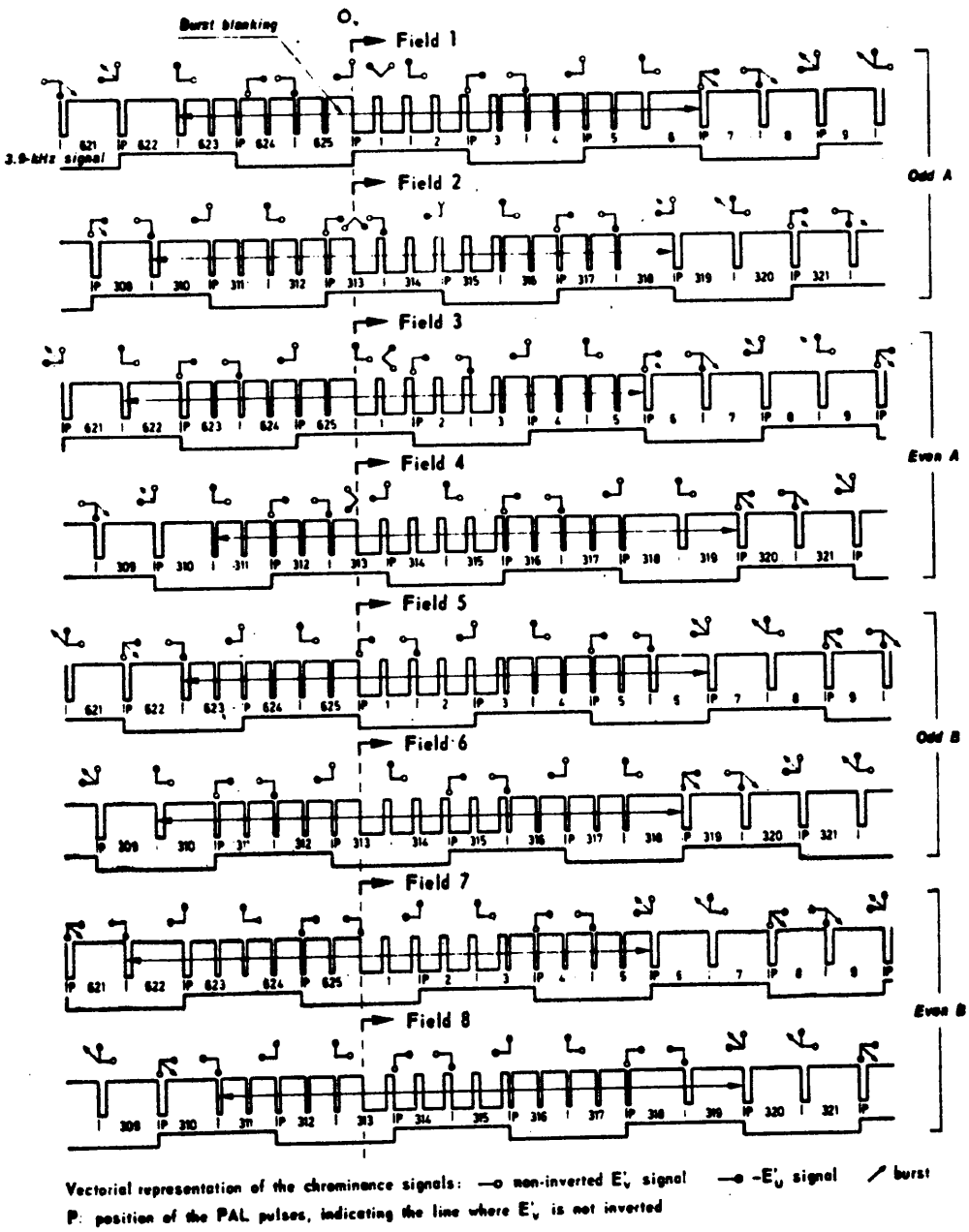


Figure II-1-The Eight-Field-Sequence of the PAL System

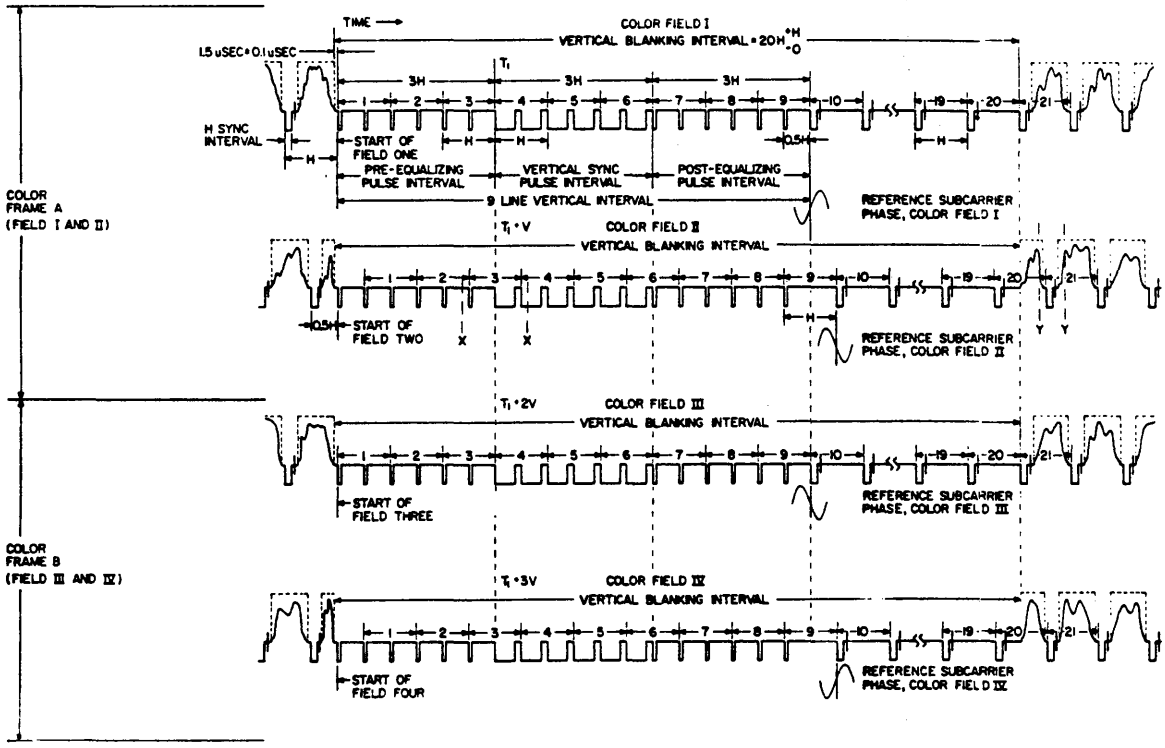


Figure II-2 - RS-170-A Synchronizing Waveforms

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APPENDIX C:

ASCII CODE LIST

CHAR	DEC	HEX	CHAR	DEC	HEX	CHAR	DEC	HEX
CTL-@ (NUL)	0	00	SPACE	32	20	@	64	40
CTL-A (SOH)	1	01	!	33	21	A	65	41
CTL-B (STX)	2	02	"	34	22	B	66	42
CTL-C (ETX)	3	03	#	35	23	C	67	43
CTL-D (EOT)	4	04	$	36	24	D	68	44
CTL-E (ENQ)	5	05	%	37	25	E	69	45
CTL-F (ACK)	6	06	&	38	26	F	70	46
CTL-G (BEL)	7	07	'	39	27	G	71	47
CTL-H (BS)	8	08	(	40	28	H	72	48
CTL-I (HT)	9	09	)	41	29	I	73	49
CTL-J (LF)	10	0A	*	42	2A	J	74	4A
CTL-K (VT)	11	0B	+	43	2B	K	75	4B
CTL-L (FF)	12	0C	,	44	2C	L	76	4C
CTL-M (CR)	13	0D	-	45	2D	M	77	4D
CTL-N (SO)	14	0E	.	46	2E	N	78	4E
CTL-O (SI)	15	0F	/	47	2F	O	79	4F
CTL-P (DLE)	16	10	0	48	30	P	80	50
CTL-Q (DC1)	17	11	1	49	31	Q	81	51
CTL-R (DC2)	18	12	2	50	32	R	82	52
CTL-S (DC3)	19	13	3	51	33	S	83	53
CTL-T (DC4)	20	14	4	52	34	T	84	54
CTL-U (NAK)	21	15	5	53	35	U	85	55
CTL-V (SYN)	22	16	6	54	36	V	86	56
CTL-W (ETB)	23	17	7	55	37	W	87	57
CTL-X (CAN)	24	18	8	56	38	X	88	58
CTL-Y (EM)	25	19	9	57	39	Y	89	59
CTL-Z (SUB)	26	1A	:	58	3A	Z	90	5A
CTL-[(ESC)	27	1B	;	59	3B	[	91	5B
CTL-\ (FS)	28	1C	<	60	3C	\	92	5C
CTL-] (GS)	29	1D	=	61	3D	]	93	5D
CTL-^ (RS)	30	1E	>	62	3E	^	94	5E
CTL-_ (US)	31	1F	?	63	3F	_	95	5F

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APPENDIX D:

SUMMARY OF REMOTE CONTROL COMMANDS

REMOTE COMMAND	KEY STROKE	DECIMAL	COMMAND DATA FORMAT
Set Gen Source	<space>	32	1=Free Run, 2=Jam, 3=Momentary Jam
Set UB Source	!	33	0=Numeric, 1=Rdr UB, 2=Rdr Time
Set Gen Mode	"	34	1 char - see Fig IV-1
Set Gen Time	(	40	8 char 'HHMMSSFF'
Set Gen UB	)	41	8 char binary group 8 first
Gen Alpha TEXT	,	44	
Gen Alpha CAPT	.	46	

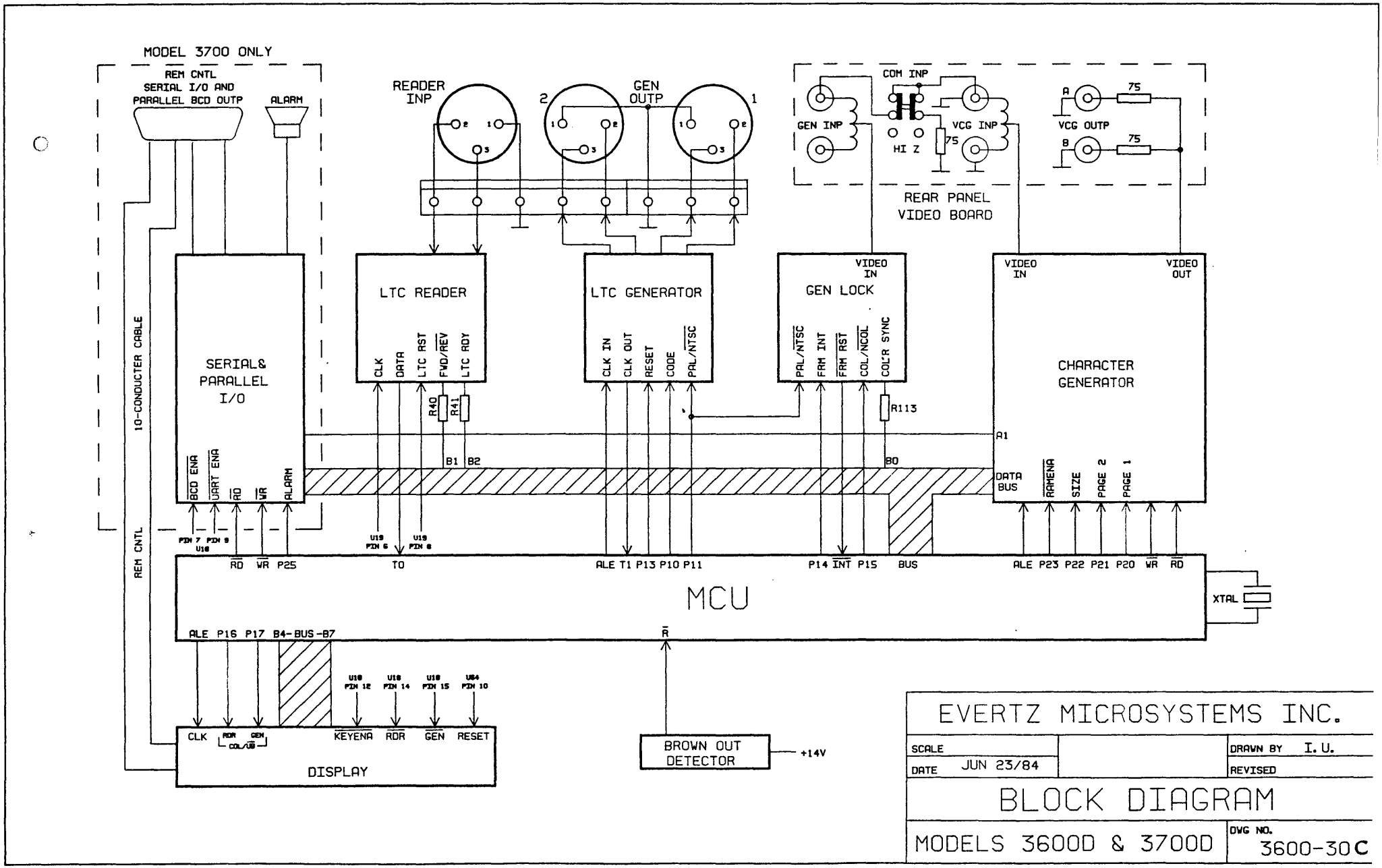
REMOTE COMMAND	KEY STROKE	DECIMAL	RESPONSE DATA FORMAT
Read Gen Source	0	48	1=Free Run, 2=Jam
Read UB Source	1	49	0=Numeric, 1=Rdr UB, 2=Rdr Time
Read Gen Status	2	50	See Fig IV-2
Read Gen Time	8	56	8 char 'HHMMSSFF'
Read Gen UB	9	57	8 char binary group 8 first
Read Rdr Status	B	66	See Fig IV-2
Read Rdr Time	H	72	8 char 'HHMMSSFF'
Read Rdr UB	I	73	8 char binary group 8 first
Read Alpha UB	L	75	Alpha-numeric text dump of VCG screen

ASCII	DECIMAL VALUE	DEFAULT	PARITY	COLOUR FRAME	DROP FRAME
@	64	Off	Off	Off	Off
A	65	Off	Off	Off	On
B	66	Off	Off	On	Off
C	67	Off	Off	On	On
P	80	Off	On	Off	Off
Q	81	Off	On	Off	On
R	82	Off	On	On	Off
S	83	Off	On	On	On
a	97	On	As per switch settings		

Figure IV-1 Set Generator Mode Commands

ASCII	DECIMAL VALUE	PARITY	BINARY GROUP 2	BINARY GROUP 1	COLOUR FRAME	DROP FRAME
@	64	Off	Off	Off	Off	Off
A	65	Off	Off	Off	Off	On
B	66	Off	Off	Off	On	Off
C	67	Off	Off	Off	On	On
D	68	Off	Off	On	Off	Off
E	69	Off	Off	On	Off	On
F	70	Off	Off	On	On	Off
G	71	Off	Off	On	On	On
H	72	Off	On	Off	Off	Off
I	73	Off	On	Off	Off	On
J	74	Off	On	Off	On	Off
K	75	Off	On	Off	On	On
L	76	Off	On	On	Off	Off
M	77	Off	On	On	Off	On
N	78	Off	On	On	On	Off
O	79	Off	On	On	On	On
P	80	On	Off	Off	Off	Off
Q	81	On	Off	Off	Off	On
R	82	On	Off	Off	On	Off
S	83	On	Off	Off	On	On
T	84	On	Off	On	Off	Off
U	85	On	Off	On	Off	On
V	86	On	Off	On	On	Off
W	87	On	Off	On	On	On
X	88	On	On	Off	Off	Off
Y	89	On	On	Off	Off	On
Z	90	On	On	Off	On	Off
[	91	On	On	Off	On	On
\	92	On	On	On	Off	Off
]	93	On	On	On	Off	On
^	94	On	On	On	On	Off
_	95	On	On	On	On	On

Figure IV-2 Read Status Responses



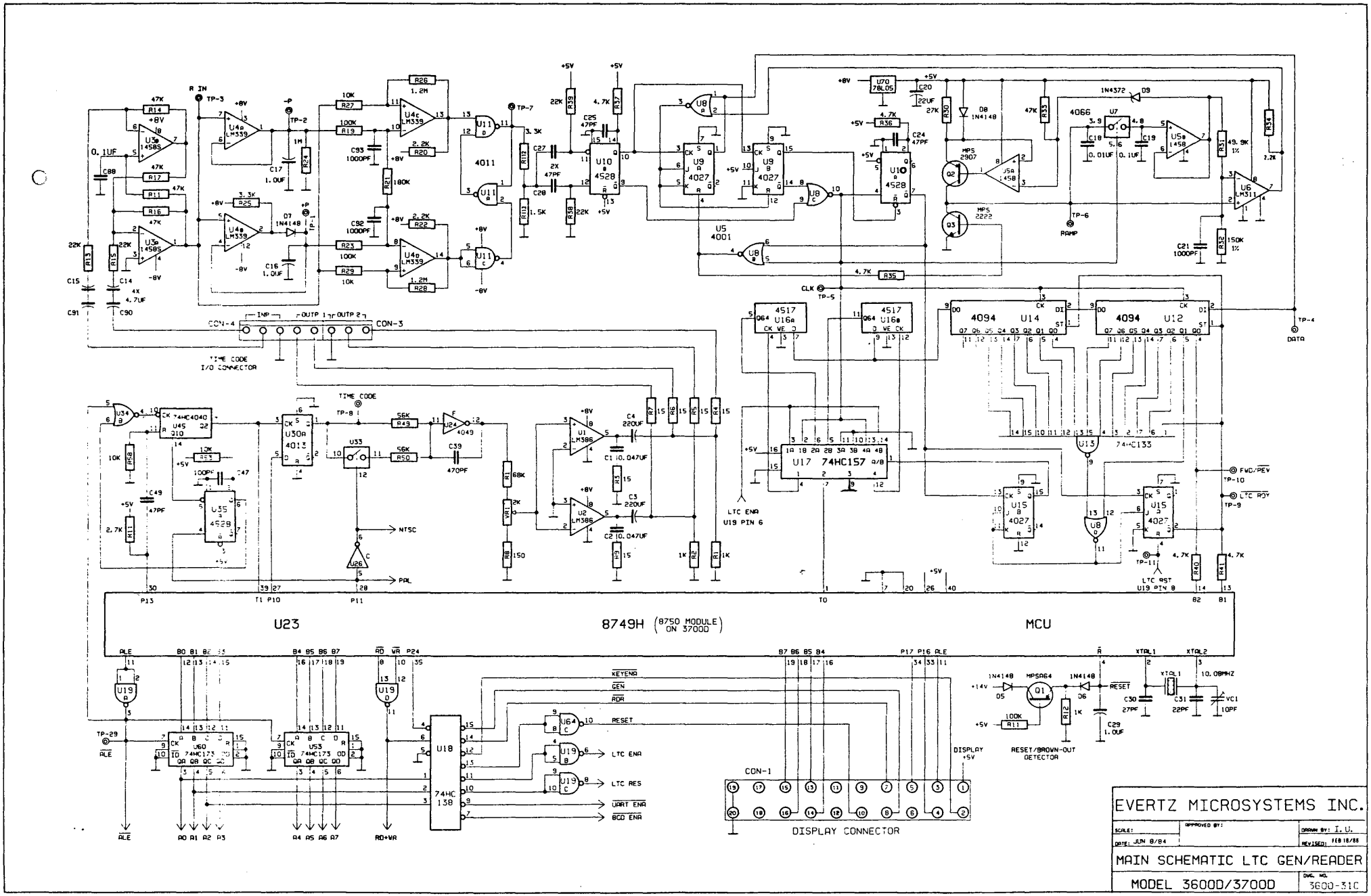
EVERTZ MICROSYSTEMS INC.

SCALE		DRAWN BY I. U.
DATE JUN 23/84		REVISED

BLOCK DIAGRAM

MODELS 3600D & 3700D

DWG NO. 3600-30C

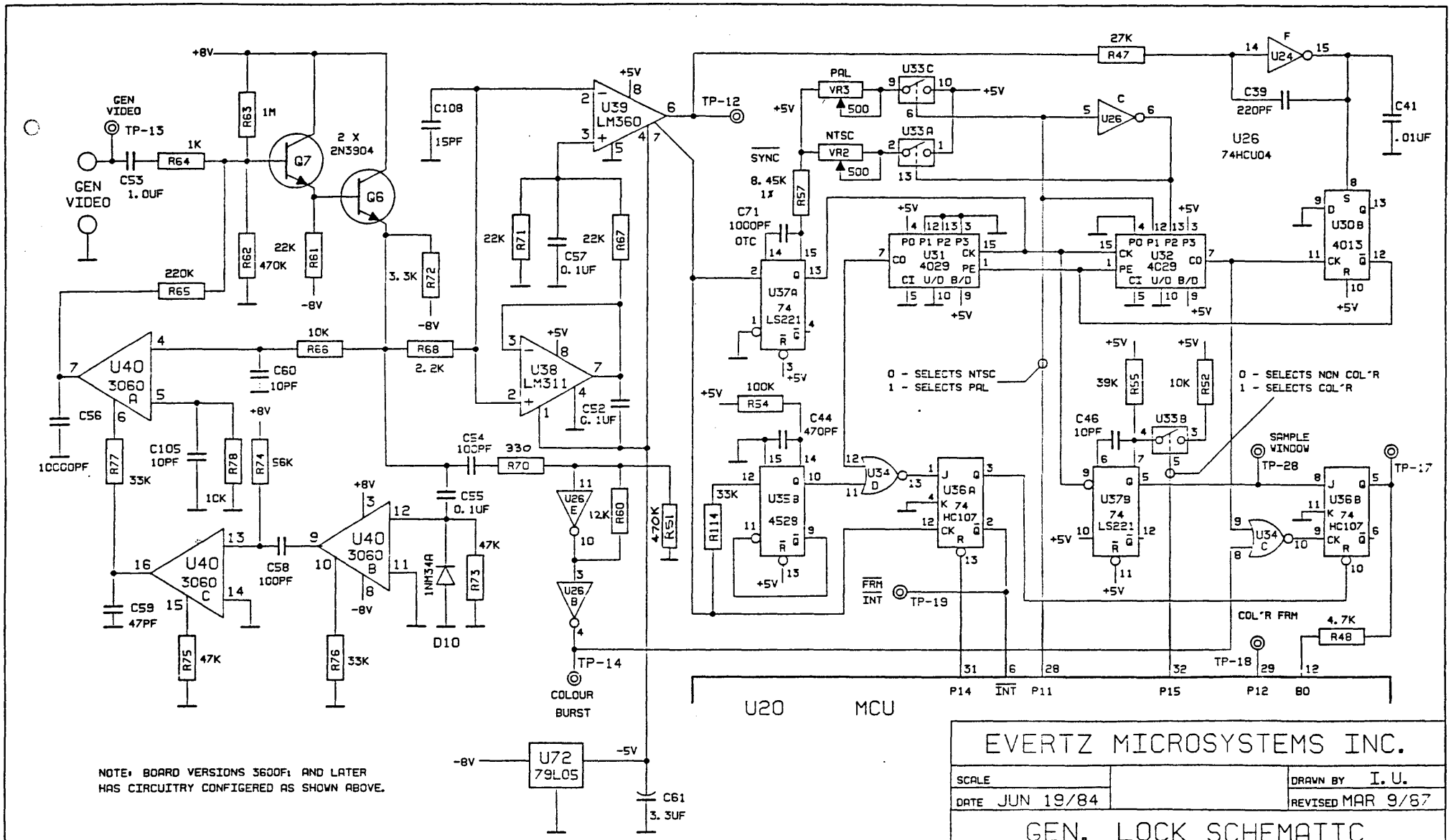


EVERTZ MICROSYSTEMS INC.

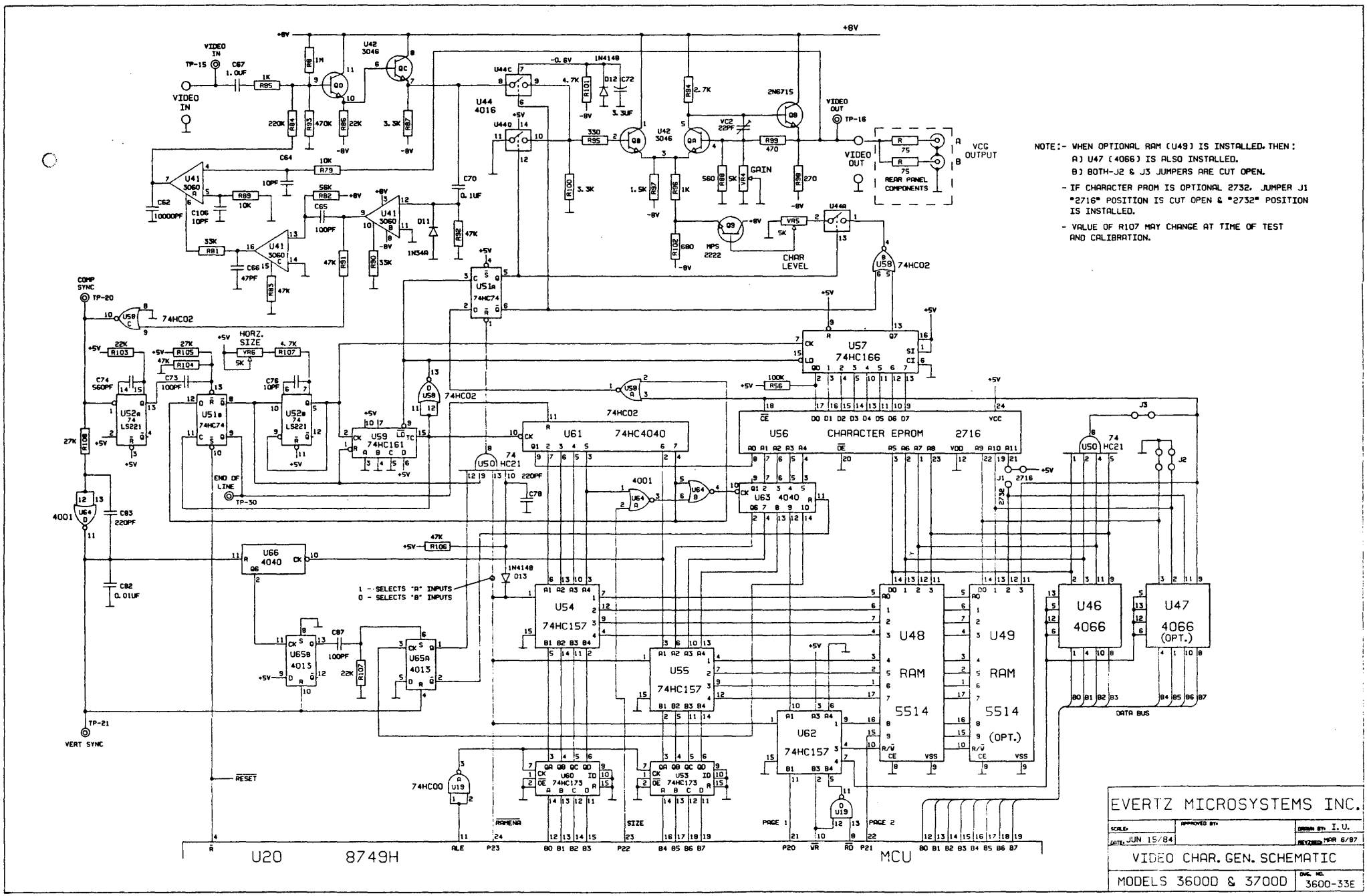
SCALE:	APPROVED BY:	DRAWN BY: I. U.
DATE: JUN 8/84		REVISED: FEB 16/88

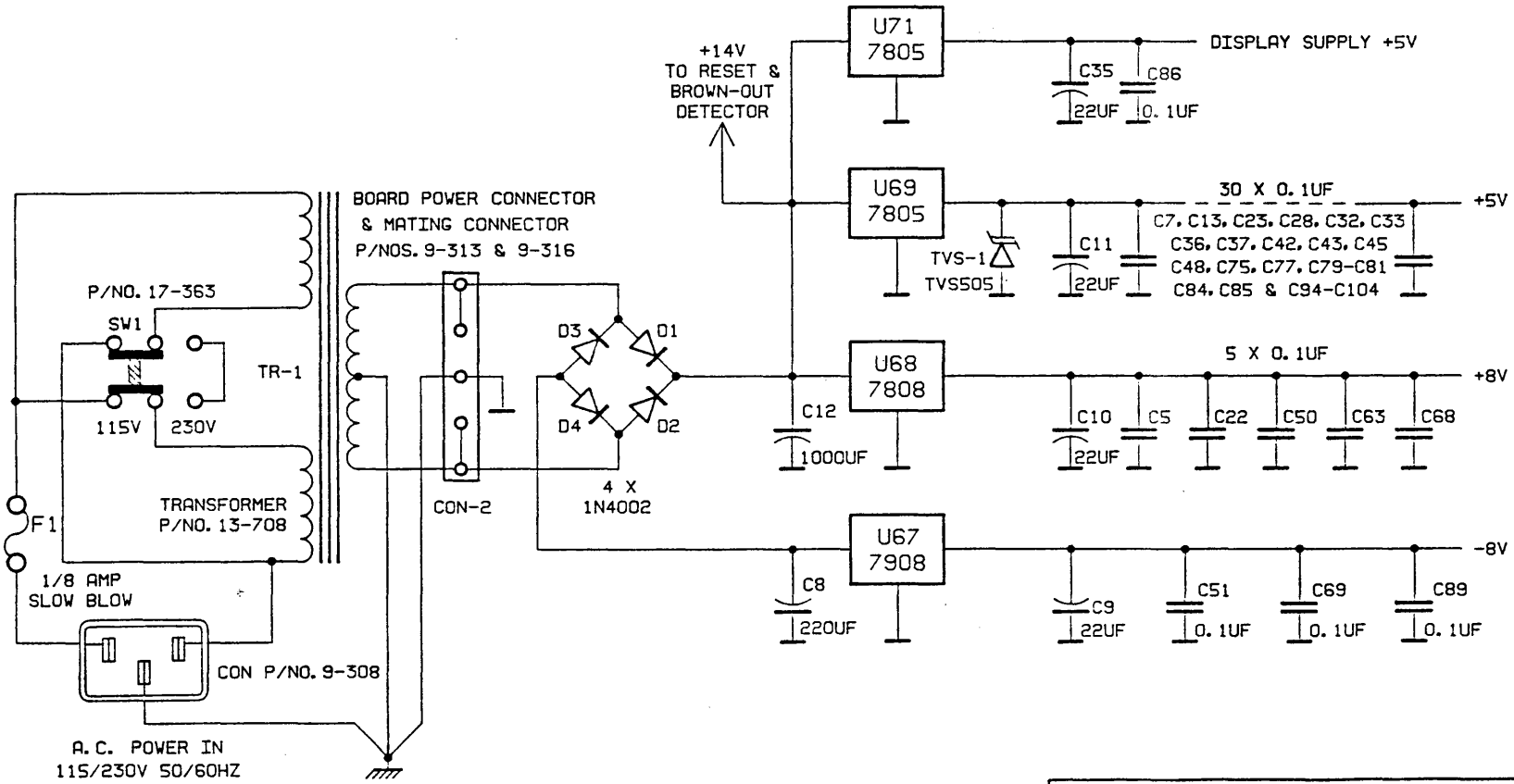
MAIN SCHEMATIC LTC GEN/READER

MODEL 3600D/3700D — DWG. NO. 3600-31C

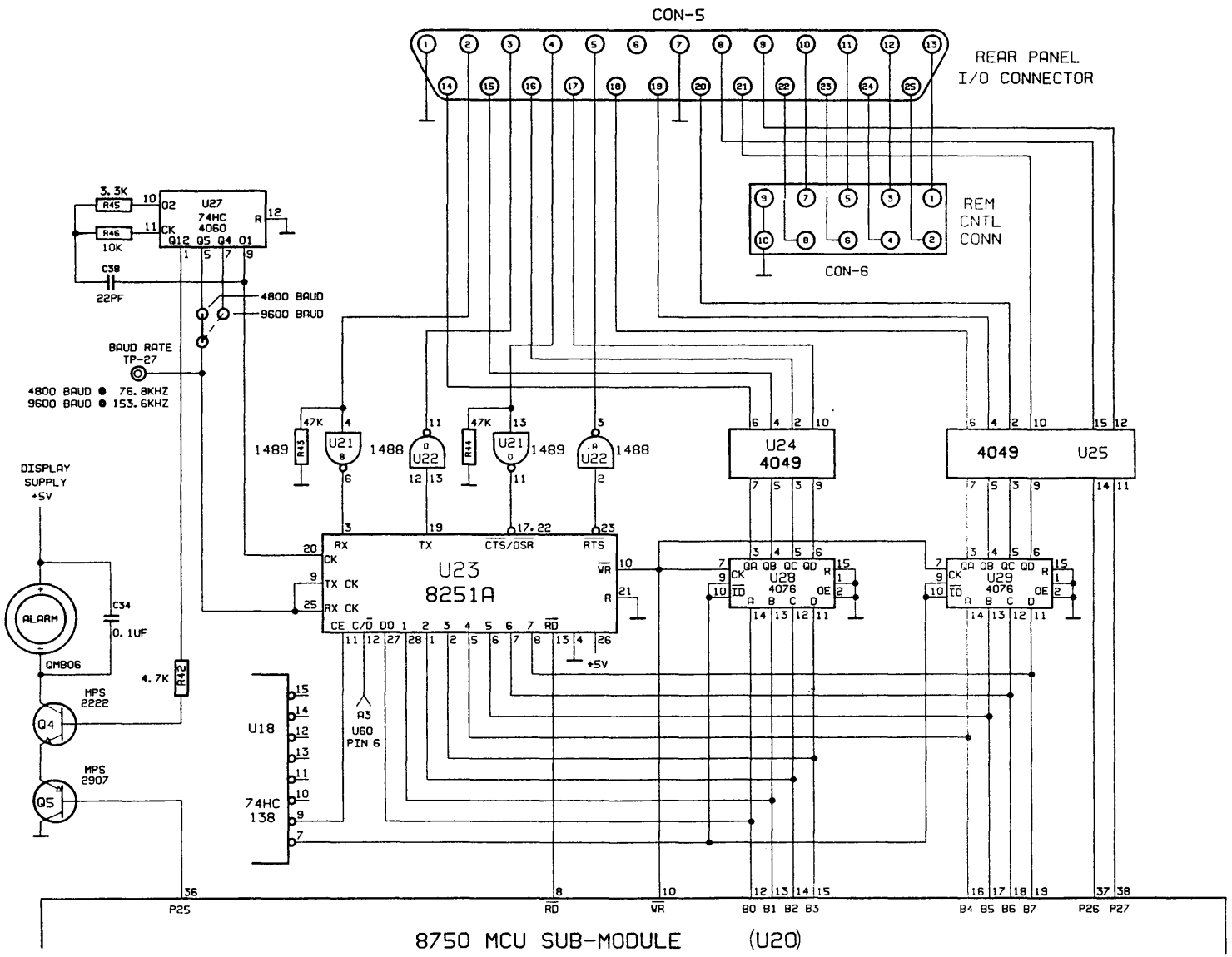


EVERTZ MICROSYSTEMS INC.	
SCALE	DRAWN BY I. U.
DATE JUN 19/84	REVISED MAR 9/87
GEN. LOCK SCHEMATIC	
MODELS 3600D & 3700D	DWG NO. 3600-32F


NOTE:- WHEN OPTIONAL RAM (U49) IS INSTALLED. THEN :
A) U47 (4066) IS ALSO INSTALLED.
B) BOTH-J2 & J3 JUMPERS ARE CUT OPEN.
- IF CHARACTER PROM IS OPTIONAL 2732. JUMPER J1 "2716" POSITION IS CUT OPEN & "2732" POSITION IS INSTALLED.
- VALUE OF R107 MAY CHANGE AT TIME OF TEST AND CALIBRATION.
VIDEO IN
VIDEO OUT
VCG OUTPUT
REAR PANEL COMPONENTS
GAIN
CHAR LEVEL
HORZ. SIZE
COMP SYNC
VERT SYNC
END OF LINE
1 - SELECTS "A" INPUTS
0 - SELECTS "B" INPUTS
CHARACTER EPROM 2716
RAM 5514
(OPT.)
DATA BUS
U20 8749H
MCU
EVERTZ MICROSYSTEMS INC.
VIDEO CHAR. GEN. SCHEMATIC
MODELS 3600D & 3700D
3600-33E
DRAWN BY: I. U.
DATE: JUN 15/84
REVISED: MAR 6/87

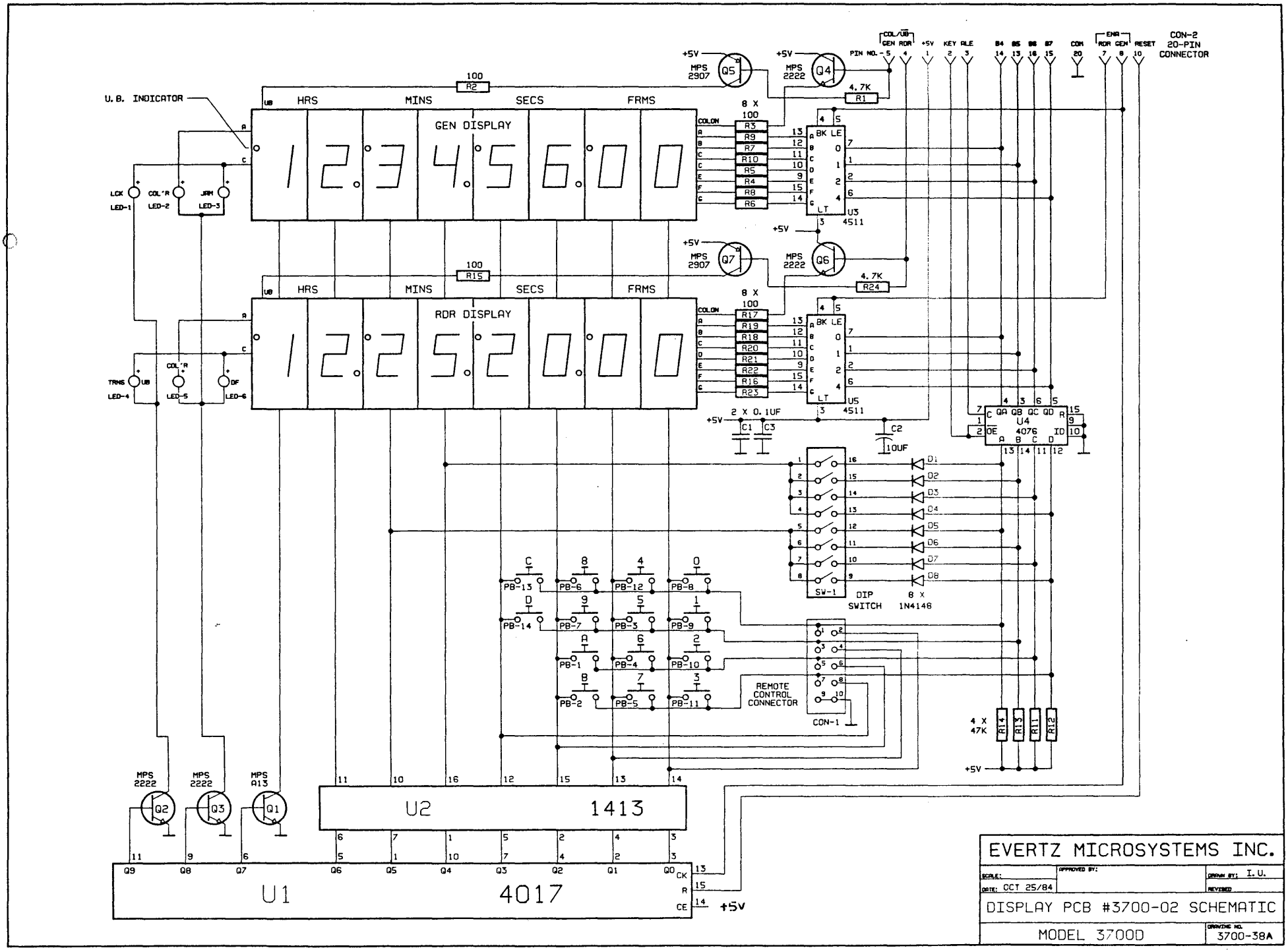


EVERTZ MICROSYSTEMS INC.		
SCALE		DRAWN BY I.U.
DATE JUN 18/84		REVISED
POWER SUPPLY		
MODELS 3600D & 3700D		DWG NO. 3600-34C



8750 MCU SUB-MODULE (U20)

EVERTZ MICROSYSTEMS INC.		
SCALE:	APPROVED BY:	DRAWN BY: I. U.
DATE: OCT 23/84		REVISED
SERIAL/PARALLEL I/O SCHEMATIC		
MODEL 3700D		DRAWING NO. 3600-36C



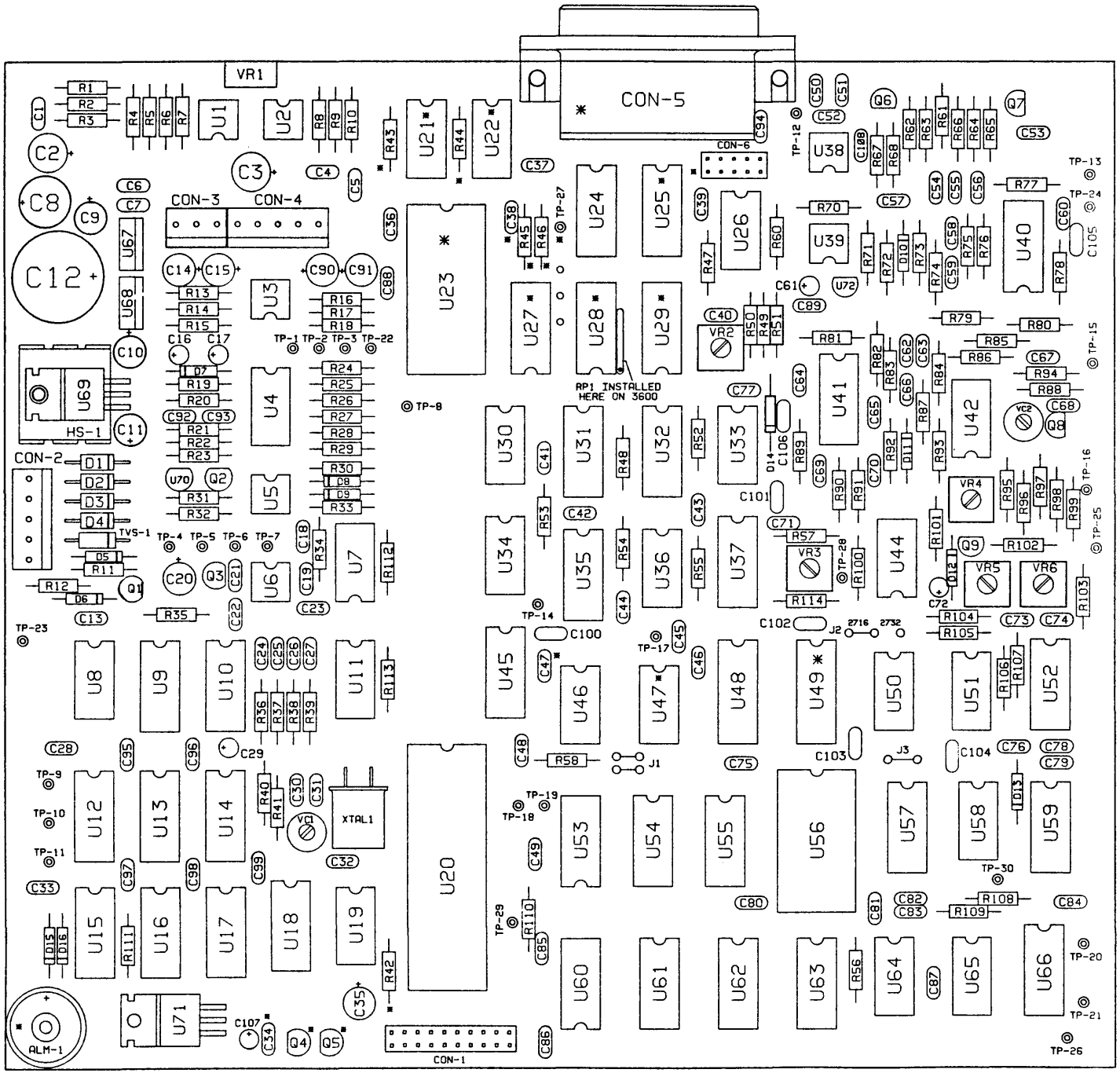
EVERTZ MICROSYSTEMS INC.

SCALE:	APPROVED BY:	DRAWN BY: I. U.
DATE: OCT 25/84		REVISED

DISPLAY PCB #3700-02 SCHEMATIC

MODEL 3700D

DRAWING NO. 3700-38A



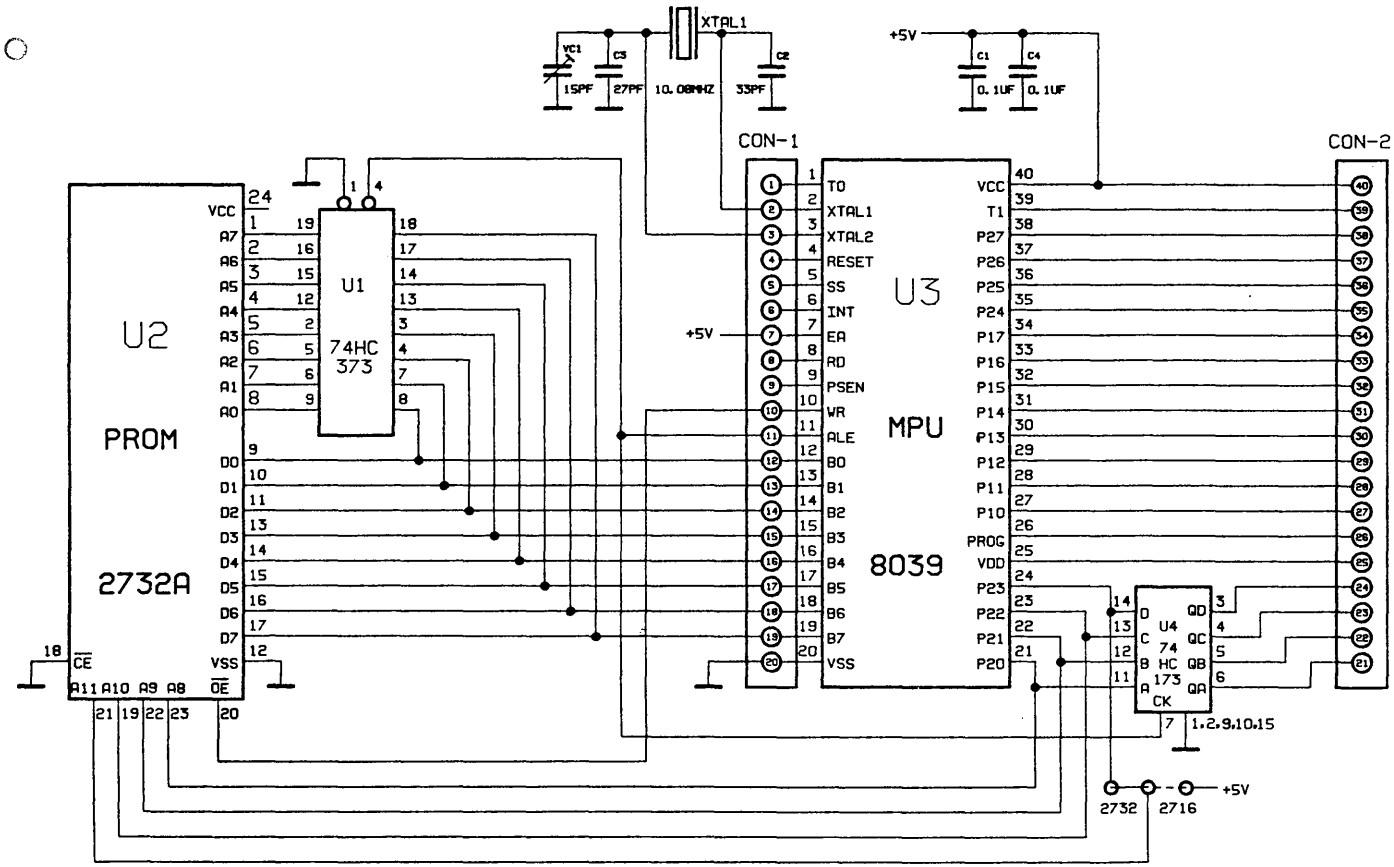
NOTE: ON MODEL 3700D
- OPTINAL PARTS (*) ARE INCLUDED.
- U20 IS REPLACED WITH SUBMODULE #8750.
- C30, C31, VC1 & XTAL-1 ARE OMITTED.
- J1 & J3 ARE CUT OPEN.

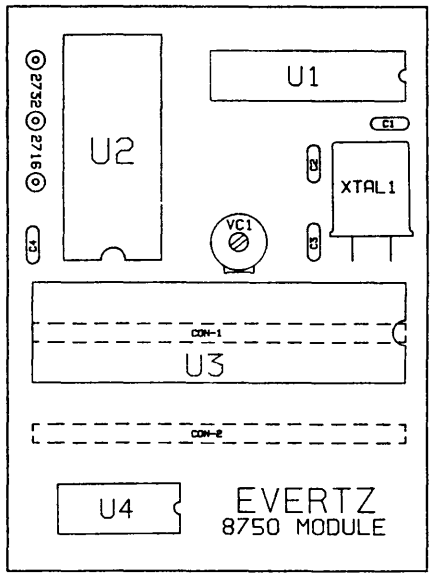
EVERTZ MICROSYSTEMS INC.

DATE: MAY 31/84	APPROVED BY:	DRAWN BY:	I. U.
REV DATE: MAR 9/87		REV BY:	I. U.

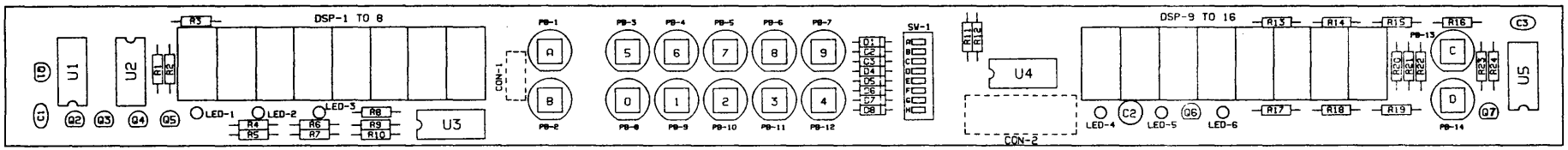
COMPONENT LAYOUT

MODELS 3600D/3700D — DRAWING NO. 3600-80G





EVERTZ MICROSYSTEMS INC.		
SCALE		DRAWN BY I. U.
DATE OCT 26/84		REVISED
MCU MODULE #8750	SCHEMATIC AND COMPONENT LAYOUT	
		DWG NO. 8750-31



EVERTZ MICROSYSTEMS INC.

SCALE:	APPROVED BY:	DRAWN BY: I. U.
DATE: OCT 29/84		REVISED

DISPLAY/KEYPAD COMP. LAYOUT

MODEL 3700D — DRAWING NO. 3700-81A

Options: 1 : 2
========

ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
OPT. 1- MODEL 3600D							
OPT. 2- MODEL 3700D							
MAIN PC BOARD							
1	Int. Circuit	1-89	AUDIO AMPLIFIER	LM386 N-1	NSC Only	2	U1,U2
2	Int. Circuit	1-627	HIGH SLEW DUAL AMP	MC1458 SP1	MOT Only	1	U3
3	Int. Circuit	1-625	QUAD VOLT COMPARATOR	LM339	NSC Only	1	U4
4	Int. Circuit	1-90	OPERATIONAL AMP	LM1458	NSC Only	1	U5
5	Int. Circuit	1-87	VOLTAGE COMPARATOR	LM311	NSC Only	2	U6,U38
6	Int. Circuit	1-26	QUAD ANALOG SWITCH	4066	SSS Only	3	U7,U33,U46
7	Int. Circuit	1-628	QUAD 2-INPUT NOR	4001-F	SSS Only	2	U8,U64
8	Int. Circuit	1-946	DUAL MONOSTABLE	4528	SSS ONLY	1	U10
9	Int. Circuit	1-14	DUAL J-K FLIP-FLOP	4027		2	U9,U15
10	Int. Circuit	1-4	QUAD 2-INPUT NAND	4011	NSC Only	1	U11
11	Int. Circuit	1-33	8-STAGE S/R	MC14094	MOT/SSS Only	2	U12,U14
12	Int. Circuit	1-654	13-INPUT NAND	74HC133		1	U13
13	Int. Circuit	1-596	DUAL 64-BIT STAT S/R	4517	SSS	1	U16
14	Int. Circuit	1-656	QUAD 2-INPUT SWITCH	74HC157		4	U17,U54,U55,U62
15	Int. Circuit	1-660	1 OF 8 DECODER	74HC138		1	U18
16	Int. Circuit	1-664	QUAD 2-INPUT NAND	74HC00		1	U19
17	Int. Circuit	1-500	MICRO CONTROLLER	D8749H	Intel/NEC	1	U20 (OPT 1)
18	Int. Circuit	1-85	QUAD RS-232 LINE REC	1489		1	U21 (OPT 2)
19	Int. Circuit	1-84	QUAD RS-232 LINE DR	1488		1	U22 (OPT 2)
20	Int. Circuit	1-529	USART	8251A	Intel	1	U23 (OPT 2)
21	Int. Circuit	1-22	HEX INVERT BUFFER	4049		1	U24
22	Int. Circuit	1-22	HEX INVERT BUFFER	4049		1	U25 (OPT 2)
23	Int. Circuit	1-676	HEX UNBUFFERED INV	74HCU04	Mot ONLY	1	U26
24	Int. Circuit	1-733	14 STAGE CNTR OSC	74HC4060	T.I.Only	1	U27 (OPT 2)
25	Int. Circuit	1-665	QUAD D REGISTER	74HC173		2	U28,U29 (OPT 2)
26	Int. Circuit	1-5	DUAL D FLIP-FLOP	4013	NSC Only	2	U30,U65
27	Int. Circuit	1-16	BIN/DEC UP/DN CNTR	4029	FSS/SSS Only	2	U31,U32
28	Int. Circuit	1-658	QUAD 2-INPUT NOR	74HC02		2	U34,U58
29	Int. Circuit	1-44	DUAL MONOSTABLE	14528	MOT Only	1	U35
30	Int. Circuit	1-651	DUAL J-K FLIP-FLOP	74HC107		1	U36
31	Int. Circuit	1-80	DUAL MONOSTABLE	74LS221	T.I.	2	U37,U52
32	Int. Circuit	1-88	HIGH SPD COMPARATOR	LM360	NSC Only	1	U39
33	Int. Circuit	1-674	TRIPLE TRANSCOND AMP	CA3060E	RCA	2	U40,U41
34	Int. Circuit	1-92	5 NPN TRANS ARRAY	LM3046N	NSC Only	1	U42
35	Int. Circuit	1-8	QUAD ANALOG SWITCH	4016	SSS ONLY	1	U44
36	Int. Circuit	1-678	14 STAGE COUNTER	74HC4040		2	U45,U61
37	Int. Circuit	1-26	QUAD ANALOG SWITCH	4066	SSS Only	1	U47 (OPT 2)
38	Int. Circuit	1-106	1K x 4 CMOS RAM	LH2114L-20	Sharp	1	U48
39	Int. Circuit	1-106	1K x 4 CMOS RAM	LH2114L-20	Sharp	1	U49 (OPT 2)
40	Int. Circuit	1-734	DUAL 4 INPUT AND	74HC21		1	U50
41	Int. Circuit	1-659	DUAL D FLIP FLOP	74HC74		1	U51
42	Int. Circuit	1-665	QUAD D REGISTER	74HC173		2	U53,U60
43	Int. Circuit	1-617	4K x 8 EPROM	2732A-2		1	U56
44	Int. Circuit	1-735	8 BIT S/R	74HC166		1	U57

ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
45	Int. Circuit	1-657	4-BIT BIN COUNTER	74HC161		1	U59
46	Int. Circuit	1-19	12-BIT BIN CNTR	4040		2	U63,U66
47	Regulator	7-701	-8V 1A	MC7908CT	Motorola	1	U67
48	Regulator	7-700	+8V 1A	MC7808CT	Motorola	1	U68
49	Regulator	7-265	+5V 1A	7805 CT		2	U69,U71
50	Regulator	7-634	+5V 100mA	MC78L05ACP	Motorola	1	U70
51	Regulator	7-618	-5V 100mA	79L05 CP		1	U72
52	Transistor	8-271		MPS A64	Motorola	1	Q1
53	Transistor	8-276		MPS 2907	Motorola	1	Q2
54	Transistor	8-275		MPS 2222	MOT Only	2	Q3,Q9
55	Transistor	8-275		MPS 2222	MOT Only	1	Q4 (OPT 2)
56	Transistor	8-276		MPS 2907	Motorola	1	Q5 (OPT 2)
57	Transistor	8-280		2N3904		2	Q6,Q7
58	Transistor	8-282		2N6715	NSC/MOT	1	Q8
59	Diode	6-254	RECTIFIER	1N4002		4	D1-D4
60	Diode	6-255	SMALL SIGN. DIODE	1N4148		8	D5-D8,D12,D13,D15, D16
61	Diode	6-586	3V ZENER	1N4372	MOT Only	1	D9
62	Diode	6-253	GERMANIUM	1N34A		2	D10,D11
63	Diode	6-257	VOLTAGE SUPPRESSOR	TVS505	Unitrode	1	TVS1
64	Resistor	4-185	1/4W 5%	1K 1/4W 5%	Philips	6	R1,R2,R12,R84,R85, R96
65	Resistor	4-161	1/4W 5%	15 OHM	Philips	6	R3-R7,R9
66	Resistor	4-174	1/4W 5%	150 OHM	Philips	1	R8
67	Resistor	4-209	1/4W 5%	68K 1/4W 5%	Philips	1	R10
68	Resistor	4-211	1/4W 5%	100K 1/4W 5%	Philips	4	R11,R19,R23,R56
69	Resistor	4-203	1/4W 5%	22K 1/4W 5%	Philips	10	R13,R15,R36,R39,R61, R67,R71,R86,R103, R109
70	Resistor	4-207	1/4W 5%	47K 1/4W 5%	Philips	12	R14,R16-R18,R22,R73, R75,R83,R91,R92, R104,R106
71	Resistor	4-191	1/4W 5%	2.2K 1/4W 5%	Philips	4	R20,R22,R34,R66
72	Resistor	4-213	1/4W 5%	180K 1/4W 5%	Philips	1	R21
73	Resistor	4-222	1/4W 5%	1M 1/4W 5%	Philips	3	R24,R63,R80
74	Resistor	4-193	1/4W 5%	3.3K 1/4W 5%	Philips	5	R25,R72,R87,R100, R113
75	Resistor	4-223	1/4W 5%	1.2M 1/4W 5%	Philips	2	R26,R28
76	Resistor	4-199	1/4W 5%	10K 1/4W 5%	Philips	9	R27,R29,R52,R53,R58, R66,R78,R79,R89
77	Resistor	4-501	1/4W 1%	49.9K 1/4W 1%	Philips	1	R31
78	Resistor	4-514	1/4W 1%	150K 1/4W 1%	Philips	1	R32
79	Resistor	4-195	1/4W 5%	4.7K 1/4W 5%	Philips	9	R35-R37,R40,R41,R48, R101,R107,R111
80	Resistor	4-195	1/4W 5%	4.7K 1/4W 5%	Philips	1	R42 (OPT 2)
81	Resistor	4-207	1/4W 5%	47K 1/4W 5%	Philips	2	R43,R44 (OPT 2)
82	Resistor	4-199	1/4W 5%	10K 1/4W 5%	Philips	1	R46 (OPT 2)
83	Resistor	4-204	1/4W 5%	27K 1/4W 5%	Philips	4	R30,R47,R105,R108
84	Resistor	4-208	1/4W 5%	56K 1/4W 5%	Philips	4	R49,R50,R74,R82

Options: 1 : 2
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ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
85	Resistor	4-218	1/4W 5%	470K 1/4W 5%	Philips	3	R51,R62,R93
86	Resistor	4-212	1/4W 5%	120K 1/4W 5%	Philips	1	R54
87	Resistor	4-206	1/4W 5%	39K 1/4W 5%	Philips	1	R55
88	Resistor	4-240	1/4W 1%	8.45K 1/4W 1%	Philips	1	R57
89	Resistor	4-200	1/4W 5%	12K 1/4W 5%	Philips	1	R60
90	Resistor	4-214	1/4W 5%	220K 1/4W 5%	Philips	2	R65,R84
91	Resistor	4-178	1/4W 5%	330 OHM	Philips	2	R70,R95
92	Resistor	4-205	1/4W 5%	33K 1/4W 5%	Philips	5	R76,R77,R81,R90,R114
93	Resistor	4-181	1/4W 5%	560 OHM 1/4W 5%	Philips	1	R83
94	Resistor	4-192	1/4W 5%	2.7K 1/4W 5%	Philips	2	R94,R110
95	Resistor	4-188	1/4W 5%	1.5K 1/4W 5%	Philips	2	R97,R112
96	Resistor	4-177	1/4W 5%	270 OHM 1/4W 5%	Philips	1	R98
97	Resistor	4-180	1/4W 5%	470 OHM 1/4W 5%	Philips	1	R99
98	Resistor	4-182	1/4W 5%	680 OHM 1/4W 5%	Philips	1	R102
99	Resistor	4-731	5*47K COMMON SIP	4606X-101-473		1	RP1 (OPT 1)
100	Trim Pot	5-247	2K	3386W-1-202	Bourns	1	VR1
101	Trim Pot	5-244	500 OHM	3386F-1-501	Bourns	2	VR2,VR3
102	Trim Pot	5-248	5K	3386F-1-502	Bourns	3	VR4-VR6
103	Capacitor	2-502	.047uF 100V	SR211C473KAA		2	C1,C4
104	Capacitor	2-141	220uF 10V R	035-54221	Philips	2	C2,C3
105	Capacitor	2-129	.1uF 50V	SR215E104MAATR		27	C5-C7,C13,C18,C22, C23,C28,C32,C33,C36, C37,C42,C43,C45,C48, C50-C52,C54,C55,C57, C63,C68-C70,C75
106	Capacitor	2-129	.1uF 50V	SR215E104MAATR		20	(cont'd)C77,C79-C81, C84-C86,C88,C89, C94-C104
107	Capacitor	2-142	220uF 25V R	035-56221	Philips	1	C8
108	Capacitor	2-136	22uF 16V	TAP22M16F	ITT	4	C9,C10,C20,C35
109	Capacitor	2-138	22uF 40V	035-57229	Philips	1	C11
110	Capacitor	2-1194	1500uF 25V R	035-56152	Philips	1	C12
111	Capacitor	2-134	4.7uF 16V	T392B475M016AS	Kemet	4	C14,C15,C90,C91
112	Capacitor	2-131	1uF 25V	TAP1M35F	ITT	3	C16,C17,C29
113	Capacitor	2-128	.01uF 200V	SR215C103KAATR		3	C19,C41,C82
114	Capacitor	2-122	1000pF 63V	629-09102	Philips	3	C21,C92,C93
115	Capacitor	2-116	47pF 100V	681-58479	Philips	7	C24-C27,C49,C59,C66
116	Capacitor	2-112	27pF 100V	681-10279	Philips	1	C30 (OPT 1)
117	Capacitor	2-111	22pF 100V	681-10229	Philips	1	C31 (OPT 1)
118	Capacitor	2-129	.1uF 50V	SR215E104MAATR		1	C34 (OPT 2)
119	Capacitor	2-111	22pF 100V	681-10229	Philips	1	C38 (OPT 2)
120	Capacitor	2-117	220pF 100V	630-09221	Philips	3	C39,C78,C83
121	Capacitor	2-120	470pF 100V	630-09471	Philips	2	C40,C44
122	Capacitor	2-110	10pF 100V	681-10109	Philips	6	C46,C60,C64,C76, C105,C106
123	Capacitor	2-119	100pF 100V	681-10101	Philips	6	C47,C54,C58,C65,C73, C87
124	Capacitor	2-926	1uf 50v	SR305E105MAA		2	C53,C67
125	Capacitor	2-125	10000pF 63V	629-09103	Philips	2	C56,C62

Options: 1 : 2
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ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
126	Capacitor	2-133	3.3uF 16V	TAP3.3M16F	ITT	2	C61,C72
127	Capacitor	2-127	1000pF 200V	SR211A102JAA		1	C71
128	Capacitor	2-121	560pF 100V	630-09561	Philips	1	C74
129	Capacitor	2-130	.33uF 35V	TAP.33M35F	ITT	1	C107
130	Capacitor	2-729	15pF 100V	681-10159	Philips	1	C108
131	Trim Capac.	3-541	10pF	808-11109	Philips	1	VC1 (OPT 1)
132	Trim Capac.	3-154	22pF	808-11229	Philips	1	VC2
133	Crystal	10-705	10.08 MHz	DYN-7F	Leigh	1	XTAL1 (OPT 1)
134	Socket	19-367	8 PIN	2-641260-3	Amp	7	
135	Socket	19-368	14 PIN	2-641609-3	Amp	18	
136	Socket	19-368	14 PIN	2-641609-3	Amp	4	(OPT 2)
137	Socket	19-369	16 PIN	2-641610-3	Amp	28	
138	Socket	19-369	16 PIN	2-641610-3	Amp	3	(OPT 2)
139	Socket	19-370	18 PIN	2-641611-3	Amp	1	
140	Socket	19-370	18 PIN	2-641611-3	Amp	1	(OPT 2)
141	Socket	19-373	24 PIN	2-641614-3	Amp	1	
142	Socket	19-374	28 PIN	1828-AG11D	Augat	1	(OPT 2)
143	Socket	19-375	40 PIN	2-641616-3	Amp	1	(OPT 1)
144	Alarm	23-390		QMB-06	Star Micronics	1	ALM1 (OPT 2)
145	Connector	9-289	20 PIN HEADER	10-89-1201	Molex	1	CON1
146	Connector	9-316	5 PIN HEADER	640388-5	Amp	1	CON2
147	Connector	9-897	8 PIN HEADER	640384-8	Amp	1	CON3/CON4
148	Connector	9-292	25PIN R/A PCB FEMALE	147-11255-12-4338	Winchester	1	CON5 (OPT 2)
149	Connector	9-553	10 POSITION	10-89-1101	Molex	1	CON6 (OPT 2)
150	Connector	9-941	20 PIN HEADER	2-87224-0	Amp	2	CON7,CON8 (OPT 2)
151	Connector	9-924	.060	60874-1	Amp	12	
152	Heatsink	22-387		5041-B	Aavid	1	HS1
153	PC Board	26-718	3600D & 3700D MAIN	3600F1	Evertz	1	
154	Hardware	30-1087	TEST POINTS	20-2137D	Bicc Vero	30	

NOTE: INSTALL TEST POINTS TP1-TP30

8750 SUB MODULE #-3700D ONLY

155	Int. Circuit	1-665	QUAD D REGISTER	74HC173		1	U1
156	Int. Circuit	1-764	ROMLESS 8749 PROC	8039HPC	Mitsubishi	1	U2
157	Int. Circuit	1-617	4K x 8 EPROM	2732A-2		1	U3
158	Int. Circuit	1-763	8-BIT LATCH	74HC373		1	U4
159	Capacitor	2-112	27pF 100V	681-10279	Philips	1	C1
160	Capacitor	2-113	33pF 100V	681-10339	Philips	1	C2
161	Capacitor	2-129	.1uF 50V	SR215E104MAATR		2	C3,C4
162	Trim Capac.	3-541	10pF	808-11109	Philips	1	VC1
163	Crystal	10-705	10.08 MHz	DYN-7F	Leigh	1	XTAL1
164	Connector	9-291	20 PIN RECEPTACLE	22-02-2205	Molex	2	CON1,CON2
165	Socket	19-369	16 PIN	2-641610-3	Amp	1	
166	Socket	19-371	20 PIN	2-641612-3	Amp	1	
167	Socket	19-373	24 PIN	2-641614-3	Amp	1	
168	Socket	19-375	40 PIN	2-641616-3	Amp	1	
169	PC Board	26-769	PROCESSOR MODULE	8750	Evertz	1	

Options: 1 : 2

ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
170	Hardware	30-1087	TEST POINTS	20-2137D	Bicc Vero	4	

DISPLAY PC BOARD MODEL 3700D

ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
1	Int. Circuit	1-7	DECADE COUNTER	4017	MSC Only	1	U1
2	Int. Circuit	1-39	BCD TO 7 SEGMENT	4511		2	U3,U5
3	Int. Circuit	1-81	7 x NPN DARL. TRANS	MC1413	MOT Only	1	U2
4	Int. Circuit	1-665	QUAD D REGISTER	74HC173		1	U4
5	Transistor	8-270		MPS A13	Motorola	1	Q1
6	Transistor	8-275		MPS 2222	MOT Only	4	Q2-Q4-Q6
7	Transistor	8-276		MPS 2907	Motorola	2	Q5,Q6,Q7
8	Diode	6-255	SMALL SIGN. DIODE	1N4148		8	D1-D8
9	LED	15-354	LARGE	B11316		6	LED1-6
10	LED Display	14-349		MAN4640A-G	G.I.	16	DSP1-16
11	Resistor	4-195	1/4W 5%	4.7K 1/4W 5%	Philips	2	R1,R24
12	Resistor	4-172	1/4W 5%	100 OHM 1/4W 5%	Philips	18	R2-R10,R15-R23
13	Resistor	4-207	1/4W 5%	47K 1/4W 5%	Philips	4	R11-R14
14	Capacitor	2-129	.1uF 50V	SR215E104MAATR		2	C1,C3
15	Capacitor	2-135	10uF 16V	TAP10M16F	ITT	1	C2
16	Pushbutton	16-359	RED	SCHADOW D6	ITT	4	PB1,PB2,PB11,PB12
17	Pushbutton	16-720	IVORY	SCHADOW D6	ITT	10	PB3-PB10,PB13,PB14
18	Switch	17-714	8 POS SPST DIP	76SB08	Grayhill	1	SW1
19	Connector	9-553	10 POSITION	10-89-1101	Molex	1	CON1
20	Connector	9-310	20 PIN TRANSITION	54-20-1	Winchester	1	CON2
21	Connector	9-311	20 PIN CABLE SOCKET	51-1120-00	Winchester	1	CON3
22	Wire	29-495	RIBBON 20 COND.	55-2028-10	Winchester	7	INCHES
23	PC Board	26-717	3700D DISPLAY BD.	3700-02A	Evertz	1	

Options: 1 : 2
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ITEM	DESCRIPTION	OUR PART	ELECT. VALUE	MFG PART NO	MANUFACTURER	QTY	CIRCUIT NO.
OPT.1-3600D							
OPT.2-3700D							
VIDEO CONNECTOR PC BOARD							
1	Resistor	4-921	1/4W 1%	75 OHM 1/4W 1%	Phillips	3	
2	Connector	9-287	BNC	038-045-4327976	Sealectro	6	
3	Connector	9-288	SOLDERLUG FOR #287	761	Essco	6	
4	Switch	17-362	KNOB SLIDE	C56206L2	Switchcraft	1	
5	PC Board	26-431	VIDEO BOARD	3800-03A	Evertz	1	
MISCELLANEOUS							
6	Transformer	13-708	115/230V 24V.54A	FT1561	Frost	1	
7	Switch	17-363	115/230V FLUSHSLIDE	46256-LFE	Switchcraft	1	
8	Fuse Holder	21-383	HARDWARE INCL.	342004	Littelfuse	1	
9	Fuse	20-377	1/8 AMP SLOBLO	MDL 1/8A	Bussman	1	
10	Connector	9-308	POWER FILTER	CA-1L	SAE	1	
11	Connector	9-284	XLR	C3M	Switchcraft	2	
12	Connector	9-283	XLR	C3F	Switchcraft	1	
13	Connector	9-815	5 PIN SOCKET	640428-5	Amp	1	
14	Connector	9-732	8 PIN SOCKET	640433-8	Amp Only	1	
15	Connector	9-312	10 PIN CABLE SOCKET	51-1110-00	Winchester	2	(OPT 2)
16	Connector	9-670	JACK SOCKET ASSLY	4750-3	RAS	2	(OPT 2)
17	Wire	29-495	RIBBON 20 COND.	55-2028-10	Winchester	12	INCHES
18	Power Cord	28-493	BLACK	17250	Belden	1	
METAL WORK							
19	Metal Work	27-475	FRONT PANEL	3700-53	Evertz	1	
20	Metal Work	27-702	3700D F. OVERLAY	3700-58A	Evertz	1	(OPT 2)
21	Metal Work	27-703	3600D F. OVERLAY	3700-58B	Evertz	1	(OPT 1)
22	Metal Work	27-474	REAR PANEL 3600/3700	3700-52A	Evertz	1	
23	Metal Work	27-473	CHASSIS	3700-51	Evertz	1	
24	Metal Work	27-476	TOP COVERPLATE	3700-54	Evertz	1	
25	Metal Work	27-478	SAFETY COVER	3700-56	Evertz	1	
26	Metal Work	27-479	MTG. ANGLE	3700-57	Evertz	2	
27	Hardware	30-1123	3/8" 4-40 CS PHIL	MS-1180P	Spae Naur	4	
28	Hardware	30-1121	1/4"4-40 PH SS SCREW	MS-2344P	Spae-Naur	9	
29	Hardware	30-1118	4-40 HEX NUT	HN-201	Spae Naur	4	
30	Hardware	30-1120	4-40 STAR WASHER	W-2046	Spae-Naur	4	