MODEL 4900

EDIT CODE READER

INSTRUCTION MANUAL

Revision 2

CONFIDENTIAL

WARNING

This equipment generates and uses radio frequency energy, and if not installed and used in strict accordance with the instruction manual, may cause harmful interference to radio communications. It has been designed to comply with the limits for a Class A computing device pursuant to sub-part J of part 15 of FCC rules, which were designed to provide reasonable protection against such interference when operated in a commercial environment.

REV.	REVISION HISTORY	DATE
1	Original Issue (S/N 1732)	1/84
	Added NORM/OPT2 Switch. Correct pin connections for Parallel Outputs and Parallel Output protocol. (S/N 1977)	4/84
2	Section 4 technical description, Appendix I and sample configurations added. Errors corrected (S/N 2019)	5/84

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1. INTRODUCTION

The model 4900 Edit Code Reader uses the latest state of the art technology, combined with our extra intelligent firmware to offer you the finest and most versatile time code reader available. The model 4900 reads the standard SMPTE/EBU longitudinal time code at speeds from 1/30th to 70 times play speed.

The recovery of recorded time code at other than play speed has always presented some degree of difficulty. Due mainly to limitations imposed by magnetic head and audio frequency amplifiers, the reproduced code waveform at sub-playspeeds often suffers from severe distortion, particularly with low end 3/4 inch recorders lacking a separate time code track. The high speed reader in the 4900 employs sophisticated input conditioning and clock/data separator circuits to reliably recover time code over the full shuttle and wind speed range of most VTR's.

In many VTR's, the time code head position with respect to the video can vary considerably from machine to machine, causing a code phase shift relative to the video frame. The 4900 compensates for this code phase error and generates properly phase-locked LTC for the purpose of dubbing or editing without losing any frame counts. A parallel (8 bit wide) interface is provided to permit time and user bit data transfer to editors, etc.

A high quality character generator allows the generation of off-line editing copies. Two character sizes may be selected, one presenting high resolution characters for good legibility and another smaller size for stacking time code and user bit information in multi-generation edits where all original data must be retained.

Installing the optional plug-in VITCode module (model 49V), gives this reader tremendous additional capabilities. It can now read VITCode at speeds from 20 or 30 times play speed right down to still frame from the de-mod output of your VTR. Time base correcting the video will significantly enhance the recovery speed range. Combined with the longitudinal reader and the powerful microprocessor firmware, you get an Edit Code Reader which will consistently decode, display and or translate time code from still frame to maximum wind speeds. The built-in intelligence automatically selects valid code from either source and presents the data to the front panel display, the character inserter, and the LTC and parallel outputs. You'll appreciate the smooth and hesitiation free code display.

2. INSTALLATION

2.1 MOUNTING

The standard unit is equipped with rack mounting angles and fits into a standard 19 inch by 1 3/4 inch (483mm x 45mm) rack space. The mounting angles may be removed if rack mounting is not desired.

2.2 POWER

Power requirements are 115 or 230 volts AC at 50 or 60 Hz, switch selectable at the rear panel. Before connecting the line power, be sure to select the proper line voltage. Also check that the line fuse is rated for the correct value. Never replace with a fuse of greater value.

2.3 Video Input and Output

The program source for the character generator or the reader video with VITCode should be applied to the Video INP loop. The video input has a high impedance input tapped off the loop through, therefore the input must be terminated with 75 ohms at the end of the line. The LTC code output will be properly phased to the input video signal at play speed.

Two isolated character generator outputs are provided to drive a preview monitor and a video recorder.

2.4 LONGITUDINAL TIME CODE IN/OUT

The LTC reader input connects to your head pre-amplifier output. When using an unbalanced input to the reader, the signal should be applied to pin 3 of the reader input connector. Normally, the unused input, (pin 2) should be connected to ground (pin 1).

A fully decoded and regenerated LTC output is provided. This output is a play speed regenerated code from the current source being read (indicated by the VITC and LTC indicators). When the incoming code is at normal play speed, the output code is properly synchronized to the video, thus compensating for LTC code misalignment from the video, or providing an LTC translation of incoming VITCode.

Note: When using the regenerated LTC output, the video from the tape being read must be looped thru the video input (See Section 2.3) to ensure correct phasing of the LTC output to the video. (See also Section 3.1 NORM/OPT2 switch)

In audio tape applications or other situations where video cannot be looped through the video input, it is advisable to use the re-clocked output instead of the regenerated output. To accomplish this, two jumpers on the main circuit board marked "RE-GEN" must be cut and two jumpers marked "RE-CLK" must be installed.

2.5 PARALLEL BCD OUTPUT

Parallel BCD time and user bit data are multiplexed on 10 output lines at the 25 pin connector (see section 2.7 for pin assignments) as follows:

The clear to send (CTS) line is brought low at the beginning of the sequence. Then, a 4 bit address is output on lines BCD0 thru BCD3 along with a positive going strobe. Eight bits of data are then output on lines BCD0 thru BCD7 along with a negative going strobe. This cycle is repeated for each of the 8 digit pairs listed below. When the output sequence is complete, the CTS line returns high. The sequence of data outputs is presented once per field, unless the display freeze is active. See Figure 2-1 for BCD output waveforms.

ADDRESS	DIGIT PAIR
0000	Frames
0001	Seconds
0010	Minutes
0011	Hours
0100	1st & 2nd Binary Groups
0101	3rd & 4th Binary Groups
0110	5th & 6th Binary Groups
0111	7th & 8th Binary Groups

Flag bits are output along with the time information as follows:

POSITION	BIT #	NTSC	PAL
Frames Bit 6	10	Drop Frame	Unassigned
Frames Bit 7	11	Colour Flag	Colour Flag
Seconds Bit 7	27	Phase Parity Bit	Binary Group #1
Minutes Bit 7	43	Binary Group #1	Binary Group #2
Hours Bit 6	58	Binary Group #2	Unassigned
Hours Bit 7	59	Unassigned	Phase Parity Bit

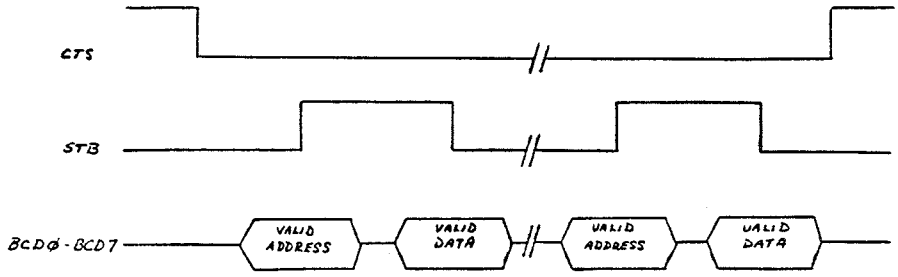


Figure 2-1 BCD Output Waveforms

2.6 REMOTE CONTROL

The remote control interface permits control from one or more remote locations. Any or all of the front panel keys can be remoted. Eight pins from the 25 pin connector (see section 2.7 for pin assignments) are used by the remote control interface. The keypad is arranged in a matrix consisting of 4 rows by 4 columns. Connection of any row with any column by a momentary contact switch uniquely identifies one of the key functions. For multiple locations, several momentary contact switches may be wired in parallel. The table below shows the position of each key function in the keypad matrix.

ROW NO.	COLUMN 1	2	3	4
1	ON/OFF	not used	USR'B	not used
2	not used	VERT	not used	not used
3	not used	not used	HOR	not used
4	FREEZE	not used	MODE	not used

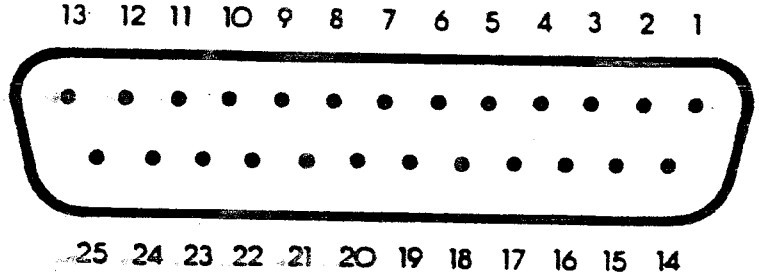
Note: **Static electricity can destroy CMOS device connected to remote control interface cable. USE CAUTION WHEN HANDLING.**

2.7 I/O CONNECTOR PIN ASSIGNMENTS

Note: To avoid conflict, connect only the pins required for your application.

Pins 10 thru 13, and 22 thru 25 refer to the remote control interface.

Pins 8, 9, and 14 thru 21 refer to the Parallel BCD data output.



Pin	Name	Description
1	GND	Signal Ground
2	--	Not Used
3	--	" "
4	--	" "
5	--	" "
6	--	" "
7	--	" "
8	STB	Address / Data Strobe
9	CTS	Clear to Send
10	R4	Remote control Row 4
11	R3	Remote control Row 3
12	R2	Remote control Row 2
13	R1	Remote control Row 1
14	BCD7	Parallel BCD Output bit 7
15	BCD6	Parallel BCD Output bit 6
16	BCD5	Parallel BCD Output bit 5
17	BCD4	Parallel BCD Output bit 4
18	BCD3	Parallel BCD Output bit 3
19	BCD2	Parallel BCD Output bit 2
20	BCD1	Parallel BCD Output bit 1
21	BCD0	Parallel BCD Output bit 0
22	C4	Remote control Column 4
23	C3	Remote control Column 3
24	C2	Remote control Column 2
25	C1	Remote control Column 1

2.8 SAMPLE CONFIURATIONS

Several sample installation setups are diagrammed below to aid the user in properly connecting the 4900 into his system. Contact us for other applications.

Figure 2-2 illustrates the basic set-up for reading LTC and VITC, making off-line cassette copies with character burn-ins, or for dubbing tapes with regenerated time code. Longitudinal code misalignments from the video frame are compensated for, and the regenerated LTC is properly timed to the video. The source video must be looped through the video input of the 4900 to ensure correct timing of the output LTC to the video. (See section 3.1 NORM/OPT2 switch)

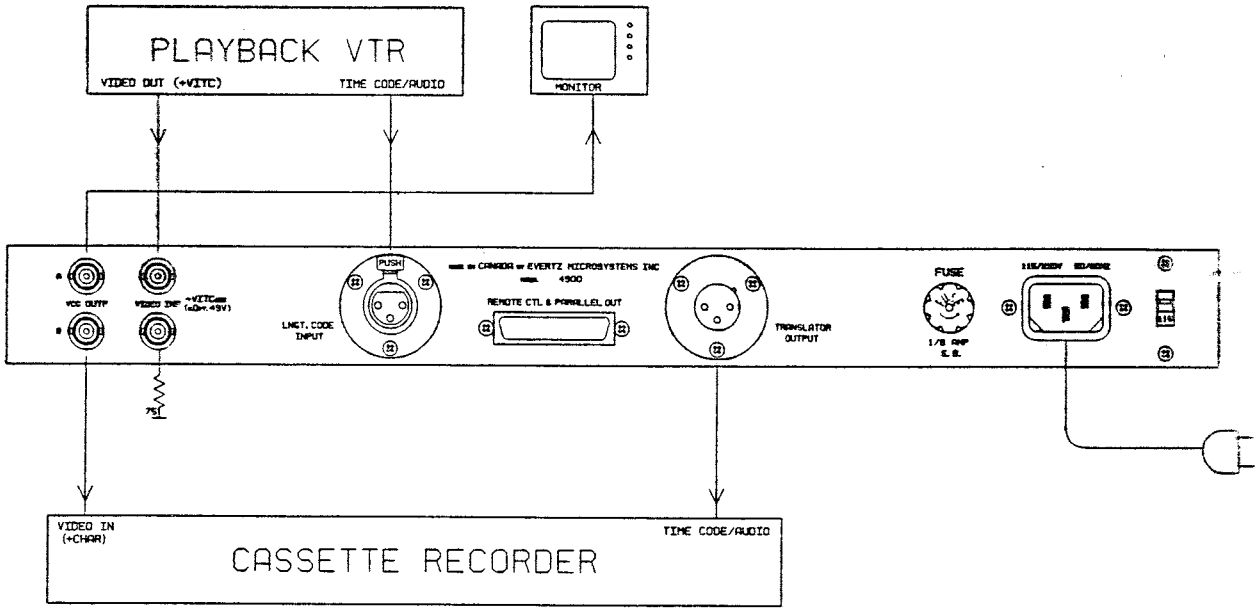


Figure 2-2 Dubbing and Off-line Character Burn In

Figure 2-3 illustrates the setup for a VITC/LTC editing system. Using the 4900 Edit Code Reader, your existing editing system can use LTC only, VITC only or both LTC and VITC together for both edit decision making and editing. The video from each source VTR is looped though the respective 4900, which will read VITC whenever it is present on the video. It is important that the VITC is recorded on vertical interval lines that will be reproduced by your VTR in playback. See your VTR manual for further information. If a time base corrector is used, the video output should be fed to the 4900 prior to TBC processing, because many TBC's blank the vertical interval, and eliminate the VITC. If it is desired to time base correct the video before the 4900, make sure that the lines containing the VITC are passed through the TBC.

The recovered VITC is translated to LTC by the 4900, which can be read by the LTC reader in the edit controller. The new LTC is generated at approximately play speed so that the edit controller can read it during slow motion decision making and also for cueing and parking the VTR during editing. When the incoming code is at play speed, the LTC is synchronized to the video, so that the edit controller can use it to synchronize the playback and record VTRs during the edit pre-roll interval, just as it would have used the original LTC from the VTR.

If it is desired to record VITC on the record VTR, a VITC/LTC jam-sync generator, such as our model 4000, must be used in the place of the 4900 on the record VTR. During the edit pre-roll, when the record VTR is in playback, the jam-sync generator will follow the numbers read from the record machine. When the record VTR switches from playback to record, the jam-synced VITC will be recorded in the video without interruption. See model 4000 Instruction Manual for more detailed information

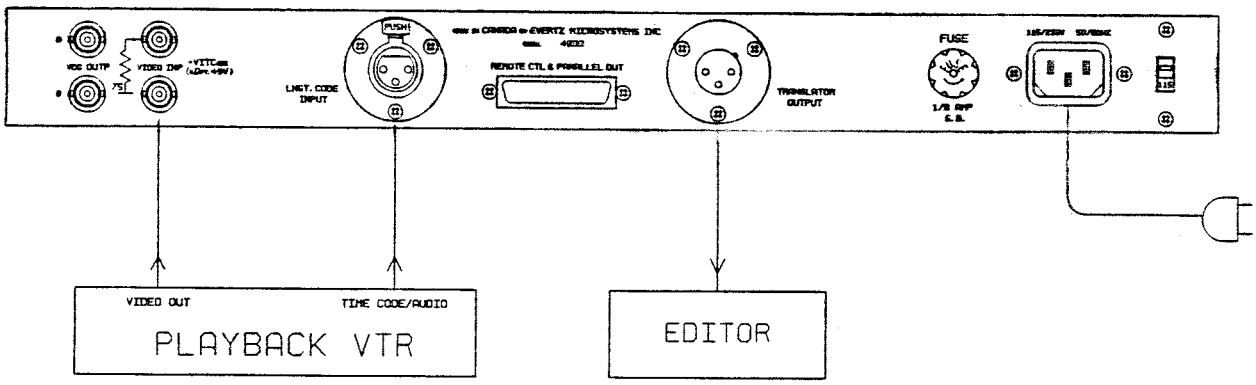


Figure 2-3 VITC translation to LTC for Editing

3. OPERATING INSTRUCTIONS

The model 4900 Edit Code Reader provides a display of time or user bit information from either the LTC or VITCode (optional) readers using an 8 digit display or using characters keyed into the input video. Operational control is handled by 6 front panel keys. A FORMAT DIP switch permits certain parameters and operating modes to be preset to adapt the unit to your particular operating methods. Five LED's provide operational status at a glance.

Figure 3-1 Front Panel Layout

3.1 FORMAT FUNCTIONS

An 8 position DIP switch is located near the centre of the front panel, and is used to configure the following operational modes. The unit will operate in these modes until they are altered using a small screwdriver or other pointed device.

FRAM/BLNK Selects frames blanking of the reader display when BLNK is selected.

VITC/LTC Selects the reader source being displayed as Longitudinal time code (LTC) or Vertical Interval Time code (VITC) when the MAN'L/AUTO SWITCH is set to MAN'L. When **AUTO** is selected, this switch is ignored.

MAN'L/AUTO Selects either manual (MAN'L) selection of reader source (see above) or automatic (AUTO) selection of the "most valid code." When AUTO is selected, the reader will continue reading from whatever source was previously selected. When it encounters invalid code, the reader will display the other source, if valid code exists on that source. Otherwise, it will continue displaying the last valid code read until valid code resumes on one of the sources. If the reader switches sources, it will not switch back, even if valid code resumes on the previous source, until it encounters invalid code on the presently selected source. This permits continuous time code reading where speeds exceed the reading capabilities of one of the readers (in excess of 30 times play speed for VITCode or less than about 1/10 play speed for LTC), as long as both LTC and VITCode have been recorded on the tape. If only one code has been recorded on the tape, then that particular code source should be selected for the best operation of the reader. When AUTO is used both codes should be identical or unpredictable results may occur.

VCG/OO-oo Selects a high resolution 16 line per field character size (OO) or a lower resolution 8 line per field. (oo) This smaller size is useful for displaying data from several generations of off-line editing without covering too much of the active picture.

FLD1/FLD2 Selects whether the VCG characters will be "on time" (FLD1) or 1 field late (FLD2). This latter mode is useful where edits will be performed on field 2, and the burn in must correspond to the actual edit point. This switch is only active when the MAN'L/AUTO switch is set to MAN'L and the VITC/LTC switch is set to LTC. For most uses this switch should be set to FLD1.

NORM/OPT1 When OPT1 is selected, the reader will read the VITCode format which was developed by SONY before standards were established by the EBU and S.M.P.T.E. This format uses bit 15 for a field mark bit, instead of the standard bit 35 (75 for PAL). For most uses this switch should be set to NORM.

NORM/OPT2 Select NORM if the regenerated LTC output is used for code dubbing applications. Select OPT 2 when the LTC output is used as a code translator to your editor's LTC reader.

NORM/OPT3 ~~Reserved for future option.~~
Select NORM if the fields are to be displayed. Use in making VITC.
Select OPT 3 when the fields are to be blanked.

3.2 READER CONTROL FUNCTIONS

Two keys in the DISPLAY key group provide control over the LED display.

USR.B Alternately displays the reader time or user bits. A status LED in the upper left corner of the reader display indicates when user bits are being displayed. Also, the colons of the reader display are blanked when user bits are displayed.

FRZ Freezes the reader display. Alternate action of this key restores the normal display mode.

3.3 CHARACTER GENERATOR CONTROLS

Four keys in the CHAR. GEN key group control the display of reader information in the character generator.

ON/OFF Alternate action of this key turns the character generator on and off.

MODE The first time this button is pressed, the reader time is displayed. The next time, the reader user bits are displayed. The third time both the time and user bits are displayed.

HOR The displayed characters move to the right 1 position each time it is pressed. When the characters reach the rightmost position they return to the left hand side. The number of horizontal positions depends on the size, and the data displayed. This key will "auto repeat" when held down for more than 1 second.

VERT Moves the displayed characters down 1 line each time it is pressed. When the characters reach the bottom of the screen, they return to the top. There are 13 (15 for PAL) vertical positions in the large size and 26 (30 for PAL) in the small size. This key will "auto repeat" when held down for more than 1 second.

3.3.1 Special Indicators

The following special indicators are used between the seconds and frames digits in the character inserter to identify non drop frame and drop frame code (NTSC only) and whether the character generator is updating on time or 1 field late (determined by FLD1/FLD2 switch setting - see section 3.1)

	FLD1	FLD2
Non Drop Frame	Colon (:)	Semi-colon (;)
Drop Frame (NTSC)	Period (.)	Comma (,)

3.3.2 Field Identification

When reading VITCode, the field number sequence will be displayed to the right of the reader time frames display. When the data being read was recorded in the non colour frame mode, ie. the COL'R indicator is off, the field number sequence will be 1, 2, 1, etc. (1, 2, 3, 4, 1, etc. for PAL). When the reader data was recorded in the colour frame mode, ie. the COL'R indicator is on, the field number sequence will be 1, 2, 3, 4, 1, etc. (1, 2, 3, 4, 5, 6, 7, 8, 1, etc. for PAL)

3.3.3 Source Identification

If the data being read contains user bits in the **Evertz** source ID format, the decoded message will be displayed if the character generator is turned on. See Appendix II for a list of the source ID messages that will be decoded.

3.4 Status Indicators

There are five status indicators that show operational status at a glance.

U.B. Located beside the reader display indicates user bits are being displayed.

VITC Indicates that the reader data being displayed is coming from the VITCode reader.

LTC Indicates that the reader data being displayed is coming from the LTC reader.

Selection of the source of reader data is controlled by the VITC/LTC and MAN'L/AUTO switches (see section 3.1 above).

COL'R Indicates that the data being read was recorded in the colour frame mode, ie. the correct relationship between frame address and colour burst phase was adhered to.

D.F. Indicates that the data being read was recorded in the SMPTE drop frame format.

4. TECHNICAL DESCRIPTION

The Model 4900 Edit Code Reader is a microprocessor based system functionally divided into the following major hardware subsystems:

1. Microcomputer and LTC Translator
2. High Speed LTC Reader
3. VITC Reader Module
4. Video Sync Separator and Character Generator

See Drawing 4900-30 for a functional block diagram

4.1 MICROCOMPUTER

At the heart of the model 4900 is an 8749 microcomputer, (MCU), U23. Its two 8 bit bi-directional ports and 8 bit bus provide peripheral interfacing to the rest of the circuit. Program memory, and scratch pad and data RAM are provided internally by the MCU, and only the external VCG RAM is required.

4.1.1 LTC TRANSLATOR

An onboard oscillator, also part of the MCU is crystal controlled. Its 10.06992 MHz (10.08 MHz PAL) is internally divided by 15, resulting in an operating frequency (ALE) of approximately 672 KHz. The MCU system clock, (ALE) is divided down by U21 to provide a clock of 167.832 KHz (168 KHz PAL) to the T1 input of the MCU. The translator clock frequency must be properly calibrated for proper translator locking to occur. It can be measured at (ALE/4) and may be adjusted using VC1. The MCU divides this clock signal internally and generates the translator time code edge for edge on P10. This output is registered to the bit clock by U22a and shaped by U20.

4.1.2 Display / Keypad Interface

An 8 digit display, 8 position DIP Format switch, and a 6 button keypad contained on a separate circuit card (3600-02) interface to the MCU via a 20 conductor ribbon cable. The 8 digit display and 4 status LED's are multiplexed; that is segment information for each digit is presented in coincidence with a digit enable pulse to the appropriate digit. The 6 keys and DIP switch are arranged in a 4 x 6 matrix. Data from 4 keys or one half of the DIP switch is latched into U5 at the time of the digit enable pulse, thus scanning the total array.

4.2 HIGH SPEED LTC READER

Incoming code is decoupled and amplified by U1, U2, U11 and associated components to provide a regenerated reader data signal at U11 pin 5. A series

of timing pulses, generated by U6 and U7, are used to properly decode 0 and 1 bits of the incoming code. A constant amplitude ramp (RAMP) is generated by U3 and associated components. Three quarters of the peak ramp level is used as a reference on comparator U4 to decode the data from the clock transitions. If the next code bit is a 0, then the ramp will exceed the reference before the next transition. (COMP) If the next bit is a 1, then an extra transition will occur before the ramp exceeds the reference, clocking flip flop U6a on.

The LTC data is shifted through sync detector U8 and U10 into one half of shift register U14 by the recovered LTC clock (CLK). Twelve consecutive 1 bits, detected by U9, (SYNC) clock flip flop U12a on, freezing the sync word data at the outputs of U8 and U10, and generating a LTC RDY signal to the MCU when it has received one frame of data. Direction information, derived from the last bit of the sync word is also fed to the MCU. A valid reader sync word toggles flip flop U12b enabling the other half of U14 to collect data from the next frame. The MCU unloads LTC data from the previous frame through switch U15 when the SEL line is low, and unloads VITC data when the SEL line is high.

4.3 VITC READER MODULE (49V)

The clock and data separator circuitry for the VITC reader is contained on a separate module (Model 49V) which connects to the main PC board by header CON 5. VITC data is recovered from the DC restored video by comparator U2. U1 and associated components provides a reference level of approximately one half the peak VITC level to U2, ensuring proper extraction of the data regardless of the level.

At VSYNC, the MCU releases the reset to U5a, enabling the VITC reader circuitry. The first VITC data bit turns on U5b, which releases the reset to CRC detector U6 and U10. A crystal controlled oscillator, U3 operates at 14.31818 MHz (14.5 MHz for PAL) and is divided by U11 to generate the 1.78977 MHZ (1.8125 MHz for PAL) VITC bit rate clock. (VTC CLK) Each positive going transition of the VITC data (VTC DATA) re-synchronizes bit rate divider U11 so that the VITC recovery clock at U7 pins 4 and 12 occurs in the middle of each bit.

Inverted VITC data is shifted into U6 which calculates the cyclic redundancy check (CRC) word for the recovered data. (See Appendix I for a discussion of the VITC data format.) Valid CRC and 90 bits of code, detected by U8, clocks U5b on, disabling the bit clock to U7, and generating the VITC RDY signal to the MCU. The MCU unloads the VITC data through switch U15 on the main PC board.

4.4 VIDEO CHARACTER GENERATOR

4.4.1 Sync Separator

Composite video is buffered by Q5 and composite sync is extracted by U24 and associated components. Immediately following each horizontal sync pulse a sample pulse is generated at U24e which allows U25 to compare the actual DC level of the video to ground potential. If they are not equal, the bias point

of Q7 is adjusted by FET Q6 operating as a variable resistor, thus ensuring proper operation of the video keyer and VITC reader with varying video and sync levels. Composite SYNC is split into horizontal sync (HSYNC) by U29a, and is integrated by U35a to derive vertical sync (VSYNC) at U35b, generating an interrupt to the MCU at U23 pin 6.

4.4.2 Field 1 / Field 2 Detector

Monostable U34a is triggered by the leading edge of HSYNC and times out about 45 μsec later generating a 3/4 H signal. During VSYNC, flip flop U26b toggles at each successive serration, clocking U26a on during field 2 of each video frame. When the video input signal comes from a 3/4" U-matic tape recorder operating in the shuttle mode, the serrations are absent, thus the field 2 detector never clocks on. The state of the field 2 detector is sampled by the MCU after each VSYNC interrupt.

4.4.3 Character Scanning Logic

The character display is formatted to allow 13 (15 for PAL) rows of 30 characters in the large size and 26 (30 for PAL) rows of 60 characters in the small size. Immediatley following VSYNC the MCU presets the vertical position into counter U39 and writes characters into one of 64 locations of RAM U40, and U41 corresponding to the position of the characters on the line. RAMENA is used to switch the clock to RAM scanning counter U42 from the dot oscillator to the MCU, while new character data is being entered. Character output is blanked during RAM updates to avoid random character noise in the video.

At the start of each field, U36 counts 32 lines past VSYNC and clocks U37b on. Counter U39 then advances (from the number preset by the MCU) every 8 horizontal lines. The Q6 output of U39 enables the horizontal dot oscillator U29b and U33 outputs a character load pulse every 8 character dots. RAM locations are scanned by U42 on the successive horizontal lines until 16 (8 for the small size) character lines are scanned. Output Q10 of U42 turns off the scanning logic until the MCU initializes it for the next field. Valid characters address corresponding sections of the character PROM U44 and character data is shifted out from U45 and keyed into the video by U28. Bit 6 of the RAM turns off the keyer control flip flop U31a at all positions where characters are not displayed.

4.4.4 Character Size and Positioning Adjustments

Horizontal size of the characters is adjusted by VR1. (HORZ SIZE) The starting position of the characters at the left of the screen is preset to about 10 μsec after the leading edge of HSYNC.

4.4.5 Video Amplifier and Character Keyer

The keyer control signal from U32 switches U28a on allowing the program video, which has been DC restored by U25, Q5 through Q7 and associated components, to pass through the video amplifier wherever characters are not present. When U28b characters are present, U32 switches U28a off and U28b on, keying the black level (0 volts DC) into the video. White level character dots are added at the common emmitter of Q8 and Q9. Isolation diodes D10 and D11 are reversed biased when no characters are present, ensuring that no spurious character information will be injected into the program video path.

To calibrate the video keyer, connect colour bars from your sync generator to the VCG input loop and to channel A of your scope, and terminate it. Connect the VCG output to channel B of your scope and terminate it. Adjust the **GAIN** trimpot (VR3) so that the output amplitude matches the input. Adjust the **LEVEL** trimpot (VR2) so that the inserted characters are slightly above peak white luminance level.

APPENDIX I:

SMPTE/EBU TIME AND CONTROL CODE SPECIFICATIONS

INTRODUCTION

The SMPTE/EBU Time and Control Code is a digital code which is used for timing and control purposes on Television tape machines and on associated audio tape machines, if any. The original code format, developed in the early 1970's, is recorded on a longitudinal track with audio characteristics, and is referred to as Longitudinal Time Code (LTC). Since then, new video recording formats have appeared which can be used at very slow tape speeds. A new version of the time code was developed which allows reliable recovery right down to still frame. This code, inserted in the field blanking interval of the video signal itself is referred to as Vertical Interval Time Code (VITC).

1. LONGITUDINAL TIME CODE

LTC is a digital signal comprised of 80 bits of information, numbered 0 through 79 inclusive, which are evenly spaced over an entire television frame. The modulation method is such that a transition occurs at the beginning of every bit period. A binary "one" is represented by a second transition one half bit period from the start of the bit. A "zero" bit is represented when there is no transition within the bit period. This system, known as bi-phase mark is illustrated below.

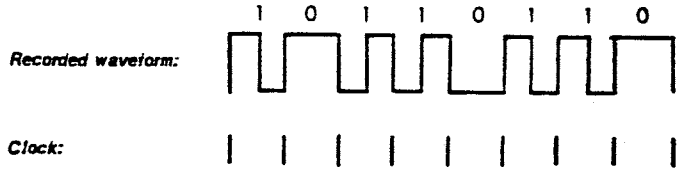


Figure I-1 Bi-Phase Mark Encoding Scheme

The nominal bit period is 80 times the television frame rate (30 Hz for NTSC 25 Hz for PAL). The clock edge before the first address bit (bit 0) occurs during the field synchronizing pulses at the start of field one of the television frame with which the code word is associated.

Each 80 bit code word is comprised of 26 time bits, 6 flag bits, 32 user bits and 16 sync bits. The basic structure of the time bits is based on the Binary coded decimal (BCD) system. In those cases where the count does not attain 9, only 2 or 3 bits are required, rather than the normal 4 bits. These six bits are used as flags to indicate various operational modes as follows:

Drop Frame (NTSC Only): If frame numbers (0,1) at the start of each minute except 0,10,20,30,40, and 50 are omitted from the count to resolve the difference between real time and colour time a "1" is set.

Colour Frame: If colour frame identification has been intentionally applied to the time numbers, a "1" is set.

Bi-phase Mark Phase Correction: This bit is put in a state such that every 80 bit word contains an even number of logic zeros.

Binary Group Flags: The 32 bits within the eight user bit (binary) groups may be assigned in any way if both binary group flags are zero. If an eight-bit ASCII character set is used for user bit data, then the first binary group flag is set to "1". At this time the second time binary group flag is always set to zero.

The following table shows the differences between SMPTE and EBU versions of the time and control code.

	SMPTE	EBU
T.V. Frame Rate	30 Hz	25 Hz
Code Bit Rate	2400 Hz	2000 Hz
Code Bit Period	416 μsec	500 μsec
Rise and Fall Times	25 μsec	50 μsec
Flag Bit Assignments		
Bit 10	Drop Frame	Unassigned
Bit 11	Colour Frame	Colour Frame
Bit 27	Bi-Phase parity	Binary Group 1
Bit 43	Binary Group 1	Binary Group 2
Bit 58	Unassigned	Bi-phase parity
Bit 59	Binary Group 2	unassigned

2. VERTICAL INTERVAL TIME CODE

VITC is a digital signal comprised of 90 bits of information, numbered 0 through 89 inclusive, which is recorded on two non-adjacent lines during the vertical blanking interval of each television field. The modulation method is such that each state of the signal corresponds to a binary state, and a transition occurs only when there is a change in the data contained in adjacent bit cells. This system, known as "non return to zero", (NRZ) is illustrated below.

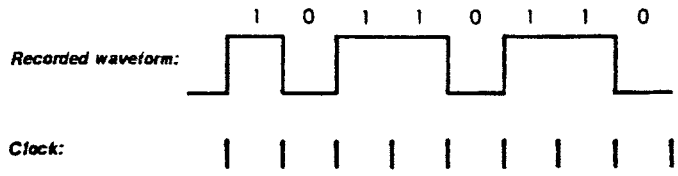
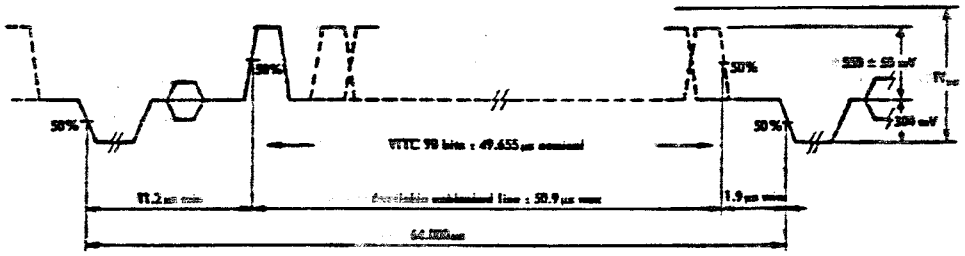
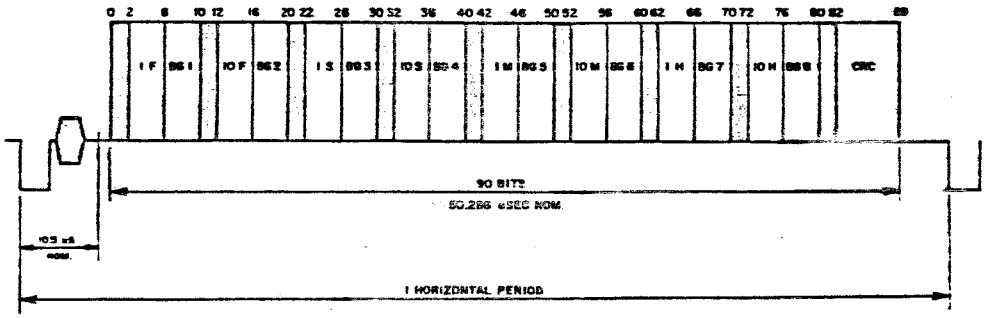


Figure I-2 Non Return to Zero Encoding Scheme

The nominal bit rate is 113.75 (116 for PAL) times the line frequency, resulting in a bit rate of 1.789 MHz for NTSC and 1.812 MHz for PAL. Each television frame is identified by a complete code word, which contains a "field mark bit" set in field 2 of each frame.



(a) EBU Specification



(b) SMPTE specification

Figure I-3 Position of VITC on the Line

The structure of the information is similar to the longitudinal time code with the following exceptions:

1. Nine sync bit pairs fixed as a "1" bit followed by a "0" bit are evenly spaced throughout the code to aid in the decoding process.

2. Eight bits are set aside at the end of the code word for error detection by means of cyclic redundancy checking. When the CRC is recalculated on recovery of the data, the result should by zero, if no errors are detected. The CRC also permits detection of bursts of errors such as can be encountered in magnetic recording.

3. The Bi-phase parity bit is used for field identification. The field mark is set to "1" during the second field of each television frame, and enables a VITC reader to identify odd and even numbered fields without reference to the field synchronizing signal.

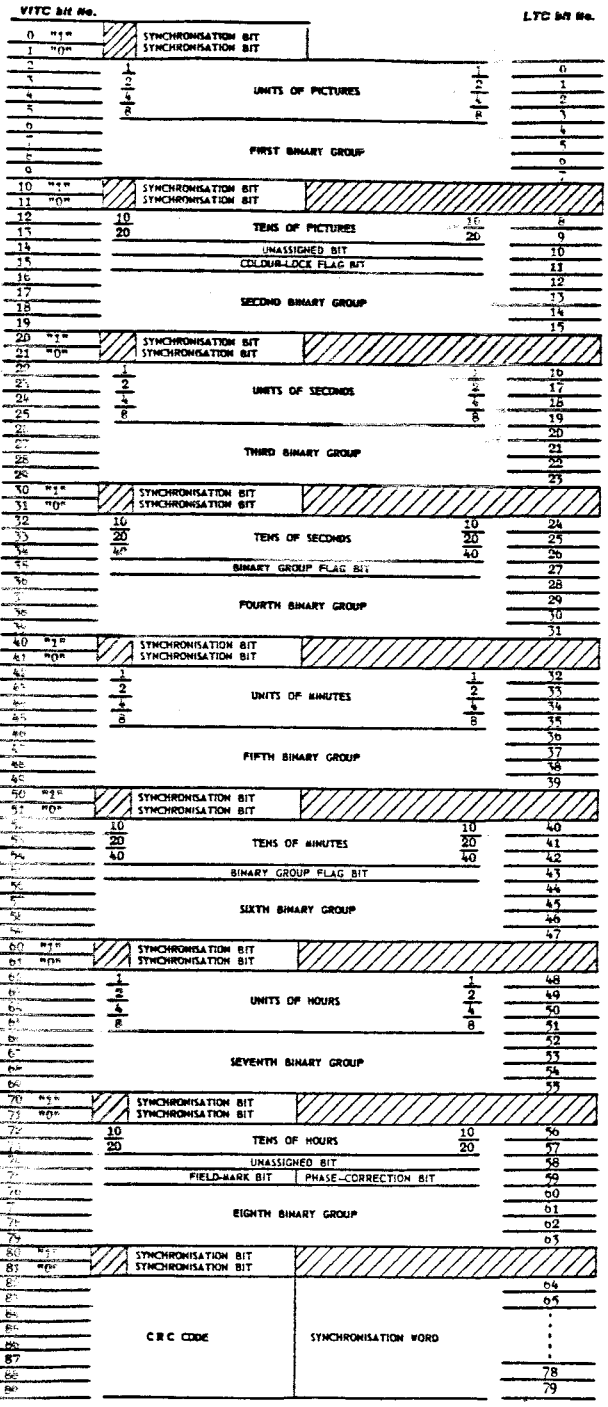


Figure I-4 Relationship between VITC and LTC (EBU)

APPENDIX II:

SOURCE IDENTIFICATION MESSAGES

DISPLAYED MESSAGE	MSG #	DISPLAYED MESSAGE	MSG #
	00	NET	32
JAN	01	OB	33
FEB	02	PRES	34
MAR	03	REM	35
APR	04	SAT	36
MAY	05	SLID	37
JUN	06	STL	38
JUL	07	STUD	39
AUG	08	TC	40
SEP	09	TEST	41
OCT	10	TV	42
NOV	11	VCR	43
DEC	12	VITC	44
AIR	13	VT	45
AUX	14	VTR	46
BARS	15	SPARE	47
BAY	16	SPARE	48
BLK	17	SPARE	49
BVU	18	SPARE	50
CAM	19	SPARE	51
CAP	20	SPARE	52
CGEN	21	SPARE	53
CLK	22	SPARE	54
CRT	23	SPARE	55
DUB	24	SPARE	56
ECM	25	SPARE	57
EDIT	26	SPARE	58
ENG	27	SPARE	59
FILM	28	SPARE	60
LINE	29	SPARE	61
MCR	30	SPARE	62
MON	31	SPARE	63

Figure II-1 - Message Select Codes