Model 5700MSC-IP
IP Network Grand Master Clock & Video Master Clock System
User Manual

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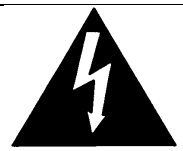
IMPORTANT SAFETY INSTRUCTIONS

	The lightning flash with arrowhead symbol within an equilateral triangle is intended to alert the user to the presence of uninsulated “Dangerous voltage” within the product’s enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.
	The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (Servicing) instructions in the literature accompanying the product.

- Read these instructions
- Keep these instructions.
- Heed all warnings.
- Follow all instructions.
- Do not use this apparatus near water
- Clean only with dry cloth.
- Do not block any ventilation openings. Install in accordance with the manufacturer’s instructions.
- Do not install near any heat sources such as radiators, heat registers, stoves, or other apparatus (including amplifiers) that produce heat.
- Do not defeat the safety purpose of the polarized or grounding-type plug. A polarized plug has two blades with one wider than other. A grounding-type plug has two blades and a third grounding prong. The wide blade or the third prong is provided for your safety. If the provided plug does not fit into your outlet, consult an electrician for replacement of the obsolete outlet.
- Protect the power cord from being walked on or pinched particularly at plugs, convenience receptacles and the point where they exit from the apparatus.
- Only use attachments/accessories specified by the manufacturer
- Unplug this apparatus during lightning storms or when unused for long periods of time.
- Refer all servicing to qualified service personnel. Servicing is required when the apparatus has been damaged in any way, such as power-supply cord or plug is damaged, liquid has been spilled or objects have fallen into the apparatus, the apparatus has been exposed to rain or moisture, does not operate normally, or has been dropped.

WARNING
TO REDUCE THE RISK OF FIRE OR ELECTRIC – SHOCK, DO NOT EXPOSE THIS APPARATUS TO RAIN OR MOISTURE

WARNING
DO NOT EXPOSE THIS EQUIPMENT TO DRIPPING OR SPLASHING AND ENSURE THAT NO OBJECTS FILLED WITH LIQUIDS ARE PLACED ON THE EQUIPMENT

WARNING
TO COMPLETELY DISCONNECT THIS EQUIPMENT FROM THE AC MAINS, DISCONNECT THE POWER SUPPLY CORD PLUG FROM THE AC RECEPTACLE

WARNING
THE MAINS PLUG OF THE POWER SUPPLY CORD SHALL REMAIN READILY OPERABLE

INFORMATION TO USERS IN EUROPE

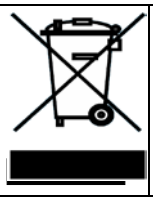
NOTE

CISPR 22 CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to the European Union EMC directive. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

CE

EN60065	Safety
EN55103-1: 1996	Emission
EN55103-2: 1996	Immunity



EN504192 2005
Waste electrical products should not be disposed of with household waste.
Contact your Local Authority for recycling advice

INFORMATION TO USERS IN THE U.S.A.

NOTE

FCC CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

WARNING

Changes or Modifications not expressly approved by Evertz Microsystems Ltd. could void the user's authority to operate the equipment.

Use of unshielded plugs or cables may cause radiation interference. Properly shielded interface cables with the shield connected to the chassis ground of the device must be used.

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REVISION HISTORY

REVISION	DESCRIPTION	DATE
0.2	Preliminary Release	July 2018

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1. OVERVIEW

Figure 1-1: Front View of the 5700MSC-IP

The 5700MSC-IP is an IP Network Grand Master Clock and a Video Master Sync Generator both referenced to GNSS (Global Navigation Satellite System (GPS and/or GLONASS)). The system features two 1Gb/s Ethernet, two 10Gb/s Ethernet SFP ports, 6 fully timeable sync outputs, 4 SDI outputs, and a loop thru reference input. For those hybrid plants where LTC outputs and AES/analog audio test generator signals required, an optional (+AUX) expansion module is available.

This combo IP Network Grand Master Clock and Master Sync Generator is ideal for timing today's IP based video broadcast, production, and distribution facilities. It provides all the future timing needs of an IP based plant while providing precision reference to any baseband SDI/Analog systems.

The test generator option(s) provide several test generator signals which are available on the 4 SDI (SD/HD/3Gbps) outputs as well as over the 10Gb/s Ethernet IP outputs (10Gb/s Ethernet SFP's are optional). There are 10 independent test signal generators when a test generator option is ordered, any can be routed to the 10Gb/s Ethernet outputs, or the SDI outputs (4 generators may be combined to form a 4K signal generator).

As for IP timing formats, the 5700MSC-IP has been designed to be enterprise class, handling all current IP timing needs with the horsepower to address the future. It supports NTP, PTP-IEEE1588, MASTER PCR, AVB-IEEE802.1AS, AES67 profile and SMPTE 2059-2. IP networking for live production and broadcast environments have very specific needs and requirements that typically involve deterministic flows, high bandwidth, and an SDN based network design. The 5700MSC-IP can be used to design a robust, safe, and deterministic timing system for any IP Network or Hybrid IP/Baseband Video system. The product has been designed to handle timing requirements of several thousands of PTP clients. The 5700MSC-IP has two 10Gb/s Ethernet ports as well as two 1Gb/s Ethernet ports that can be configured to provide and distribute any of the timing protocols described above.

This 5700MSC-IP is delivered with a GNSS head capable of receiving GPS and GLONASS satellite constellation signals and complete with a 50ft cable for remote mounting. (100ft, 400ft and fiber optic extension options are available for longer cable lengths).

A high stability, temperature controlled oscillator provides the 5700MSC-IP with better than 1.0x10-8 (or 0.01ppm) frequency reference. The free running drift of this 10MHz reference will be less than 0.1Hz (which amounts to less than one millisecond time drift per day). This guarantees that any frequency drift, with time and temperature, will be within the tolerances expected from the best SPGs or master clocks available in the industry. Note that the provided GNSS head capable of receiving GPS and GLONASS satellite constellation signals is required for PTP, AVB PCR, or 2059-2 timing protocols to be hosted by the system. The 5700MSC-IP can also produce PTP, AVB, PCR or 2059-2 timing protocols when using a PTP reference of suitable quality.

The SPG section of the 5700MSC-IP provides six independent timeable reference outputs. These six sync outputs may be configured to provide independently timed color black (black burst) outputs, independently timed HDTV tri-level sync outputs, 10MHz outputs, word clock, and various available pulses.

It is available with a main processing board and optional redundant power supply.

Features:

- Modular 1RU design
- IP Network Grand Master Clock for NTP, PTP-IEEE1588, MASTER PCR, AVB-IEEE802.1AS, and SMPTE 2059-2
- 2 x 1000BASE-T RJ45 ports
- 2 x 10 GbE ports (SFP's are not provided and are optional)
- 6 independently timeable sync outputs, 8 with the +AUX option
- 4 optional SDI test generator outputs with the +SDI-TG option (supports SD/HD/3Gbs SDI)
- Optional 10 GbE video test generator support with the +10G-TG option (SFP's are not included)
- Configurable to run in Boundary Clock mode for larger enterprise scale network designs (with an upstream 5700MSC-IP Grand Master Clock)
- Can drive and interoperate with the sister product, the modular 7800SRG-IP, which is a PTP referenced SPG (to generate NTSC and PAL blackburst HD, and other bespoke analog reference signals.)
- GNSS referenced system capable of receiving GPS and GLONASS satellite constellation signals – outdoor antenna and 50ft cable provided.
- Optional 100ft, 400ft, 800ft, 1200ft and fiber optic extenders available for GNSS antenna
- All active components are front panel extractable & serviceable
- Optional dual power supply for redundancy (+2PS option)
- Full featured front panel control interface
- Contact closure output for critical warning (+AUX option)
- VistaLINK® control for device configuration and status monitoring
- Multi System GNSS referenced designs will be in sync and timed.
- An optional expansion module (+AUX option) provides AES & analog audio test generator, LTC, DARS, and GPIO functionality.
- An optional automatic changeover unit (5700ACO) provides automatic survivability changeover for baseband signals (video reference,wordclock, 10Mhz, LTC, DARS, and SDI test generators)

Ordering Options:

• +2PS	Redundant power supply
• +SDI-TG	4 outputs, configurable SD/HD/3G SDI test/black generators
• +10G-TG	Test generator outputs over 10 GbE ports and 4 SDI outputs, configurable SD/HD/3G SDI test/black generators (includes +SDI-TG option)
• +AUX	Includes expansion test module which provides AES and analog audio test generator, DARS, GPIO, and LTC outputs.

SFP Options:

• +SFP10G-TR13-A	1310nm laser, standard sensitivity 1310nm optical transceiver, 10km, single mode

Automatic Changeover Option:

- 5700ACO Automatic changeover unit (5700ACO) provides automatic survivability changeover for baseband signals (video reference,wordclock, 10Mhz, LTC, DARS, and SDI test generators)

1.1. QUICK START GUIDE

This section discusses the major steps in getting a new installation of a 5700MSC-IP up and running.

1.1.1. Mounting and Power Connections

The 5700MSC-IP chassis holds the main board, one power supply, and one fan module. Dual power supplies are an available option in which case a second power supply replaces the fan module. The chassis has built-in rack mounting ears and fits in a standard 19" rack. Two fans on each side cool the unit. Clearance of 2" (5cm) must be maintained around the fan exhausts on either side of the chassis. The power supply operates from an AC line frequency of 50Hz to 60Hz, at 100V-240V (auto-sensing). The fan module runs off of the single power supply. The power consumption of a 5700MSC-IP is 125 Watts with all options installed.

If dual power supplies are fitted, they should both be supplied with AC power. Each power supply has its own IEC C14 AC power inlet. The inlets are isolated from each other and can be powered by the same AC power source but ideally should be powered from different AC sources for true redundancy. If both supplies are not powered, the unpowered supply will trigger a system fault. A redundant power supply may be added at any time to a unit by removing the fan module and installing the second power supply.

The fan module is hot swappable and the power supplies are hot swappable when configured with dual power supplies. The fan module and power supplies can accessed from the front of the unit by removing the front panel. Each power supply and fan module has a Phillips mounting screw at the front that can be used to secure the module in order to prevent accidental removal.

1.1.2. Front Panel Installation

The 5700MSC-IP comes with a removable front panel that is equipped with two color LCD screens, along with 10 pushbuttons, and a control knob for navigating the menu system and configuring the unit. The front panel is secured by the two thumbscrews on either end. The front panel can be removed and re-installed while the unit is running to provide access to the power supplies and for troubleshooting purposes. When re-installing the front panel be sure to fully tighten the thumb screws.

Note: Care should be taken when handling the front panel to not inadvertently disconnect the ribbon cable connection on the 7800MSC-IP card or the 5700-AUX card.

When AC power is applied to the 5700MSC-IP and the power supplies are switched on, the unit will start up automatically. The front panel should become operative within approximately 30 seconds.

1.1.3. Configuring the Ethernet Ports

The 5700MSC-IP chassis houses a 7801FC-IRD frame controller board and a 7800MSC-10G master clock board. The 7800MSC-10G master clock board has five Ethernet interfaces. The two 1Gb/s and

two 10Gb/s ports are located on the rear plate of the 7800MSC-10G, while the frame Ethernet port shares the frame controller's Ethernet port, and hence the same IP subnet. Each of the master clock board interfaces must be configured with unique, valid IP addresses on separate IP subnetworks. Please refer to Figure 1-2 as an example of how this is done.

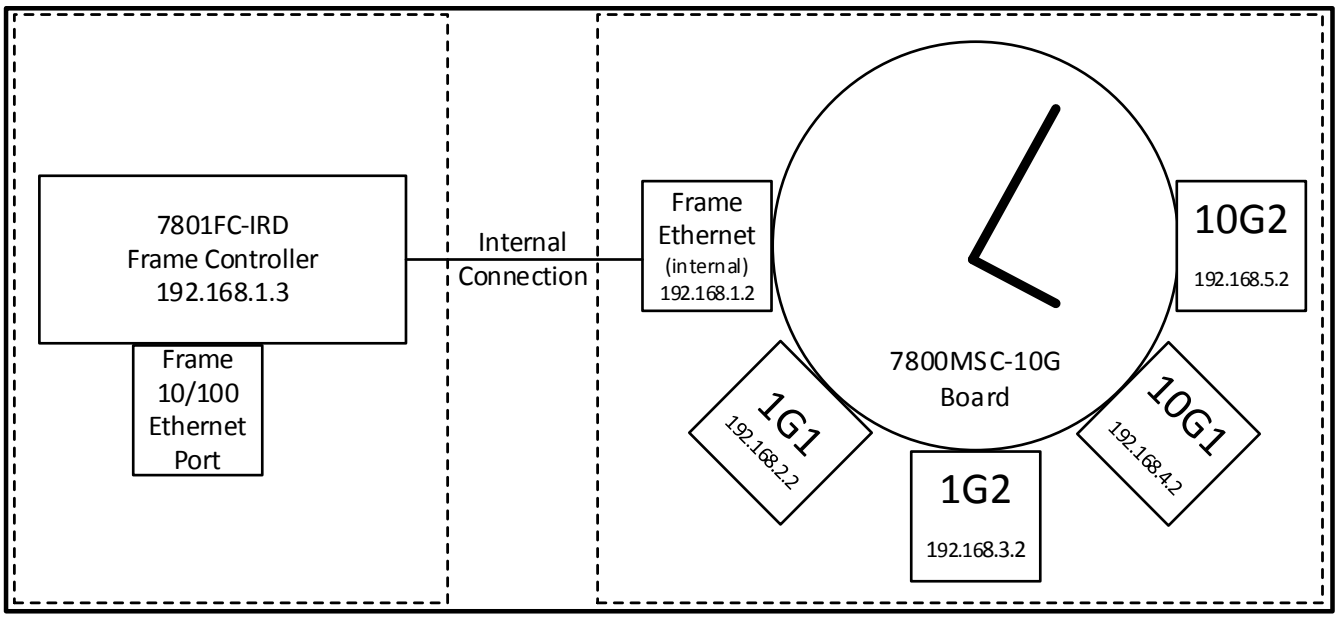

Figure 1-2: Ethernet Port Configuration

Press the **GENERAL** button on the front panel to access the general setup menu. This menu can be used to configure the two 1Gb/s Ethernet ports, the frame Ethernet port and the two 10Gb/s Ethernet SFP ports on the 5700MSC-IP. The 1GigE 1, 1GigE 2, 10GigE 1 and 10GigE 2 ports are used to carry mission-critical data, such as PTP, NTP and PCR. The frame Ethernet port is used for management purposes (VistaLink Pro, syslog, firmware updates, etc.).

The current menu selection will be indicated by the **>** character. Rotate the control knob or press the ↑ and ↓ buttons to select the *IP Control* menu item and press the **SELECT** button or depress the knob. Assign an unused IP address and subnet mask to the the two 1Gb/s Ethernet ports, the frame Ethernet port and the two 10Gb/s Ethernet SFP ports. The five ports must be on separate subnets in order to function properly. When entering an IP address, the control knob can be used to set each octet. Depress the control knob while turning to adjust in larger steps. The Ethernet link status and current IP settings can be viewed by pressing the **STATUS** button and selecting the the either of the two 1Gb/s Ethernet ports, the frame Ethernet port or either of the two 10Gb/s Ethernet SFP ports status screens.

If SNMP monitoring or control of the unit is desired, the SNMP feature must first be enabled (it is disabled by default). Select the **GENERAL** menu and press **ESC** to return to the root menu. Scroll down to *EngineeringMenu* and press **SELECT**. A password is required to enable the engineering menu items. Press **SELECT** on *Password* and use the ↑ and ↓ buttons or control knob to enter each digit of the numeric password and then press **SELECT**. The default password is 5700. The SNMP menu should now be accessible and SNMP can be enabled through *SNMP Ctl*. The trap addresses must be assigned if SNMP traps are required to be sent to remote logging software such as

VistaLINK® Pro. Contact Evertz customer service if a MIB to the 5700MSC-IP is required. Note that the Frame port should be used as the primary management interface.

If syslog event monitoring (requires syslog server, which is not included) is desired, the syslog server address must be configured, and syslog level 1 or syslog level 2 must be enabled. Select the **GENERAL** menu and press **ESC** to return to the root menu. Scroll down to *EngineeringMenu* and press **SELECT**. A password is required to enable the engineering menu items. Press **SELECT** on *Password* and use the ↑ and ↓ buttons or control knob to enter each digit of the numeric password and then press **SELECT**. The default password is 5700. The Syslog IP Address and Syslog Enable menu should now be accessible.

1.1.4. Selecting and Connecting the Frequency References

Pressing the **INPUT** button on the front panel will select the input menu. From here the frequency and time references of the unit can be configured. Use the control knob to select the *Frequency Ref* menu item and press **SELECT** or depress the knob. The *Reference Src* menu item selects six different ways the 5700MSC-IP can lock its master oscillator.

- ***GNSS Mobile*** – The 5700MSC-IP will look for a Global Navigation Satellite System (GNSS) antenna attached to the GPS port on the back of the unit. This mode is intended for applications where the location of the GNSS antenna is movable such as mobile production trucks. Start-up time before receiving data is optimized assuming the location may have changed from the previous time.

- ***GNSS Fixed*** – The 5700MSC-IP will look for a GNSS antenna attached to the GPS port on the back of the unit. This mode is intended for applications where the location of the GNSS antenna is fixed. Start-up time before receiving data will be longer the first time the unit is first powered up as the antenna determines the fixed location. Subsequent start-up times will be shorter as the unit assumes the location has not changed from the previous time.

The *GPS Enable* and *GLONASS Enable* menu items in the *Engineering Menu* control whether the receiver will lock to satellites from the GPS and/or GLONASS Global Navigation Satellite Systems.

With either the ***GNSS Mobile*** or ***GNSS Fixed*** menu choices, the ovenized oscillator inside the 5700MSC-IP will lock to the 1PPS pulse from the GNSS antenna. This provides a very accurate frequency reference to the unit. The high precision time and date provided by the GNSS antenna is used to phase the outputs of the 5700MSC-IP by referencing them to a specific point in GNSS time. Multiple 5700MSC-IP units locked to GNSS will all have the same phase on their outputs. This also means the time reference will be forced to GNSS.

- ***Ten MHz*** – The 5700MSC-IP will look for a 5MHz or 10MHz reference on its reference loop input, frame reference 1, or frame reference 2. The 5MHz/10MHz reference should come from a source that has higher stability than the internal oscillator of the 5700MSC-IP such as a Rubidium or Caesium frequency standard. A 5MHz or 10MHz reference does not provide any phase information and the phase of the outputs will not be the same between different 5700MSC-IP units.

- ***Video*** – The 5700MSC-IP will genlock to an analog black burst or HD tri-level reference applied to its reference loop input, frame reference 1, or frame reference 2. The frequency stability of

the 5700MSC-IP will be only as good as that of the reference input. The phase of the outputs will be aligned to that of the reference input.

- ***Internal*** – The 5700MSC-IP will free run on its internal high stability ovenized oscillator. Select this option if no external reference is available to the unit.

- ***1588*** – The 5700MSC-IP can synchronize with a PTP master to determine a frequency reference.

There are three other menu items that control how the 5700MSC-IP locks to its reference. These are *Genlock Range*, *Genlock Source*, and *Lock type*. Press the **HELP** button for a short description on what each menu item does.

1.1.5. Selecting and Connecting Time References

Once the desired frequency reference has been selected and the antenna/reference connections have been made, the time reference should be selected. The time reference is how the 5700MSC-IP obtains time and date for the system clock. Press the **INPUT** button to access the input menu. Return to the root level by pressing **ESC** a few times. Select the *Time* menu using the control knob and press **SELECT**. Use the *Reference Src* menu item to choose a time reference for the unit. There are other menu items that control how the 5700MSC-IP handles the time reference. Press the **HELP** button to identify the function of each item.

- ***GNSS*** – When a GPS or GLONASS receiver is connected to the unit, it can obtain continuous time and date updates from GNSS. If the frequency reference has been set to one of the GNSS modes, the time reference will also be forced to GNSS. However it is also possible to use a frequency reference other than GNSS (such as video) and still use GNSS as a very accurate time reference. See note above regarding GLONASS operation.

- ***VITC*** – The 5700MSC-IP will look for Vertical Interval Time Code on the selected line of a black burst signal that is applied to the reference loop input, frame reference 1, or frame reference 2. It can also decode date information from the user bits in several different formats. **In order to use VITC as a time reference, the frequency reference must first be set to *Video*.**

- ***None*** – The 5700MSC-IP will not acquire time from any outside source. The time and date must be manually entered using the front panel in the **GENERAL** menu. The high frequency stability of the unit and battery backup will ensure the 5700MSC-IP keeps fairly accurate time.

- ***SNTP*** – The 5700MSC-IP can synchronize once daily to time and date from an NTP server.

- ***1588*** – The 5700MSC-IP can synchronize with a PTP master to determine the time and date.

1.1.6. Configuring PTP

The 5700MSC-IP may be configured to provide Precise Time Protocol (PTP), which is designated as IEEE1588-2008, using the default IEEE1588 Annex J profile, the SMPTE 2059-2 Professional Broadcast Environment profile or the AES 67 profile. Furthermore, the 5700MSC-IP may be configured to function in roles of PTP GrandMaster, PTP Master, PTP Slave, and PTP Boundary Clock. The following sections outline configuration of each of the PTP parameters and options.

1.1.6.1. PTP All Ports Menu

To navigate to this menu, press the **GENERAL** button on the front panel of the 5700MSC-IP, then the **ESC** button to reach the top level of the menu. With the encoder knob, scroll down to the *PTP All Ports* submenu, and press the **SELECT** button. You will see a list of choices as shown below.

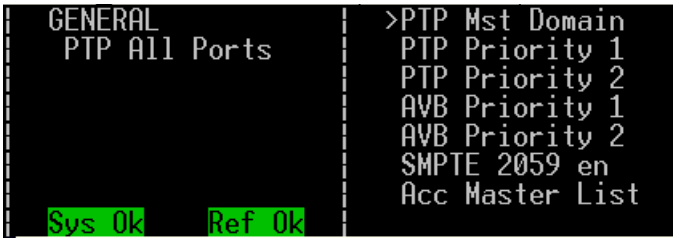

Figure 1-3: PTP All Ports Menu

This is where all PTP global options are set.

- Enter your PTP domain number (0 through 127) in the PTP Mst Domain submenu.
- Enter the PTP priority 1 and priority 2 values (0 through 255) in the respective submenus.
- Enter AVB priority 1 and priority 2 values (0 through 255) in the respective submenus.
- Set the SMPTE 2059 en to the respective sync spigot that you wish Sync Metadata to be based upon.

Set PTP Acceptable Masters if you wish to restrict PTP Masters that this unit will lock to. (An acceptable master is defined by its unicast IP address.)

1.1.6.2. PTP Port Specific (GigE 1, GigE 2, 10GigE 1, 10GigE 2, and Frame Ethernet) Settings

To navigate to this menu, press the **GENERAL** button on the front panel of the 5700MSC-IP, then the **ESC** button to reach the top level of the menu. With the encoder knob, scroll down to the PTP port that you wish to configure and press the **SELECT** button. You will see a list of choices as shown below.

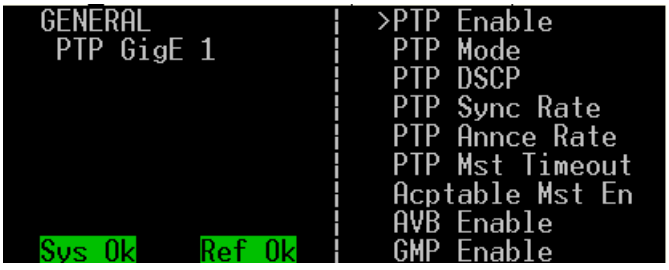

Figure 1-4: PTP GigE 1

- Enter the *PTP Enable* submenu to enable or disable PTP on the respective port (GigE 1 in Figure 1-4)
- Set the *PTP Mode* to the PTP Profile that you wish. The choices are IEEE1588 annex j, SMPTE 2059 and AES 67.
- Set the *PTP DSCP* to the value that you wish. The default for IP video networking is 56.
- Set the *PTP Sync Rate* to the value that you wish. This should be the same as other PTP devices on the same PTP network that this 5700MSC-IP will be communicating with via this port.

- Set the *PTP Announce Rate* to the value that you wish. This should be the same as other PTP devices on the same PTP network that this 5700MSC-IP will be communicating with via this port.
- Set the *PTP Master Timeout* to the value that you wish. This should be the same as other PTP devices on the same PTP network that this 5700MSC-IP will be communicating with via this port.
- Enter the *Acceptable Master Enable* submenu to specify whether this port will allow itself to become a slave to all other clocks that qualify, or to be restricted to the list defined in Section 1.1.6.1.
- Enter the *AVB Enable* submenu to turn AVB on or off for this port.
- Enter the *GMP Enable* menu to select which Sync spigot will be referred to for phasing purposes if an Evertz 5600GMP GrandMaster Proxy will be communicating with this port.

1.1.7. Configuring PCR

PCR configuration is done on a per-port basis: (GigE 1, GigE 2, 10GigE 1, 10GigE 2 and Frame Ethernet). To navigate to this menu, press the **GENERAL** button on the front panel of the 5700MSC-IP, then the **ESC** button to reach the top level of the menu. With the encoder knob, scroll down to the PCR port that you wish to configure and press **SELECT**. You will see a list of choices as shown below.

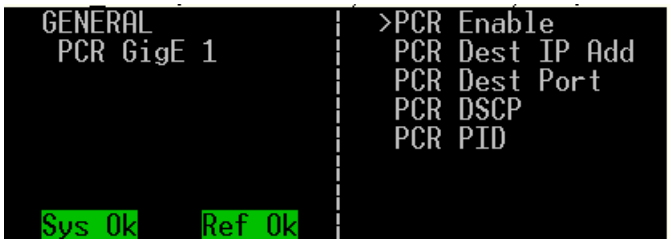

Figure 1-5: PCR GigE 1 Menu

- Enable or disable PCR with the *PCR Enable* submenu.
- Set the PCR multicast address with the *PCR Dest IP Add* submenu.
- Set the PCR port number with the *PCR Dest Port* submenu.
- Set the PCR DSCP value with the *PCR DSCP* submenu. (56 is the default value for IP Video networks.)
- Set the PCR PID value with the *PCR PID* submenu.

1.1.8. Checking the Status of the Unit

After the input references are connected and set up, the status of the unit can be checked by pressing the **STATUS** button on the front panel. There are several different status screens which can be selected by using the control knob or the ↑ and ↓ buttons. The status of the frequency and time references can be viewed by choosing the *Lock status* screen and pressing **SELECT**. Press **ESC** to return to the status menu to select another screen for viewing. Any screen name that is highlighted with a red or yellow background indicates that one of the statuses in that screen is in a fault or warning condition.

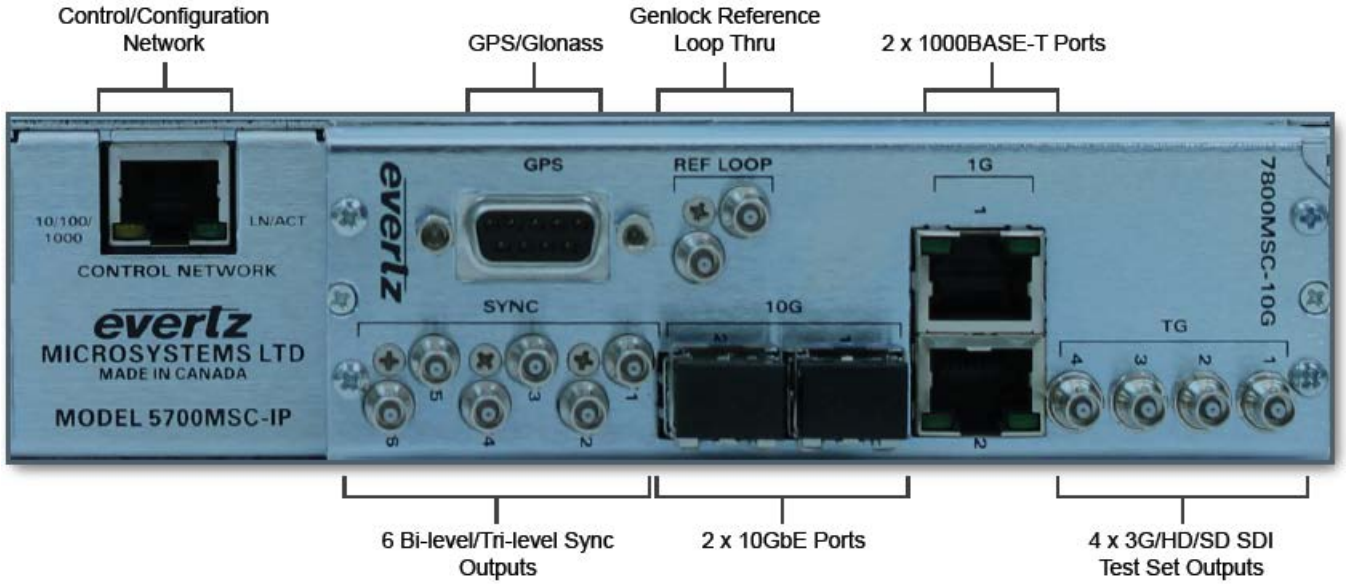

Figure 1-6: 5700MSC-IP Rear Panel View

1.1.9. Wiring the Outputs

Most outputs are provided as HD-BNC connectors and wiring is straightforward. The GigE 1 and GigE 2 ports use a standard RJ-45 connector, and the 10GbE ports require an SFP10G-TR13-A (not included).

1.1.10. Configuring the Sync Outputs

The sync outputs of the 5700MSC-IP are configured in the **OUTPUT** menu, accessed by pressing the **OUTPUT** button. All sync outputs are derived from the master oscillator and will be locked in frequency and phase. The sync outputs are all programmable to output several different sync types and can be phased independently from each other.

In the **OUTPUT** menu, the sync outputs are configured using the *SYNC 1* to *SYNC 6* sub-menus. Each sync output can set to output any number of black burst or HD tri-level standards. They are all phased independently. When configuring a sync output, the mode must be selected first. By default, the mode of all sync outputs are set to NTSC-M black burst for North American units, and PAL-B black burst for European units. Configure the mode of each sync output to the format desired for the installation. Note that with +AUX option, the 10MHz and WC outputs may also be configured as sync outputs.

There are numerous other configuration settings for each sync output, some may be disabled (dark text) or enabled (white text) depending on the output mode selected. Scroll over each of the available menu items and press the **HELP** button for more information on the function of each menu item.

1.1.11. Configuring the Test Generator Outputs

The unit has been equipped with four SDI video test generators on HD-BNC outputs. Each generator can output a number of **SDTG**, **HDTG**, or **3GTG** options. These are configured in the *TG 1*, *TG 2*, *TG 3*, and *TG4* menus. If the 4K Test Generator Option is installed, these four SDI spigots may be configured to act together for a quad-link, single Ultra HD Test Generator (Square Division) or a quad-link, single 2SI Test Generator (Sequential Interleave); when this is done, all four links are controlled by SDI TG 1. All test generators are derived from the master oscillator and will be automatically locked in frequency and phase. The test generators are independent from one another and can be configured to different formats and different phase offsets. By default, all phases will be aligned to the selected frequency reference.

The unit also has two 10GbE ports that can output test generators if the +10G-TG option is ordered. Each 10GbE port can output 3 test generators, which can be configured in the *TG 5, IP 1a*; *TG6, IP1b*; *TG7, IP1c*; *TG8, IP2a*; *TG9, IP2b*; and *TG10, IP 2c* menus. Encoding options include SMPTE 2110 and ASPEN, based on the firmware that is installed.

The quickest and easiest way to discover how to configure the outputs is to scroll through the available menu items and press the **HELP** button for a description of each menu item function.

1.1.12. Configuring the Time Outputs

All time outputs from the unit come from the System Time clock. This clock can be viewed by pressing the **STATUS** button and selecting the *System/In time* screen. When the time reference is obtained from a GNSS sources, the system time will be Coordinated Universal Time (UTC). UTC time is the same at all locations around the world.

In order to output local time, the Time Zone must be selected to match the time zone offset of your location. For example, in North America, Eastern Standard Time (EST) is UTC –5:00 hours. Central Standard Time (CST) is UTC –6:00 hours. Mountain Standard Time (MST) is UTC –7:00 hours. Pacific Standard Time is UTC –8:00 hours. The 5700MSC-IP also supports Daylight Savings Time, which must be enabled separately for each time output. Below are descriptions of the time outputs available from the 5700MSC-IP.

- ***Sync Outputs*** – When a Sync output mode is set to NTSC-M or PAL-B black burst, VITC time can be inserted onto two lines in the vertical blanking interval. The VITC is controlled by the *Vitc Ctl*, *Vitc Line 1*, *Vitc Line 2*, *Dropframe Ctl*, *Color Frame*, *Set Jam Time*, *Jam Output*, *Jam all Vitc*, *Time offset*, *Time Zone*, and *DST enable* menu items.

- ***Server Protocols*** – The 5700MSC-IP will support Network Time Protocol and Precision Time Protocols. These are configured by pressing the **GENERAL** button and entering the *NTP rules*, *PTP All ports, PTP GigE 1, PTP GigE 2, PTP 10G 1, and PTP 10G 2* sub-menus. The 5700MSC-IP hosts an NTP server and also sends out periodic NTP broadcasts. NTP time should always be UTC. PTP broadcast rates are determined using the PTP sub-menus listed above.

- ***Test Generator Outputs*** – Timecode can be “burned-in” at the bottom of any of the the 5700MSC-IP test signal outputs. These are configured by pressing the **OUTPUT** button and entering the appropriate TG menu. The time is controlled by the *TC Burn In*, *Dropframe Ctl, Set Jam Time, Jam Output, Jam all VitcLtc, Time Offset*, *Time Zone*, and *DST enable* sub-menu items.

1.1.13. Final Steps of Set Up and Securing All Connections

Once the 5700MSC-IP has been configured, the various *STATUS* screens should be checked to ensure there are no items displayed with a red or yellow background. The left LCD screen should show Sys **OK** and **Ref OK** with a green background in the bottom corners.

The power supply and fan modules (accessed by removing the front panel) should be secured to the chassis by fastening the Phillips mounting screw. The GPS D-Sub connector on the back of the unit should be secured to the 5700MSC-IP using mounting screws. The AC power cords can be fixed to the unit using the retaining clips provided.

1.1.14. Access Control

The engineering menu password can be changed from the default to prevent unauthorized tampering of SNMP and menu access control settings. The *SNMP Ctl* menu item can be changed to *SNMP off* or *SNMP status* to prevent remote SNMP control of the unit. Furthermore, pressing the **PANEL LOCK** button can lock the front panel. This prevents accidental changes by someone bumping or leaning into the front panel. The front panel can be unlocked by pressing the **SELECT** and **PANEL LOCK** buttons simultaneously.

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2. TECHNICAL SPECIFICATIONS

2.1. ANALOG SYNC OUTPUTS

Output Standards:

Black Burst:	SMPTE ST 170 (NTSC-M), ITU-R BT.1700-1 (PAL-B)
Bi-Level:	Slo-Pal 625i/48, 625i/47.95, 480p/59.94
HD Tri-Level:	SMPTE ST 274 (1080p/23.98, 1080p/24, 1080i/50, 1080i/59.94, 1080i/60, 1080p/23.98sF, 1080p/24sF, 1080p/25, 1080p/29.97, 1080p/30, 1080p/50, 1080p/59.94, 1080p/60) SMPTE ST 296 (720p/59.94, 720p/60, 720p/50, 720p/30, 720p/24)
Pulse Signals:	PAL color frame, 1Hz pulse, IRIG DATUM 1/1.001Hz pulse, 6/1.001Hz pulse
CW Signals:	5MHz, 10MHz, NTSC-M Subcarrier, PAL-B Subcarrier
Wordclock:	48kHz Wordclock Level 5V CMOS (1kΩ) or ±1V (75Ω)
10MHz Output:	1.0V p-p, 2.0V p-p, in 75Ω, SNR > 70dB rms SFDR > 50dBc
Connector:	75Ω HD-BNC, bayonet positive locking (Amphenol)
Number of Outputs:	6
DC Offset:	0V ±0.05V
Return Loss:	> 40dB up to 10MHz
SNR:	> 75dB rms
Output Levels:	1.0V p-p, 2.0V p-p, in 75Ω, selectable

2.2. GPS/GLONASS RECEIVER

Temperature:	-40°C to +70°C
Humidity:	95% R.H. Condensing at 60°C

2.3. 1000BASE-T NETWORK

Quantity:	2
Network Type:	IEEE 802.3 (10BASE-T), IEEE 802.3u (100BASE-T), IEEE 802.3ab (1000BASE-T)
Connector:	RJ-45
Timing:	NTP, PCR, AVB (IEEE802.1AS), IEEE1588 (annex J), SMPTE 2059-2, AES67

2.4. 10GBE TIMING NETWORK

Quantity:	2
Network Type:	IEEE 802.3ae (10GbE)
Connector:	SFP (not included), LC/UPC
Timing:	NTP, PCR, AVB (IEEE802.1AS), IEEE1588 (annex J), SMPTE 2059-2, AES67

2.5. GENLOCK INPUT (VIDEO/10MHZ SELECTABLE)

Type:	Autodetects standard SMPTE ST 170 (NTSC-M), ITU-R BT.1700-1 (PAL-B), Color Black 1V p-p with optional VITC and 10-

	field pulse HD Tri-level Sync (same HD standards as sync outputs)
Number of Inputs:	2 Loop thru
	High impedance, isolated, differential external termination required
Connector:	75 Ω HD-BNC, bayonet positive locking (Amphenol)
Return Loss:	>40dB to 10MHz (with external 75Ω termination)
Input Level Range:	
Video:	-3.5dB (double-terminated) to +6dB (un-terminated)
10MHz:	0.3V p-p to 4.0V
Frequency Lock Range:	
Wide mode:	±15ppm min
Narrow mode:	±0.1ppm min

2.6. SDI TEST GENERATORS (WITH +SDI-TG, OR +10G-TG OPTIONS)

Standards:	With SDI-TG option SMPTE ST 259-C (270Mb/s),
	With HDTG option, SMPTE ST 259-C (270Mb/s), SMPTE ST 292-1 4:2:2
	With 3GTG option, SMPTE ST 259-C (270Mb/s), SMPTE 292-1 4:2:2, SMPTE 372 dual link, and SMPTE ST 424
	For SMPTE ST 2048-2 and SMPTE ST 2036-1 2160 line formats
	Quad link SMPTE ST 292-1 4:2:2, Quad link SMPTE ST 424 4:2:2
	SMPTE ST 425-3 Dual link 3Gb/s, SMPTE ST 425-5 Quad link 3Gb/s
Number of Outputs:	4
Embedded Audio:	Up to 4 audio groups as specified in SMPTE ST 299-1 or SMPTE ST 272
	Selectable tone frequencies (from 20Hz to 12kHz) and audio group
Connector:	75Ω HD-BNC, bayonet positive locking (Amphenol)
Signal Level:	800mV nominal drive
DC Offset:	0V ±0.5V
Rise and Fall Time:	100ps HD/3G, 600ps SD
Overshoot:	< 10% of amplitude
Jitter:	< 0.2 UI
Return Loss:	> 15dB to 1.5GHz
	> 10dB to 3GHz

2.7. PHYSICAL

Dimensions:	19” W x 1.75” H x 11.5” D
	(483mm W x 45mm H x 292mm D)
Weight:	8lbs (3.5kg)

2.8. ELECTRICAL

Voltage:	Auto ranging 100 to 240V AC, 50/60Hz
Configuration:	Optional redundant supply available
Power:	125W (all options installed)
Safety:	TüV Listed
	Complies with EU safety directives
EMI/RFI:	Complies with FCC Part 15 Class A
	Complies with EU EMC Directive

2.9. +AUX EXPANSION MODULE OPTION (AES & ANALOG AUDIO TEST SET, DARS, GPIO, AND LTC)

2.9.1. LTC Outputs

Standard:	SMPTE ST 12-2 or IRIG-B
Frame Rate:	24, 25, 30 and 29.97 (drop frame and non-drop frame)
Number of Outputs:	2 balanced
Connectors:	Female DB-15
Level:	
Unpowered:	Adjustable, 1.0V to 8.0V p-p, balanced
Output Impedance:	44Ω balanced (un-powered)
Rise Time:	40 ±10µs
Jitter:	< 2µs

2.9.2. DARS & AES Test Generator Outputs:

Standard:	
Unbalanced:	SMPTE ST 276-1 single ended AES (24-bits) (1V p-p into 75Ω)
Balanced:	AES3 (24-bits)
Number of Outputs:	
DARS:	1 unbalanced, 1 balanced
AES Test Gen:	2 unbalanced, 2 balanced
Connector:	
Unbalanced:	BNC per IEC 61169-8 Annex A
Balanced:	Removable Terminal Strip
Sampling Rate:	48kHz
Impedance:	
Unbalanced:	75Ω unbalanced
Balanced:	110Ω balanced
AES Tones:	Menu selectable

2.9.3. Analog Audio Tone Generator

Number of Outputs:	2
Type:	Balanced analog audio
Connector:	6 pins on 16-pin removable terminal strips
Output Impedance:	66Ω
Signal Level:	-30 to +10dBu into 10kΩ load
DC Offset:	< 10mV
Noise Floor:	< -90dBu, unweighted
THD+N:	< -100dB with 1kHz @ +10dBu into 10kΩ load

2.9.4. General Purpose Inputs and Output

Number of Inputs:	2
Number of Outputs:	2 (function menu selectable)
Output Type:	Opto-isolated, active closure to GND, 20kΩ pull-ups to +5V
Input Type:	Opto-isolated, senses closure to GND, pull-ups to +5V
Connector:	4 pins plus 2 ground pins on DB-15 female

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3. THEORY OF OPERATION

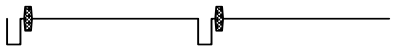
The 5700MSC-IP is equipped with six programmable sync outputs along with a 10MHz and a Wordclock output. When equipped with a test generator option (+SDI-TG, +10G-TG, +AUX), analog/digital audio and analog/digital video outputs will be available.

3.1. OUTPUTS

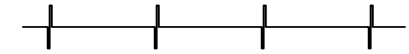
3.1.1. Sync Outputs

The sync output section provides six sync outputs along with a 10MHz and a Wordclock output. The 10MHz and Wordclock outputs can be configured as additional sync outputs, if required. All sync outputs are generated from the master oscillator and will be locked in frequency to the selected reference. Most sync output types will be phase locked to the reference, depending on the reference type and the phase information supplied. When a video sync mode is selected, an independent phase offset can be applied to the output. The sync outputs are configured from the **OUTPUT** root menu.

All sync outputs are fully programmable to output several different sync formats by changing the sync mode. The different output modes are described below.

Black Burst Signals 	
NTSC-M PAL-B	There are two color black output modes, one in NTSC-M format and the other in PAL-B format. These modes are referred to as “black burst” or “color black” because they contain black video and have a colorburst to provide a colorframe reference. Vertical Interval Time Code (VITC) can be inserted on up to two lines in these modes. Additionally, a SMPTE ST 318 ten-field reference can be inserted onto line 15 for the NTSC-M output mode. Both these outputs modes can be phased independently over the entire color frame sequence.

HD Tri-Level Signals

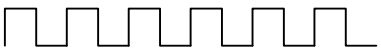


North American 1080i/60 1080i/59.94 1080p/60 1080p/59.94 1080p/30 1080p/29.97 720p/60 720p/59.94 720p/30	Analog tri-level sync output modes are available for a variety of HD formats. These outputs are generated according to SMPTE ST 274 and SMPTE ST 296. All tri-level sync formats can be phased independently. If the 1035i/59.94 format is required, select 1080i/59.94. These sync formats are identical to each other. Similarly, if 1035i/60 is required, select 1080i/60. The 1080p/30sF, 1080p/29.97sF, and 1080p/25sF sync formats are identical to the 1080i/60, 1080i/59.94, and 1080i/50 output modes available here. The 1080p/60, 1080p/59.94, and 1080p/50 sync formats can be used for 3G 1080p synchronization, but contain no field information. The 1080i/60, 1080i/59.94, and 1080i/50 formats should be used instead, whenever possible.
European 1080i/50 1080p/50 1080p/25 720p/50	
Film Standards 1080p/24 1080p/24sF 1080p/23.98 1080p/23.98sF 720p/24	

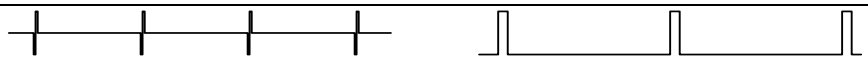
Continuous Wave (CW) Signals

10MHz 5MHz NTSC-M Subcarrier PAL-B Subcarrier	The continuous wave (CW) output modes produce a sine wave at a specific frequency. The 10MHz and 5MHz outputs are locked in frequency to the reference but are not phased with respect to the reference. The NTSC Subcarrier (3.579MHz) is phase locked only when using either GNSS or NTSC black burst as a reference. It will be inverted (180º out of phase) with respect to a proper NTSC subcarrier and is better described as a “burst-locked sinewave”. The PAL Subcarrier (4.434MHz) is phase locked only when using GNSS or PAL black burst as a reference. It is generated at sine (U) phase.

Wordclock



Wordclock	The wordclock output mode produces a square wave at 48kHz. It is high during subframe1 (left channel) and low during subframe2 (right channel). Sync outputs that are set to wordclock cannot be independently phased. There is a single global wordclock phase control in the *AES Audio* menu. The wordclock output amplitude is set with the *Wordclock level* menu item.

Pulse Signals 	
1Hz 1/1.001Hz 6/1.001Hz PAL Colorframe IRIG1 Datum	The pulse output modes provide timing pulses that can be used to lock downstream equipment or can be helpful for troubleshooting purposes. These outputs cannot be phased and always remain phase-locked to the frequency reference. These signals may not be affected by any global phase offset. The pulse type is set with the *Pulse type* menu item. Refer to the pulse diagrams in Figure 3-1 and Figure 3-2 for timing relationships. The 1Hz pulse goes high at the beginning of each second. The 1/1.001Hz pulse indicates the start of the second for 29.97Hz LTC/VITC rates and is also synchronized to NTSC color field 1. Will be high for the duration of NTSC color field 1. The 6/1.001Hz pulse indicates where 59.94Hz video coincides with the 23.98Hz standards. This pulse is only phase locked when using a GNSS reference or NTSC with a ten-field pulse. The PAL Colorframe pulse will be high during PAL color field 1. It will only be phase locked when referenced to GNSS or a PAL-B reference. The IRIG1 Datum pulse will go high at the start of the IRIG second for 100ms. This pulse will be aligned within 20 microseconds of the GNSS 1PPS pulse when locked to a GNSS reference.
Bi-Level 	
625i/48 625i/47.95 480p/59.94	The slo-PAL sync output modes use the PAL video format but run at a slower frame rate to be synchronous with 24Hz and 23.98Hz film standards. These output modes consist of sync pulses only and do not have a colorburst. These outputs can be phased independently. Note that VITC cannot be inserted onto slo-PAL outputs.

3.1.2. Test Generator Options

A variety of audio and video test generators are available.

+SDI-TG and +10G-TG Options:

- Serial Digital Interface Test Generators (SDI TGs). There are four independent test generators. The SDI-TG option provides the capability to generate Standard Definition formats. The HDTG option adds the ability to generate High Definition formats. The 3GTG option adds the ability to generate 3G formats as well as dual-link formats. The 3GTG option also includes 3D test patterns in various formats. All test generators have an audio embedder and can generate audio tones in up to four groups of audio. They also feature a 2-line configurable on-screen message display and timecode burn-in window at the bottom of the image.

+AUX Option:

- Analog Audio test generators. Two channels, Left & Right. Supplied as balanced outputs on the AUDIO terminal block. Can be configured to output continuous, or timed audio tones.
- Digital Audio test generators. Two AES outputs with configurable audio tones and a silent DARS output. Provided as unbalanced outputs on HD-BNC connectors and also as balanced, isolated outputs on the AUDIO terminal block.

3.1.3. Global Pedestal Control

There is a single control to enable or disable applying 7.5IRE setup to all sync outputs. This control only affects the NTSC-M output format. This control is located in the **OUTPUT** root menu.

3.1.4. Global Phase Controls

The Global Phase feature of the 5700MSC-IP provides a single point of control from which all video outputs can be phased simultaneously. There are separate controls for each of the frequency lock modes (GNSS+, Video, 10MHz, and Internal) to allow different phase offsets to be applied depending on the lock source. This global phase allows for phase correction to be applied when locking to a 10MHz reference.

The “10MHz” and “Internal” global phase settings are reset to zero at startup. This is done because no phasing information is supplied in these reference modes and the phase of the outputs will be random when the unit is restarted.

Once enabled, the global phase offset can be specified in milliseconds, microseconds, and nanoseconds. The global phase offset is applied before the individual phase controls for each output. Refer to Table 3-1 for a list of all the outputs affected and the minimum phasing resolution for each. The outputs unaffected by global phase will remain locked to the reference. The Global Phasing menu in the **OUTPUT** root menu is used to configure global phase.

Output	Affected by Global Phase	Minimum Phasing Resolution
Sync – NTSC & PAL modes	Yes	1 ns
Sync – Tri-level modes	Yes	1 ns
Sync – 5MHZ/10MHZ CW modes	No	-
Sync – NTSC/PAL subcarrier modes	No	-
Sync – PAL Color Frame Pulse	No	-
Sync – 1Hz and 1/1.001Hz Pulses	No	-
Sync – 6/1.001Hz pulse	No	-
Sync – Wordclock	Yes	59 ns
IRIG Datum Pulse	Yes	1 ms
AES/DARS outputs **(+AUX Option only)**	Yes	163 ns
LTC outputs **(+AUX Option only)**	Yes	1 us
SDI TG outputs **(+SDI-TG and +10G-TG Options only)**	Yes	37 ns SD 13.5 ns HD & 3G

Table 3-1: Global Phasing Characteristics

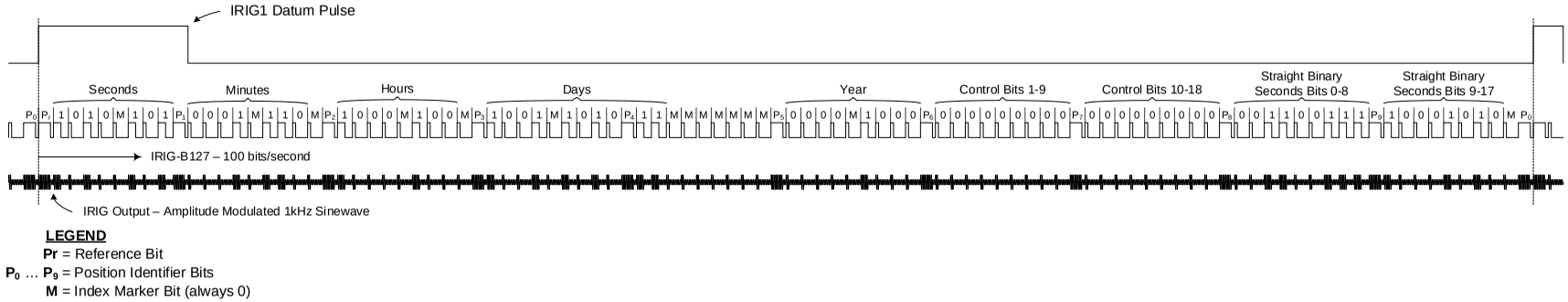


Figure 3-1: IRIG-B127 Format and Alignment to IRIG1 Datum Pulse

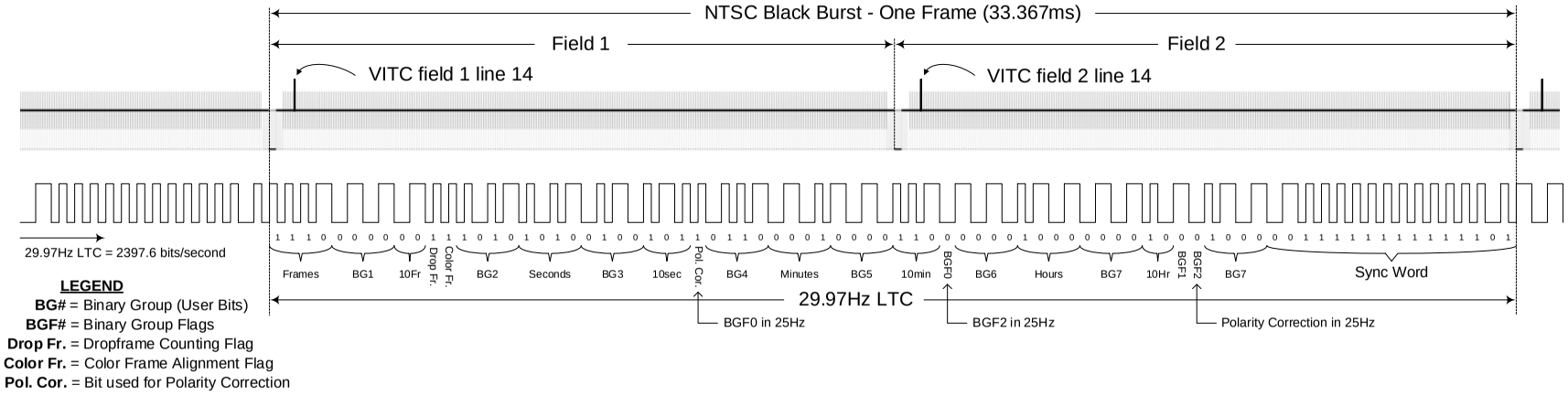


Figure 3-2: 29.97Hz LTC Format and Alignment to NTSC Video

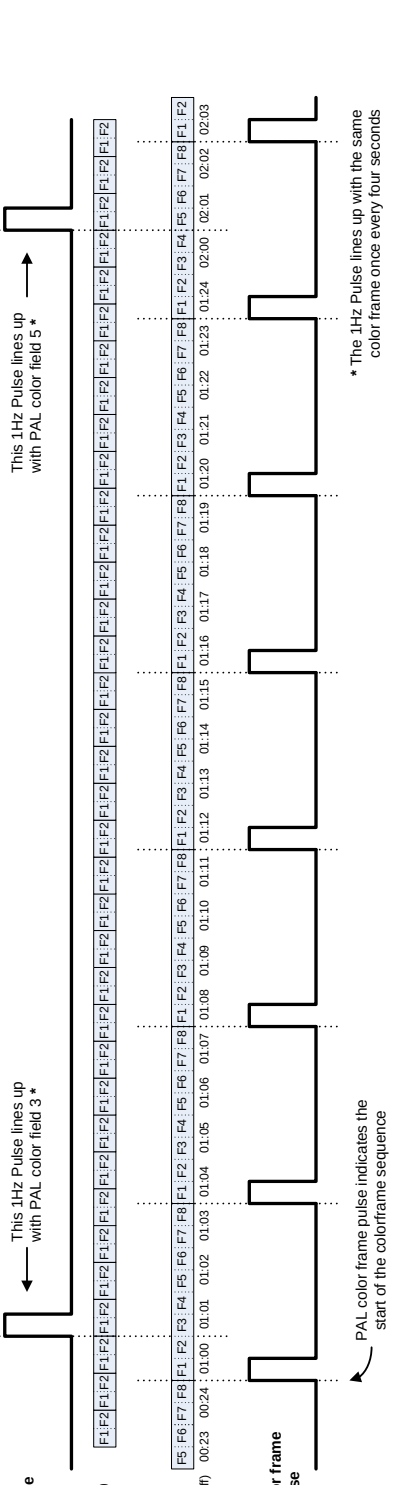


Figure 3-3: PAL Alignment to 1Hz Pulse and PAL Color Frame Pulse

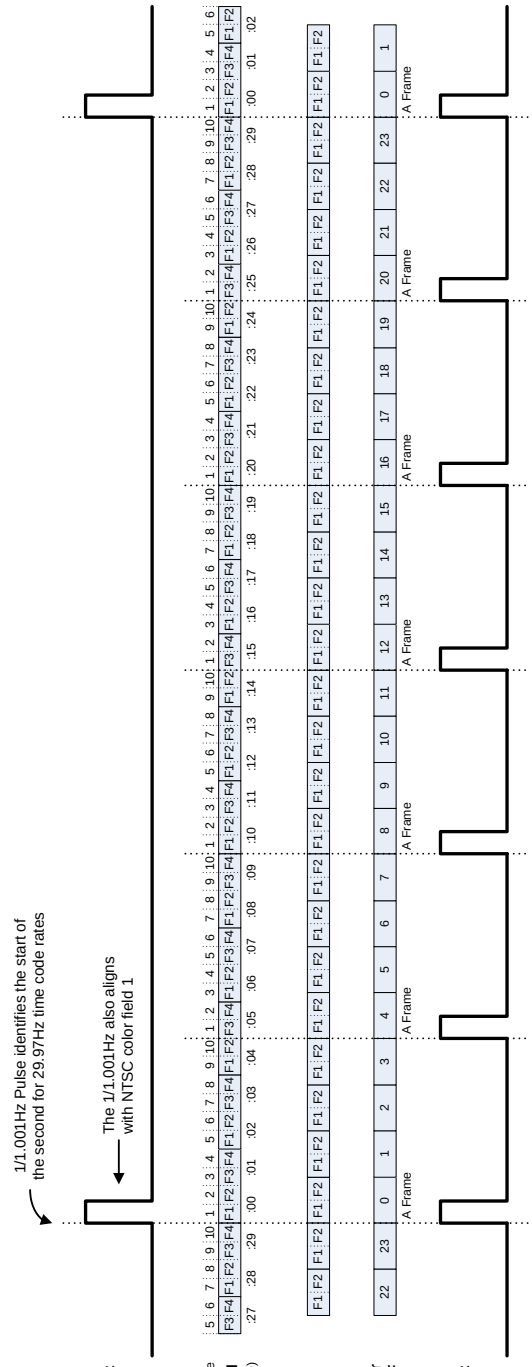


Figure 3-4: NTSC Alignment to 1/1.001Hz Pulse and 6/1.001Hz Pulse with VITC Color Framing

3.2. GENLOCK

3.2.1. Frequency Locking

At the heart of the 5700MSC-IP is the master oscillator circuit. Refer to the block diagram in Figure 3-5 below. For maximum versatility and reliability, two separate oscillators are employed. In *narrow* mode, an ovenized quartz oscillator (OCXO) is used for maximum stability. In *wide* mode, a voltage controlled oscillator (VCXO) provides a wide lock range and fast lock times. For added reliability this dual configuration allows the unused oscillator to act as a backup to the active oscillator. In the case of a hardware fault the backup oscillator will take over.

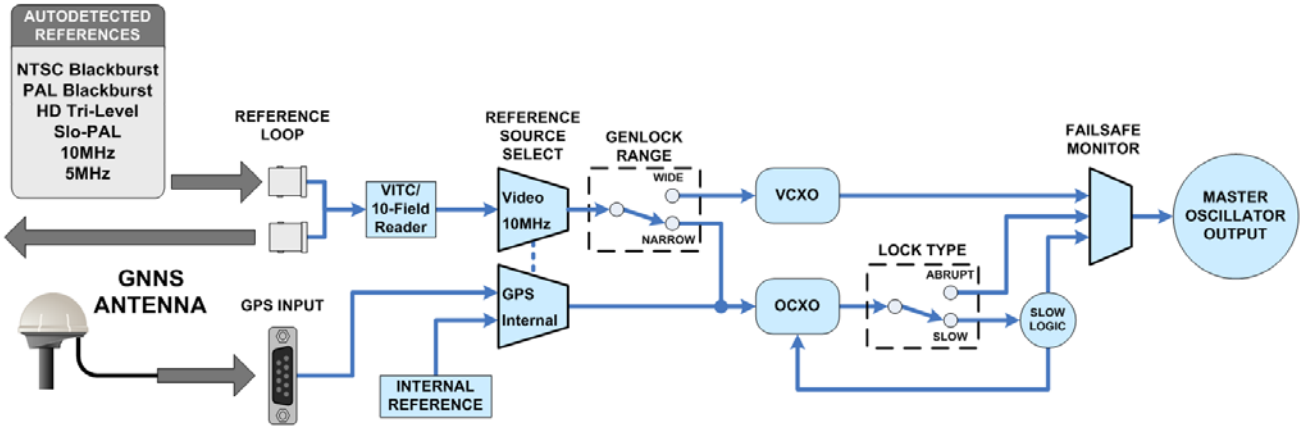


Figure 3-5: Main Oscillator Circuit Block Diagram

The 5700MSC-IP can be configured to free-run on its internal reference, or it can lock its oscillator to an available frequency reference. This locking operation uses a Phase Lock Loop (PLL) to continuously adjust the oscillator to track the frequency and phase of the reference signal. In *narrow* mode an additional feature is available whereby the adjustment rate of the oscillator is limited to prevent sudden changes during a re-locking operation (see *Slow* mode in section 3.2.4). The 5700MSC-IP can lock to several different frequency reference types. The supported signal types are shown in Table 3-2. Video and Continuous Wave (CW) signals are applied to the frame reference 1 BNC, frame reference 2 BNC or reference loop HD-BNCs and are auto-detected. A GNSS receiver can also be connected to the unit and used as a frequency reference (see section 3.5). Each reference type is explained in detail in the following sections.

Reference	Lock Type	Phase Lock Period	Lock Diagram	Lock Range
NTSC	Sync edge/burst	2 Color Frames	Figure 3-6	Wide/Narrow
NTSC+10field	Sync edge/burst	5 Frames	Figure 3-7	Wide/Narrow
PAL	Sync edge/burst	4 Color Frames	Figure 3-9	Wide/Narrow
HD Tri-Level	Sync edge	1 Frame	Figure 3-10	Wide/Narrow
Slo-PAL	Sync edge	1 Frame	-	Wide/Narrow
10MHz CW	Edge	None	Figure 3-11	Wide/Narrow
5MHz CW	Edge	None	Figure 3-11	Wide/Narrow
GNSS	1pps edge	4004 PAL frames/ 4800 NTSC frames	Figure 3-12	Narrow only
Internal Ref	Free-run	None	Figure 3-11	Narrow only

Table 3-2: Frequency Reference Types for the 5700MSC-IP

3.2.2. Selecting the Frequency Reference Type

The frequency reference for the 5700MSC-IP is selected with the *Freq Reference Src* menu item in the *Frequency Ref* menu off the **INPUT** root menu. When *GNSS* is selected, the 5700MSC-IP will use the GNSS receiver attached to the GPS port on the rear of the unit (see section 3.2.13). When set to *Ten MHz*, the 5700MSC-IP will look for a 5MHz or 10MHz continuous wave (CW) signal on the frame reference 1 BNC, frame reference 2 BNC or reference loop input HD-BNCs (see section 3.2.12). When set to *Video*, the 5700MSC-IP will lock to an analog video sync signal (auto-detected) that is applied to frame reference 1, frame reference 2 or the reference loop HD-BNC connectors (see section 3.2.5). When set to *Internal*, the 5700MSC-IP will free-run off its internal reference (see section 3.2.12.1).

The *Inputs* status screen in the **STATUS** root menu can be used to view which frequency references have been detected by the 5700MSC-IP. The first three lines indicate status of video sync, 5MHz or 10MHz detection, and GNSS status.

3.2.3. Selecting the Genlock Range

The *Genlock Range* menu item in the *Frequency Ref* menu selects which oscillator is used when locking to a video sync or CW reference. When *Narrow* is selected, the high-stability oven controlled quartz oscillator (OCXO) is used and the VCXO runs as backup. When *Wide* is selected, the voltage controlled quartz oscillator (VCXO) is used and the OCXO runs as backup. It should be noted that when the frequency reference source is set to *GNSS* or *Internal Ref*, the genlock range is forced to *Narrow* mode (OCXO) regardless of this menu setting.

In the event that the frequency reference is lost, the 5700MSC-IP will free-run using the selected oscillator. The *Narrow* range OCXO has extremely high stability which will translate to very low drift. This also translates into lower jitter on the outputs. Another advantage of the *Narrow* range is that it allows use of the *Slow* re-lock mode that prevents glitches when re-locking to a reference (see section 3.2.4). The disadvantages of the Narrow range are that it requires a very tight reference source (±0.1 PPM) and requires a longer time to fully lock. The OCXO also requires five minutes of warm-up time before reaching full stability once the unit has been powered on.

The Wide range VCXO provides very fast lock times with a wide lock range (±15 PPM) which means it can lock to just about any reference signal. It can be useful if the 5700MSC-IP reference source changes frequently such as in a post-production facility. The *Wide* range cannot be used when locking to GNSS or when free-running on the internal reference. In almost all cases, the *Narrow* range is superior and should be left as the default selection.

In the event that the frequency reference is lost when locked in *Wide* mode, the 5700MSC-IP will freerun on its VCXO. Note that this oscillator can freerun at a frequency outside the *Narrow* mode lock range which may cause problems for downstream 5700MSC-IP units. The Wide oscillator is also capable of going beyond the frequency tolerance specifications stated in ITU-R BT.601 and SMPTE ST 292-1. Operating outside the range of ±10ppm may cause locking issues for downstream equipment.

Genlock Range	Oscillator	Lock Range	Time to Lock	Jitter	Free-run Drift
Narrow	OCXO	± 0.1 PPM	>20 seconds	very low	very low
Wide	VCXO	± 15 PPM	<1 second	Low	moderate

Table 3-3: Genlock Range Characteristics

The status of the reference and lock progress can be monitored on the *Lock Status* screen, accessed by pressing the **STATUS** button and selecting *Lock Status*. The current position within the tuning range of the selected oscillator is shown as *OCXO center* or *WIDE center*. It is displayed as a percentage (+100% to –100%) of the total tuning range. This reading gives an idea of how close to the edges of the tuning range the oscillator is when locked to a reference.

The *Narrow* range OCXO oscillator ages over time and the center frequency may drift. It is important that despite any drift it retains the ability to lock to a precision frequency source such as GNSS or a rubidium/cesium frequency standard. Such frequency sources are extremely accurate. The oscillator is guaranteed from the factory to lock to such a reference within ±10% of the center of its tuning range. The aging of the oscillator is 10% maximum for the first year, and 5% for every year thereafter. This translates to an expected lifetime of 15 years. If the oscillator locks at over ±90% of its tuning range, a warning condition will be indicated and the status line will be shown in Red. Keep in mind that the *OCXO center* value is only meaningful when locked to a very accurate frequency reference.

The 5700MSC-IP monitors the condition of both oscillators at all times. If an oscillator problem is detected, the unit will seamlessly switch to the unused oscillator and report an internal hardware fault. This will activate the *Hw Fail* message on the front panel and can also send out an SNMP trap. If such a fault occurs, it is not advisable to power down or attempt to restart the unit. Contact Evertz customer service for further assistance at +1 905-335-7570 or see www.evertz.com/support.

3.2.4. Lock Type Selection

When the *Genlock Range* is set to *Narrow*, the *Lock Type* controls how the 5700MSC-IP will respond when its oscillator becomes out of sync to the frequency reference. This situation can occur if the incoming frequency reference changes or is reconnected after a period of absence long enough that the 5700MSC-IP oscillator has drifted and is no longer synchronized. There are two lock types available: *Slow* and *Abrupt*.

In the *Abrupt* mode, the 5700MSC-IP will respond to any change in the incoming frequency reference with an immediate re-lock, shifting the timing of the unit to match the reference. This effect will ripple to the outputs and may cause undesired effects in downstream equipment, depending on the amount of correction performed. This is the default mode of operation. When the *Genlock Range* menu item is set to *Wide*, the relocking mode is always *Abrupt*, regardless of the *Lock Type* menu setting.

When the *Slow* lock mode is selected, the 5700MSC-IP will detect when its oscillator is not synchronized to the reference and issue a frequency reference unlocked warning. It will display REF JAM NEEDED on the left LCD display and can also be configured to send out an SNMP trap. It will then gradually adjust the frequency of the OCXO, limiting the rate of change, until the oscillator is brought back into sync with the incoming reference. Once this “slow” re-lock process is complete, the “REF JAM REQUIRED” warning will be cleared. The Lock progress display will return to 100% and the unit will continue normal operation.

The *Slow* lock type can take a long time to relock to the reference signal, especially when correcting for a large discrepancy in phase. It takes about a minute to correct for a phase

difference of one line of video. At any time during this Slow relock process, the operator can force the 5700MSC-IP to immediately lock to the reference by performing a frequency *jam*. This can be performed by selecting *Jam Reference* in the *Jam Input* menu off the **INPUT** root menu. It can also be performed remotely through SNMP. Once the *Jam Reference* has been initiated, the frequency and phase from the reference is jammed into the main oscillator, forcing it to lock immediately. Performing a *Jam* may cause disturbances on all sync and test generator outputs as the phase of the unit is reset.

Careful consideration and testing of Slow lock mode effects should be made, especially when using multiple 5700MSC-IP units locked to each other. Portable truck systems that may require a cold start of all equipment should allow for some time for oscillator warm-up and GNSS lock but could require a manual frequency *jam* to be performed in order to get units locked up quickly.

When the unit is first started up, or if the frequency reference source is changed by the user, a frequency *jam* is always performed. This *jam* occurs even if the *Lock Type* has been set to *Slow* mode. When locked to GNSS, this initial frequency *jam* could occur 5 to 30 minutes after the unit has been restarted, once GNSS lock is fully established.

If a large shift in the reference occurs while Slow lock mode is enabled, the outputs of the 5700MSC-IP may be out of phase for a long time while re-locking. The 5700MSC-IP will gradually slew its oscillator to bring it back into phase with the reference. This slewing action combined with the apparent phase shift may seem to indicate that the unit is completely unlocked to the reference and freerunning. This should not be considered a fault. A manual jam can be performed at any time to force the 5700MSC-IP to lock immediately.

3.2.5. Video Genlock Operation

The 5700MSC-IP can lock to various analog video sync references including NTSC, PAL, Slo-Pal signals, and HD tri-level signals. The applied video reference type is auto detected. The full list of supported standards is shown in Table 3-4. The lock behavior is described for each of the main video sync types.

Video Signal	Frequency Lock	Phase Lock
NTSC-M	Sync edge/Burst	2 Color Frames
NTSC-M + 10field	Sync edge/Burst	5 Frames
PAL-B	Sync edge/Burst	4 Color Frames
625i/48	Sync edge	1 Frame
625i/47.95	Sync edge	1 Frame
1080i/60	Sync edge	1 Frame
1080i/59.94	Sync edge	1 Frame
1080i/50	Sync edge	1 Frame
1080p/60	Sync edge	1 Frame
1080p/59.94	Sync edge	1 Frame
1080p/50	Sync edge	1 Frame
720p/60	Sync edge	1 Frame
720p/59.94	Sync edge	1 Frame
720p/50	Sync edge	1 Frame
720p/24	Sync edge	1 Frame
720p/30	Sync edge	1 Frame
1080p/23.98	Sync edge	1 Frame
1080p/23.98sF	Sync edge	1 Frame
1080p/24	Sync edge	1 Frame
1080p/24sF	Sync edge	1 Frame
1080p/25	Sync edge	1 Frame
480p/59.94	Sync edge	1 Frame

Table 3-4: Supported Analog Video Sync References

3.2.6. Serial Digital Video Timing

The 5700MSC-IP has four separate serial digital video test generators that can be phased independently, and are also phased by the Global Phase controls. In all the supported standards, SD, HD, and 3G, the video outputs are aligned to the supplied reference. The alignment to analog sync has been calibrated using SMPTE compliant timing and is guaranteed to be accurate to within one sample.

It should be noted that certain Tektronix equipment such as the WFM700 and WFM7120 will not show correct alignment of a serial digital video source to a supplied external analog reference. These devices appear to have been calibrated to the output of an unknown video DAC. This means they will not display correct SMPTE timing due to the delay introduced in the measurements by the DAC process. Since the outputs of the 5700MSC-IP are aligned using SMPTE timing, their phase must be advanced significantly in order to appear correct with Tektronix timing.

With no phase offset applied, the SDI outputs of the 5700MSC-IP will be measured by Tektronix gear as approximately 4.7us delayed (SD) or 1.3us delayed (HD) when the Tektronix device is externally referenced to the respective analog sync

Examples of equipment that perform SMPTE compliant timing measurements are the Phabrix SX/DX and OmniTek OTM-1000.

3.2.7. NTSC Genlock Operation

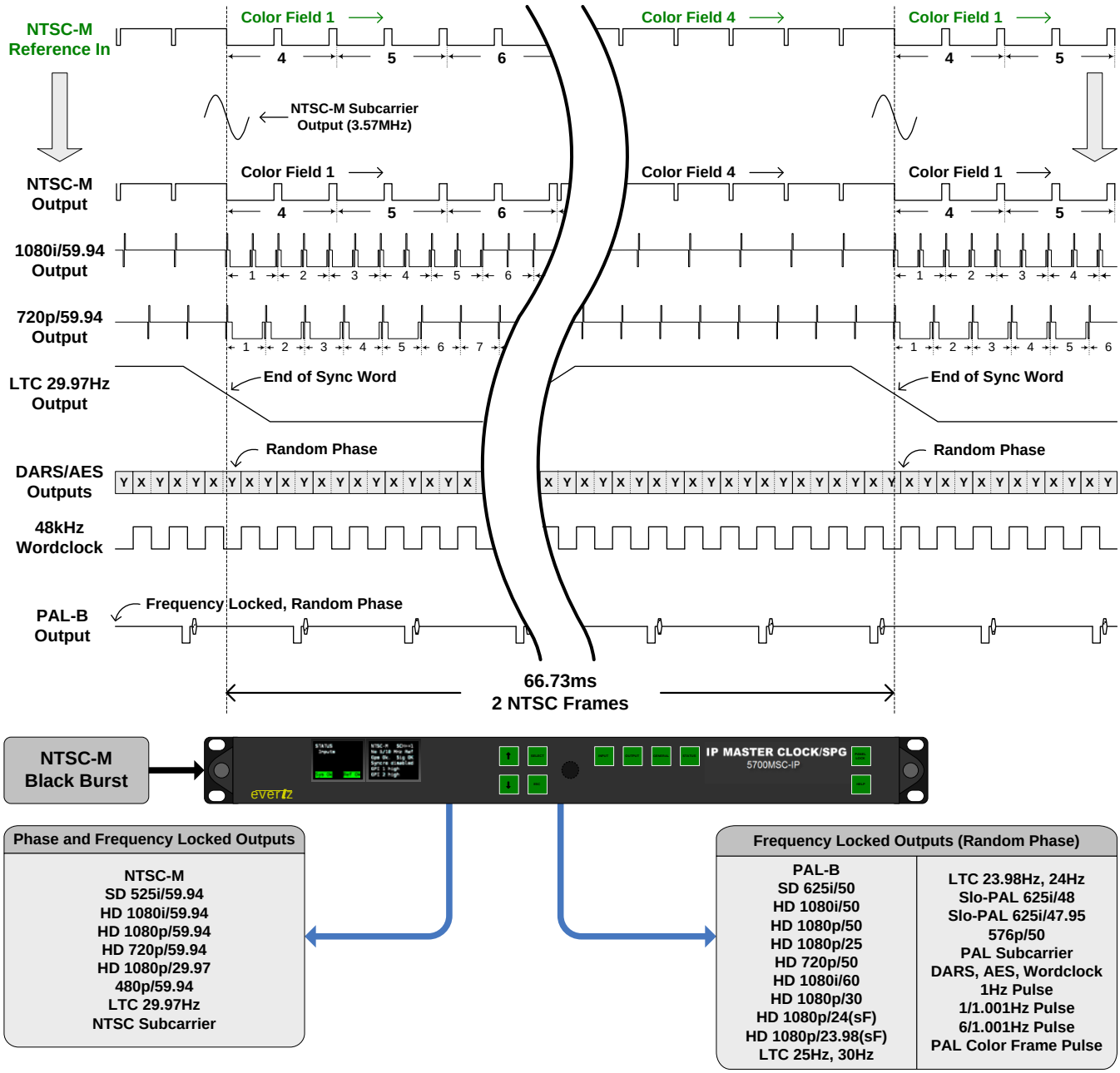


Figure 3-6: Lock Diagram #1 - NTSC Reference without 10field Reference

Figure 3-6 shows the timing relationship between the outputs of the 5700MSC-IP and the applied NTSC video reference. The master oscillator will lock its frequency to the NTSC video reference, and all outputs will become frequency locked. This frequency locking process uses both the horizontal sync and the colorburst to obtain an accurate lock. The applied NTSC reference should have no video content and a low Subcarrier to Horizontal (SCH) offset to assure proper lock. The approximate SCH value is shown in the *Inputs* status screen. If the SCH error is higher than 30º, the 5700MSC-IP will fall back to locking to the horizontal edge of the video only. If the SCH error is in excess of 50º, or the colorburst cannot be accurately measured, the 5700MSC-IP will report that the applied reference is unlockable.

It is important to ensure that the incoming black burst reference is of good quality. There should be no video content on the reference otherwise reference lock could be lost, or higher jitter may be produced on the outputs.

The color frame sequence of the NTSC reference is decoded and used to phase the outputs. Because the NTSC color frame sequence is only 2 frames long, this is not enough phase information to *deterministically* lock signals which align to NTSC on longer periods. This includes 23.98Hz standards, DARS/AES signals, and the 6/1.001Hz pulse. These signals align with NTSC once every 5 frames. This is illustrated in Figure 3-4. The phase of these signals will be set arbitrarily and cannot be guaranteed to be the same between different units that are locked to the same reference. The phase may also change if the unit is restarted.

The phase locking ability of the 5700MSC-IP when supplied with an NTSC reference is summarized at the bottom of the lock diagram (Figure 3-6). The HD standards listed apply to both the HD test generators and the tri-level sync outputs. The serial digital video test generator outputs are phased according to SMPTE compliant timing, which may differ from the timing shown on Tektronix equipment.

If the NTSC reference is lost, the unit will freerun on the selected oscillator. Note than when the *Genlock Range* is set to *Wide*, the freerun drift upon loss of reference will be much higher. When the NTSC reference is re-applied the *Lock Type* menu selection controls how the 5700MSC-IP will respond to re-align its internal oscillator with the reference.

When locked to NTSC **without** a ten-field reference, the AES/DARS outputs cannot be deterministically phased. The *AES/DARS/WC lck* menu item located in the *AES Audio* menu off the **OUTPUT** root menu should be set to *NTSC/fractional*, however the phase relationship will be chosen arbitrarily and may change if the reference is lost or the unit is restarted.

3.2.8. NTSC Genlock with Ten-field Reference

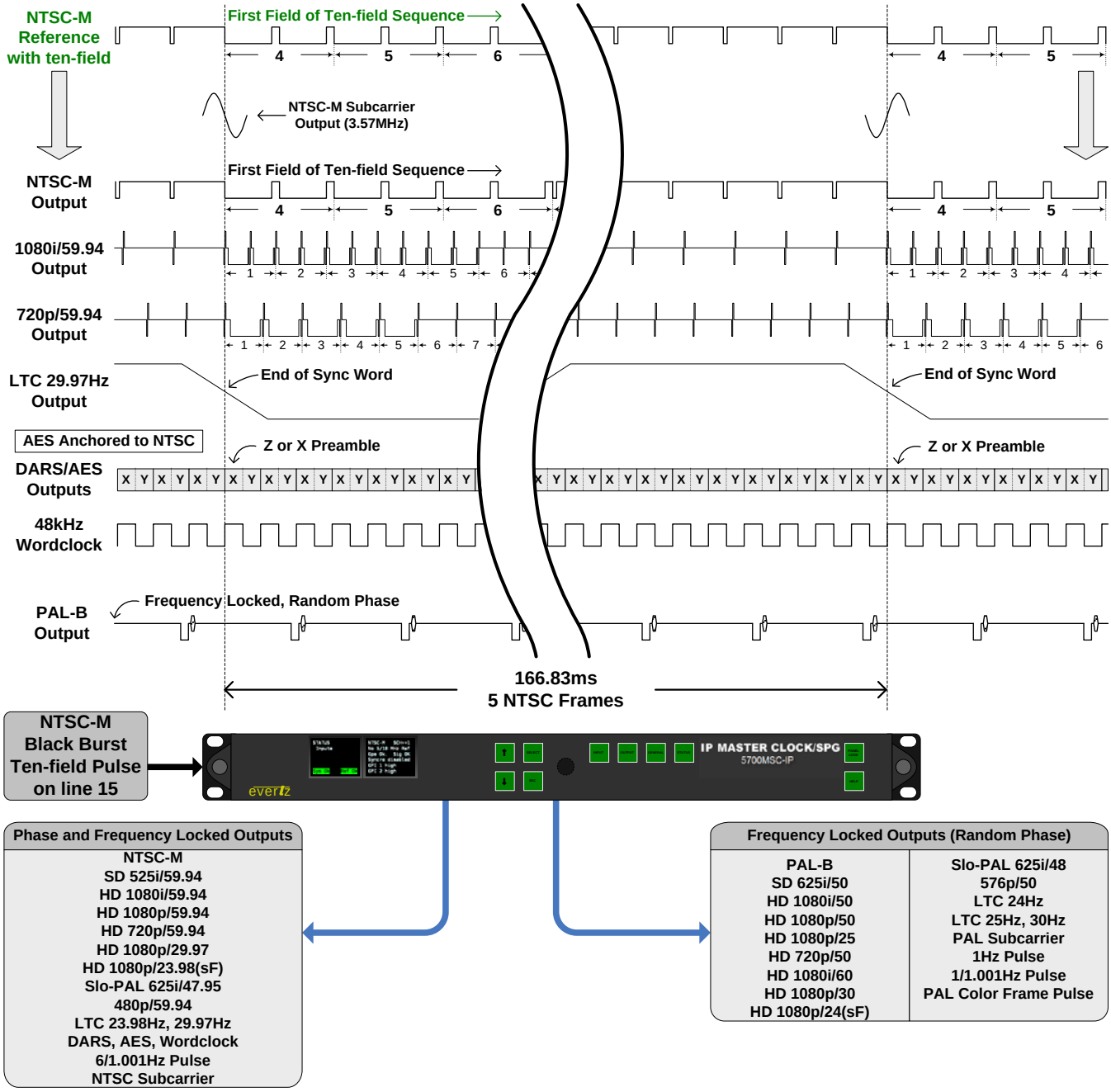


Figure 3-7: Lock Diagram #2 – NTSC Reference with Ten-field Reference

When an NTSC reference is applied that carries a ten-field reference pulse in the vertical blanking interval (VBI) as specified in SMPTE ST 318, the phase locking ability of the 5700MSC-IP is enhanced. The ten-field reference provides 5 frames worth of phasing information that allows deterministic locking of 23.98Hz standards, the 6/1.001Hz pulse, and DARS/AES signals. These outputs can be guaranteed to be the same phase between multiple units. The color frame sequence of the NTSC reference is also decoded and used for phasing NTSC sync outputs. Note that the lock diagram above (Figure 3-7) now shows a span of 5 frames instead of 2 frames for regular NTSC lock (Figure 3-6).

The SMPTE ST 318 ten-field reference can be generated by the 5700MSC-IP on any NTSC sync output. It is turned on and off using the Ten Field Ctl menu item. The 10field waveform is illustrated below in Figure 3-8. The number of pulses indicates where in the sequence the frame belongs. It is inserted on lines 15 (field 1) and 278 (field 2).

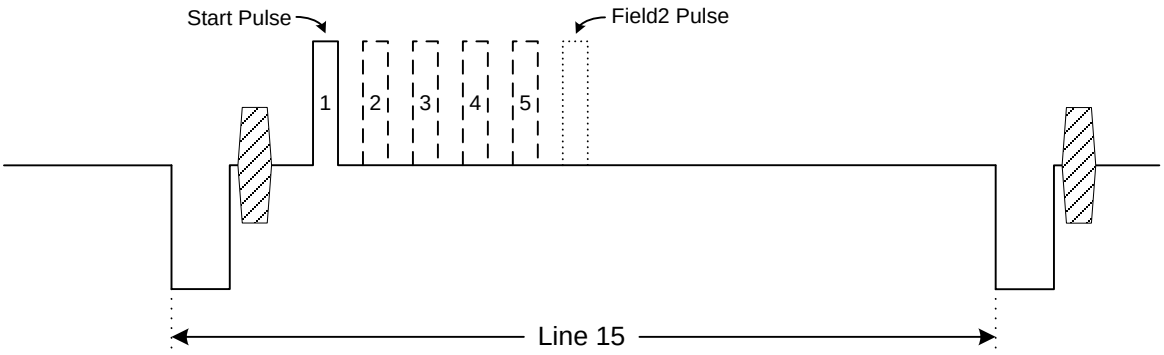


Figure 3-8: SMPTE ST 318 Ten-field Reference on NTSC line 15

Note that AES/DARS Test Generator Outputs are only available on the +AUX option.

When the 5700MSC-IP is locked to an NTSC reference with a ten-field pulse, the AES, DARS, and Wordclock outputs can be phase locked properly. The *AES/DARS/WC lck* menu item located in the *AES Audio* menu off the **OUTPUT** root menu should be set to *NTSC/fractional*.

In the NTSC ten-field lock diagram above (Figure 3-7), the AES/DARS outputs are displayed as frames. Each frame is divided into two subframes, labeled X and Y. The X subframe identifies channel 1 (left channel). The Y subframe identifies channel 2 (right channel). The wordclock output is high during channel 1 and low during channel 2. Note that the AES/DARS and wordclock outputs can be phased independently. If the phase of the AES/DARS outputs is changed for any reason, the phase of the wordclock output should be changed as well to match.

The AES/DARS outputs provide a fixed sample rate of 48kHz (48,000 samples per second). This means that during a single NTSC frame, 1601.6 AES frames will have been generated. It takes five NTSC frames to fit a whole number of AES frames (8008 frames). This means that 48kHz AES/DARS will line up evenly with NTSC sync once out of every five frames, and during the other four frames the AES/DARS waveforms will appear to be partially shifted. The 10field sequence identifies frame #1 (a single pulse) as the frame where the AES/DARS waveforms line up perfectly to horizontal sync of line 4 of the NTSC waveform. This is illustrated in lock diagram #2 (Figure 3-7).

Note that the Z preamble (which identifies the start of a 192-frame AES block) will only line up with NTSC sync once every 120 frames (4.004 seconds). This is in contrast to PAL sync where it will line up every frame. This essentially renders the *AES Coarse* phase adjustment meaningless when locked to an NTSC reference. The alignment of an AES block to analog video sync is not important for proper reception of an AES signal.

If the NTSC reference is lost, the unit will freerun on the selected oscillator. Note than when the *Genlock Range* is set to *Wide*, the freerun drift upon loss of reference will be much higher. When the NTSC reference is re-applied the *Lock Type* menu selection controls how the 5700MSC-IP will respond to re-align its internal oscillator with the reference.

3.2.9. PAL Video Genlock Operation

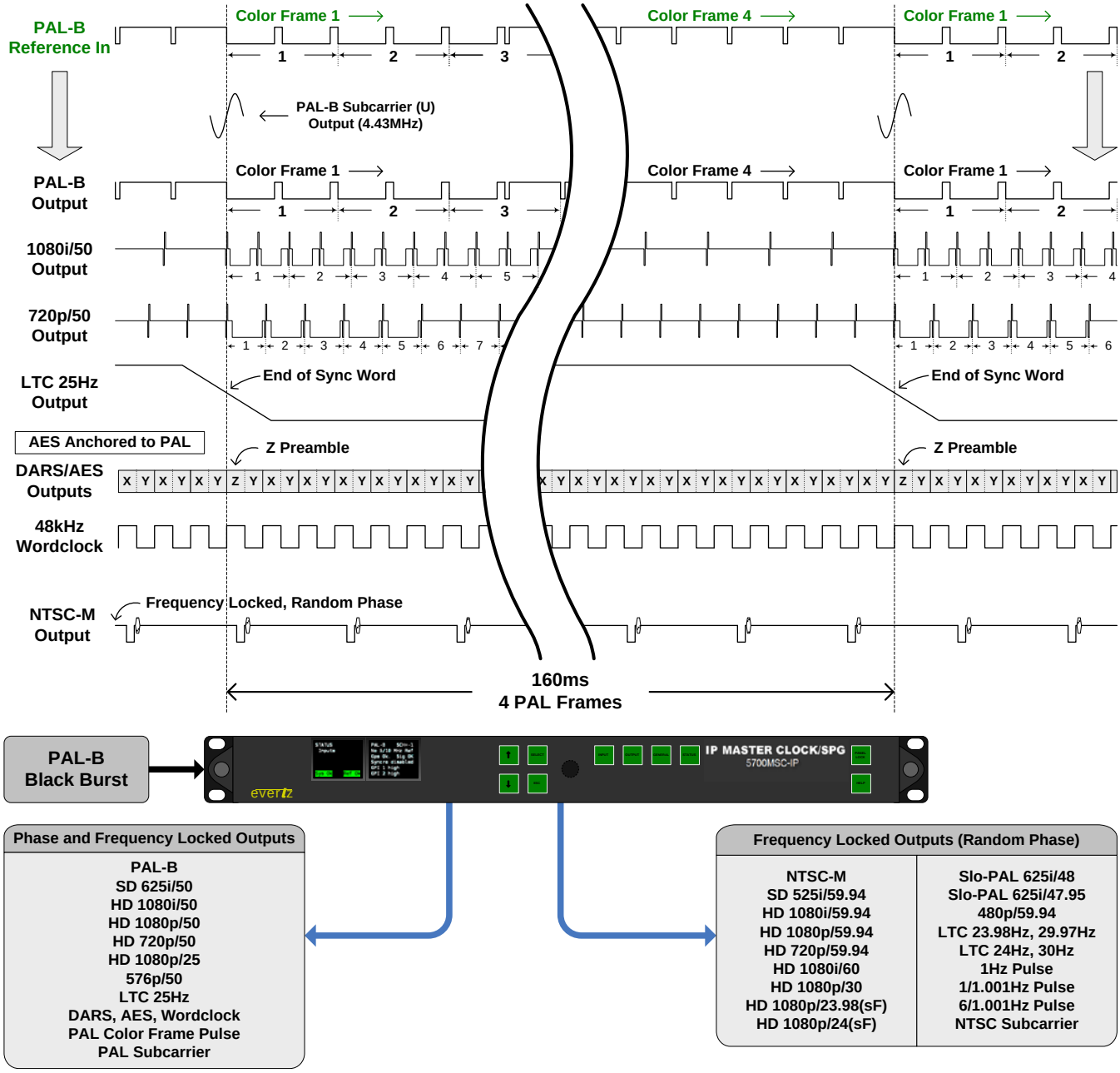


Figure 3-9: Lock Diagram #3 – PAL Genlock

Refer to Figure 3-9 for the timing relationship of signals when the 5700MSC-IP is locked to a PAL black burst reference. The color frame sequence is decoded from the PAL reference and provides a 4 frame phase reference. As with NTSC references, the 5700MSC-IP locks to both the horizontal sync edges and colorbursts of the PAL reference. If the Subcarrier to Horizontal sync error is higher than 30º the 5700MSC-IP will fall back to horizontal sync edge locking only. If the SCH error is higher than 50º, or the colorburst cannot be measured, the unit will report that the reference is unlockable.

When the 5700MSC-IP is provided with a PAL reference, the AES/DARS outputs can be deterministically phase aligned. This is because an even number of AES samples are generated during each frame of the PAL reference. Exactly 1920 AES frames fit into a single PAL frame. The *AES/DARS/WC lck* menu item should be set to *PAL/integer* to assure that the AES/DARS outputs are anchored to the PAL reference. Because the AES signal coincides with the PAL signal on every frame, the phase of the AES/DARS outputs will be the same between multiple 5700MSC-IP units that are locked to PAL. In addition, the AES block length of 192 frames is evenly divisible into a single PAL frame so the start of an AES block (identified by the Z preamble) will correctly align to line 1 of the PAL reference (as illustrated in lock diagram #3 of Figure 3-9).

A PAL reference provides enough information for phasing of 50Hz and 25Hz standards, but does not provide a long enough phase period to deterministically phase 60Hz or 24Hz standards. The standards that can be phased properly are listed at the bottom of lock diagram #3 (Figure 3-9). The HD standards listed apply to both the HD test generators and the tri-level sync outputs. The serial digital video test generator outputs are phased according to SMPTE compliant timing, which may differ from the timing shown on Tektronix equipment.

If the PAL reference is lost, the unit will freerun on the selected oscillator. Note that if the Genlock Range is set to Wide, the freerun drift upon loss of reference will be much higher. When the PAL reference is regained, the *Lock Type* menu selection controls how the 5700MSC-IP will respond to re-align its internal oscillator with the reference.

3.2.10. HD Tri-Level Genlock

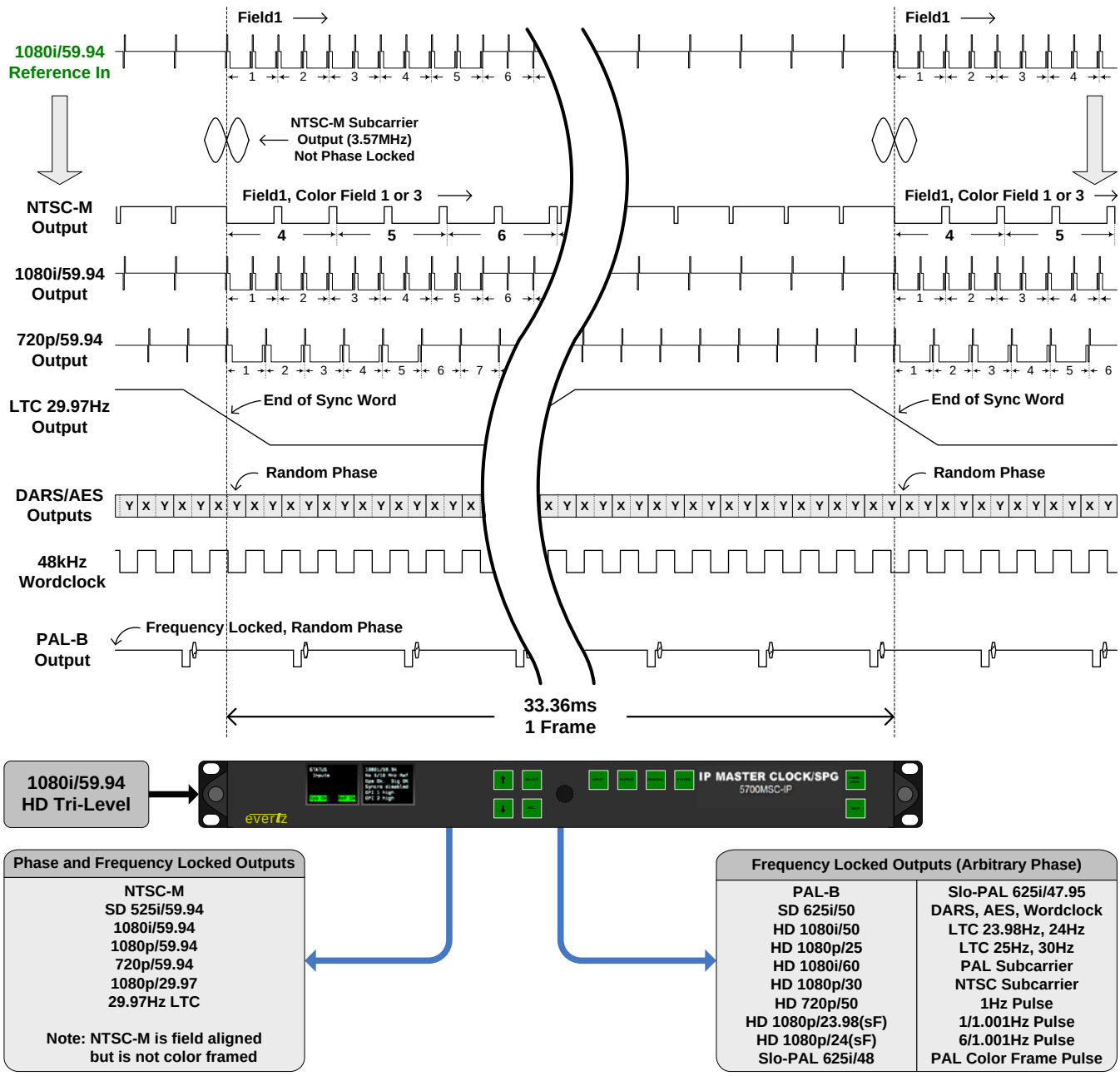


Figure 3-10: Lock Diagram #4 – HD Tri-Level Genlock Operation

The 5700MSC-IP can lock to several different HD analog tri-level signals. The main oscillator frequency is locked to the rising edge of the tri-level waveform. The phase information provided by tri-level reference signals is limited and each signal standard can only be used to deterministically phase lock standards of a similar frame rate. Lock diagram #4 above gives an example for 1080i/59.94 tri-level sync. Refer to Table 3-5 for a summary on the phase locking capability with other tri-level references.

It should be noted that tri-level references do not supply enough phase information to color frame NTSC-M or PAL-B sync outputs. When multiple 5700MSC-IP units are locked to a tri-level source, the

black burst outputs from either unit cannot be guaranteed to have the same color frame phase. As such, the subcarrier outputs of the two units may also not be in phase with each other.

For tri-level sync standards that run at a fractional rate (i.e. 1080i/59.94, 720p/59.94) the AES, DARS, and Wordclock output cannot be deterministically phase locked. This is because only one frame of phase information is provided by the tri-level reference. For these standards, the AES/DARS, and Wordclock output cannot be guaranteed to be the same phase between different units, or that the phase will remain the same if the 5700MSC-IP is restarted.

Reference	Phase Locked Outputs
1080i/60	1080i/60, 1080p/60, 720p/60, AES/DARS, 30Hz LTC
1080i/59.94	NTSC, 525i/59.94, 1080i/59.94, 1080p/59.94, 720p/59.94, 480p/59.94, 29.97Hz LTC
1080i/50	PAL, 625i/50, 1080i/50, 1080p/50, 720p/50, 1080p/25, 576p/50, AES/DARS, 25Hz LTC
720p/60	720p/60, 1080p/60, AES/DARS
720p/59.94	720p/59.94, 1080p/59.94, 480p/59.94
720p/50	720p/50, 1080p/50, 576p/50, AES/DARS
720p/24	625i/48, 720p/24, 1080p/24, 1080p/24sF, AES/DARS, 24Hz LTC
1080p/23.98	625i/47.95, 1080p/23.98, 1080p/23.98sF, AES/DARS, 23.98Hz LTC
1080p/23.98sF	625i/47.95, 1080p/23.98, 1080p/23.98sF, AES/DARS, 23.98Hz LTC
1080p/24	625i/48, 720p/24, 1080p/24, 1080p/24sF, AES/DARS, 24Hz LTC
1080p/24sF	625i/48, 720p/24, 1080p/24, 1080p/24sF, AES/DARS, 24Hz LTC
1080p/25	PAL, 625i/50, 1080i/50, 720p/50, 1080p/25, 576p/50, AES/DARS, 25Hz LTC

Table 3-5: Phase Locking to HD Tri-Level Standards

3.2.11. Slo-PAL Genlock

The 5700MSC-IP supports two Slo-PAL references to provide an ability to lock film-rate standards while using a common analog sync format (PAL). The two standards supported are 625i/48 for use with 24Hz film standards and 625i/47.95 for use with 23.98Hz film standards. With Slo-PAL references, the 5700MSC-IP locks its frequency to the horizontal sync edges and uses the vertical sync for phasing. See Table 3-6 for phasing ability of each reference type.

With a Slo-PAL reference, the AES/DARS outputs can be properly phase aligned since the number of AES samples (48,000 per second) is evenly divisible by Slo-PAL frame rates. There are exactly 2,000 AES samples generated for each frame of 48Hz Slo-PAL. Exactly 2,002 AES samples are generated for each frame of 47.95Hz Slo-PAL.

Note that a 47.95Hz Slo-PAL reference does not provide enough phasing information to deterministically lock the 6/1.001Hz pulse output. When multiple 5700MSC-IP units are referenced to a 47.95Hz Slo-PAL signal, the 6/1.001Hz pulse outputs are not guaranteed to be lined up.

Reference	Outputs Phased Deterministically
625i/48	625i/48, 720p/24, 1080p/24, 1080p/24sF, AES/DARS, 24Hz LTC
625i/47.95	625i/47.95, 1080p/23.98, 1080p/23.98sF, AES/DARS, 23.98Hz LTC

Table 3-6: Slo-PAL Phase Locking

3.2.12. Continuous Wave and Internal References

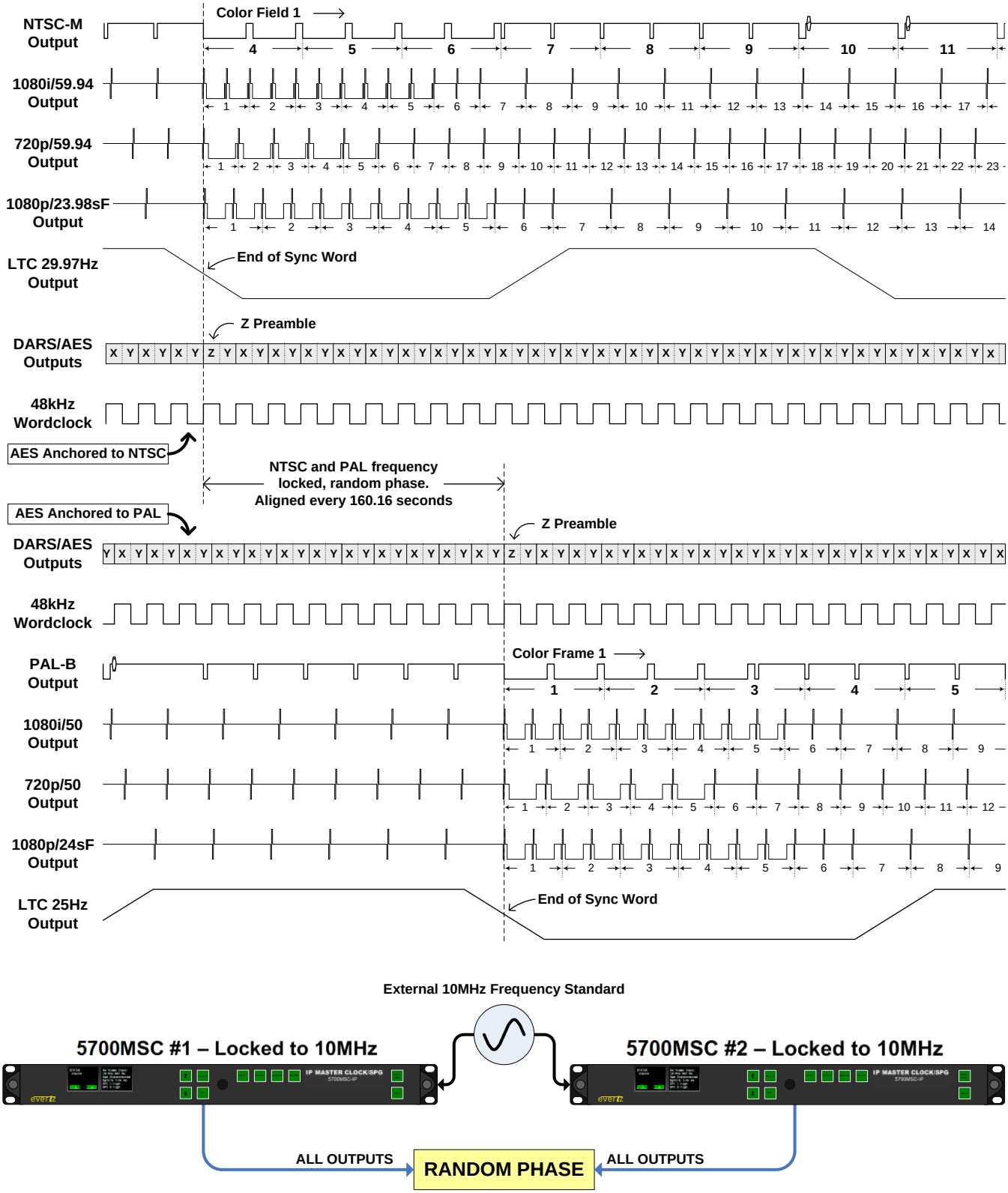


Figure 3-11: Lock Diagram #5 – 10MHz and Internal Frequency References

The 5700MSC-IP can use either 10MHz or 5MHz continuous wave (CW) frequencies as a reference. These signals are applied to the frame reference input BNCs or reference loop-through HD-BNCs and the frequency is automatically detected by the 5700MSC-IP. With CW signals, the main oscillator frequency is locked to the incoming reference but absolutely no phasing information is supplied. The 5700MSC-IP will arbitrarily pick an internal phase reference point once frequency lock is obtained. Lock diagram #5 (Figure 3-11) illustrates the generation of signals when locked to a reference that provides no phasing information.

While outputs of the same standard will be phased correctly to each other, they will not be phased deterministically. The outputs of multiple units locked to a CW reference cannot be guaranteed to be in phase. Furthermore, if the 5700MSC-IP unit is restarted the phase relationships can change as a new phasing point is chosen. Likewise if the CW reference is lost, any drift accumulated during the time the reference is absent cannot be corrected for once the reference is regained.

In order to align the output phase of two 5700MSC-IP units that are locked to a stable CW reference, the *Ten MHz Global Phase* controls can be used. When the *Ten MHz Global Phase* is enabled, the 5700MSC-IP outputs can be phased manually to align them with another source. In this configuration, the unit will maintain a stable phase relationship as long as the CW reference is uninterrupted and the unit is not restarted. If a restart does occur, the 10MHz Global Phase controls are automatically disabled and reset to zero at startup.

When a CW reference is used, the phase of the DARS and AES outputs can be anchored to either NTSC or PAL standards. This is chosen using the *AES/DARS/WC lck* menu item in the *AES Audio* menu. This menu item should be set to the dominant video standard that will be used in the particular installation.

When the CW reference is lost, the 5700MSC-IP will freerun on its active oscillator, selected by the *Genlock Range* menu item. The *Lock type* menu item controls how the 5700MSC-IP responds when the reference is regained.

3.2.12.1.Internal Frequency Reference

When *Internal Ref* is selected for the frequency reference, the 5700MSC-IP will free-run on the 10MHz output of its high-stability OCXO oscillator, regardless of the *Genlock Range* menu item setting. The locking operation is similar to when locking to CW signals. The 5700MSC-IP will pick an arbitrary phase reference to generate all outputs. This phase reference will be different between multiple 5700MSC-IP units set to free-run, and will change if the unit is restarted.

The output phase of a 5700MSC-IP that is running off its internal reference can be adjusted by using the *Internal Global Phase* controls. When enabled, these controls will allow for **temporarily** bringing a free-running 5700MSC-IP into phase with another piece of equipment. Although the internal oscillator of a 5700MSC-IP is very stable, it will inevitably drift away from another reference due to the slight variation in frequency of its internal oscillator.

3.2.13. GNSS Frequency Reference

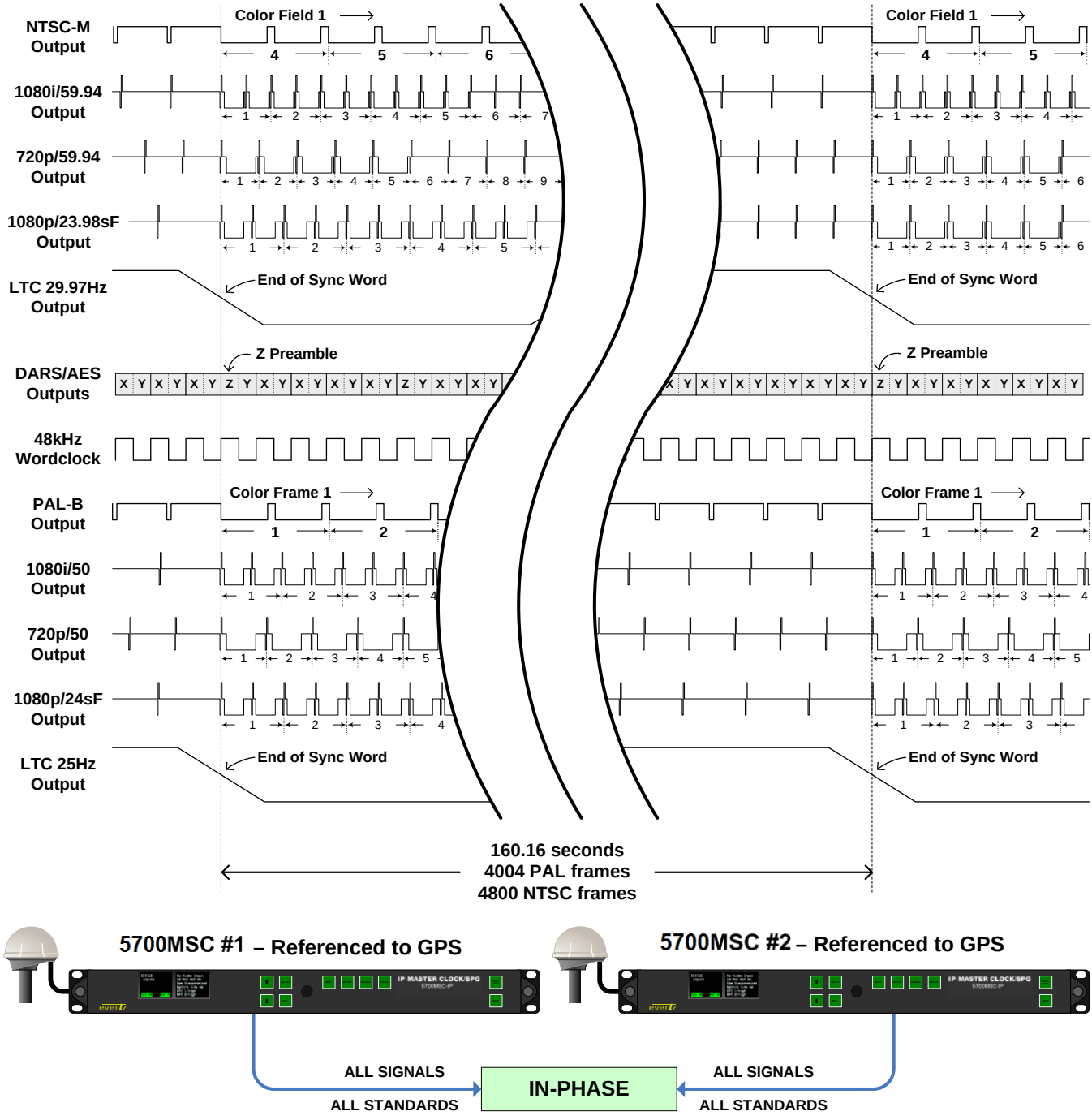


Figure 3-12: Lock Diagram #6 – GNSS Frequency Reference

The 5700MSC-IP unit can lock in frequency and phase to the high-accuracy timing provided by the GNSS satellites. The main oscillator frequency is locked to the 1 pulse per second (PPS) timing pulse provided by the receiver. Because of the low rate of this timing pulse, only the high-stability OCXO oscillator can be used and the *Genlock Range* control will be forced to Narrow regardless of the menu setting.

The GNSS receiver also provides highly accurate time. The 5700MSC-IP uses the time information to set the phase of all outputs. This is done by choosing a moment in GNSS time when all standards started at their initial phase. By working backwards to that moment, the instantaneous phase of any standard can be determined for any point in time. This allows true deterministic cross-standard phasing. See Figure 3-12 for the timing relationship between multiple standards when locked to GNSS.

Because the 5700MSC-IP uses GNSS time to determine the phase of the outputs, the time reference will be forced to use GNSS, regardless of the time *Reference Src* menu item setting.

Using GNSS as a frequency reference is the only way to guarantee that all outputs across multiple standards will be phased to each other across multiple units. Furthermore, when two 5700MSC-IP units are separated by a large distance, using GNSS receivers can assure they will be phased to within 100ns of each other. Note than when using multiple units the antenna cable lengths should be matched as closely as possible to eliminate any cable length propagation delay effects that may cause phase errors between them.

If the GNSS receiver is unplugged, or if the number of satellite signals being received drops to 0, the 5700MSC-IP will free-run on its high stability OCXO. The *Lock type* menu item controls how the unit will respond when the GNSS signal is restored. When the unit first starts up, the phase of its outputs are random until GNSS lock is acquired.

While GNSS provides a convenient way to lock the 5700MSC-IP in all standards simultaneously and ensure extremely good frequency accuracy, there can be issues dealing with limited availability and phase errors. A GNSS reference can be described as a “soft” lock. As more satellite signals are discovered, the phase accuracy of the GNSS lock improves. However, there will always be some “wander” associated with GNSS lock due to uncontrolled variables such as atmospheric disturbances and terrestrial interference. This can cause problems when two different units are locked to separate GNSS receivers.

Under ideal conditions, with 8 satellite signals being received, the maximum wander in phase between two units locked to two separate GNSS antennas can be up to 15ns. This is greater than the duration of a single sample of serial digital HD video which may cause problems for router installations that require sample-accurate timing. During poor weather conditions, the satellite signal strength will drop which will cause fewer satellite signals to be available for phase corrections. This is why mounting of the GNSS receiver is extremely critical in order to get the best phase locking performance. If the receiver does not have a clear view of the sky or is subject to multipath interference due to reflections off buildings, the phase wander between units can quickly climb to unacceptable levels. The unpredictability of such variations can be difficult to troubleshoot so these characteristics must be taken into account during the design phase of any system.

3.3. TIMEKEEPING

The 5700MSC-IP contains a **system clock** to keep track of time and date. The *stability* of this clock is equal to the selected frequency reference. The *accuracy* of this clock is determined by the selected time reference and lock mode. The 5700MSC-IP can access time references through the GNSS receiver, PTP from another 5700MSC-IP, SNTP, or VITC read from a black burst reference. The **system clock** should always be set to Coordinated Universal Time (UTC). Time zone offsets can be applied to the timecode outputs to provide local time.

The **system clock** is synchronized to the selected time reference by performing a *time jam*. This is different than the continuous PLL process that is used for frequency references. The **system clock** in the 5700MSC-IP runs independently at the frequency provided by the **master oscillator**. Ideally, once the **system clock** has been set, it should keep perfect time forever. In practice stability errors, however slight, creep in and accumulate over time. Even when locked to GNSS or an atomic frequency standard, leap seconds will occur in UTC time requiring the **system clock** to be occasionally adjusted.

The 5700MSC-IP has several timecode outputs, each of which possess their own clock that runs independently from the **system clock**. The LTC outputs and each sync output (including 10MHz and Wordclock) and test generator outputs have their own independent clock. The timecode clocks are synchronized to the **system clock** once a day at user specified times. This allows for timecode rates that do not count in real-time. Note that NTP and IRIG time is derived directly from the **system clock**.

The **system clock** time/date is constantly compared to the time/date that is provided by the selected time reference. Whenever a significant difference is detected, a *system time jam* will be required to bring the **system clock** back into sync with the time reference. A *system time jam* effectively jams the time and date acquired from the time reference into the system clock. This effect ripples to all timecode output clocks jamming them as well. Exactly when a *system time jam* is allowed to take place is determined by the *Lock Type* that is selected. The amount of difference between the **system clock** and the time reference must exceed a certain threshold before a system time *jam* is declared necessary. This threshold is different for each time reference type.

3.3.1. Time Lock Types

The 5700MSC-IP **system clock** runs independently from the time reference. When a difference that exceeds the threshold is detected between the **system clock** and the time reference, a time jam is required to set the system clock to the time reference. How and when such a *jam* occurs is configured by the *Lock Type* menu item located in the *Time* menu off the **INPUT** root menu. The four *jam* modes are shown below with detailed descriptions.

Figure 3-13: 5700MSC-IP Jam Modes

Always - Whenever the **system clock** is different than the time reference**,** a *jam* will automatically be performed. In this mode, the **system clock** will continuously track the time reference. Any change in the time reference will immediately affect all timecode clocks. This mode is most useful when the time reference is known to be reliable and stable such as with GNSS.

Never - In this mode, the time comparator is effectively shut off and the **system clock** will run independently from the time reference. No jam warnings will be generated. It is still possible to synchronize the system clock to the time reference by performing a manual time *jam*. This mode is useful when a time reference is not being used or is not always available.

User - When the time comparator detects a difference between the **system clock** and the time reference, it will notify the operator with a jam warning. The message "TIME JAM NEEDED" will be displayed on the front panel, and optionally an SNMP trap can be sent. The operator can then decide if and when to perform a *jam* in order to cause minimum disruption to systems. This mode should be selected when the time outputs of the 5700MSC-IP require absolute minimum disruptions.

Daily - The time comparator is shut off in this mode. A *jam* will be performed once a day at the time specified by the *Input Jam Time* control. This way the **system clock** can be brought into sync with the reference regularly, at time of day when any disruptions would go unnoticed.

When the Time Reference is set to SNTP, the Time Lock Type is forced to Daily.

A manual time jam can be initiated using the *Jam Time* menu item. When a *time jam* is performed, all timecode clocks are also *jammed*. Exercise caution before initiating a *jam*.

3.3.2. Coordinated Universal Time (UTC)

Coordinated Universal Time (UTC) is used worldwide as the basis of civil time and runs at the same rate as International Atomic Time (TAI). Unlike atomic time, Coordinated Universal Time is kept within one second of *mean solar time*, or Greenwich Mean Time (GMT). The rotation of the earth is very slightly slowing which causes the solar day to lengthen by a fraction of a second. This introduces a slight error between atomic time and solar time. Over weeks, months, and years, the error can add up until atomic time is a full second ahead of solar time. Because UTC runs at the same rate as atomic time, it must be slowed down if it is to match solar time.

Leap seconds are introduced periodically and cause UTC clocks to count one extra second in a day to slow them down. The rotation of the earth is unpredictable which means the need for a leap second cannot be predicted more than six months in advance. If a leap second is necessary, it will occur at the end of the day usually on either June 30th, or December 31st. Refer to www.iers.org for more information and bulletins on upcoming leap seconds. Leap seconds can cause complications with 25Hz LTC or PAL VITC.

The 5700MSC-IP expects that the time reference provides UTC time. This is a requirement for the NTP server hosting using the NRC protocol.

3.3.3. Time Reference Sources

The **system clock** can be referenced in one of several ways. The reference type is selected in the *Time* menu located in the **INPUT** root menu. The *Reference Src* menu item is used to select between GNSS, LTC, VITC, IRIG, SNTP, 1588 and None. Note that the time reference will be forced to GNSS if the frequency reference has been set to GNSS, no matter what has been selected here.

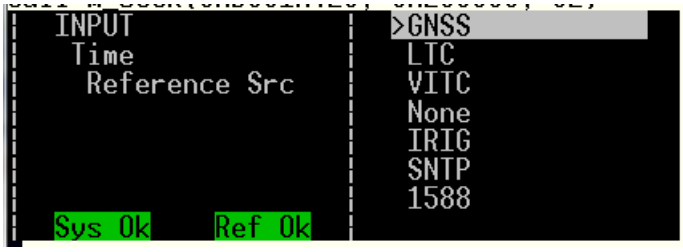


Figure 3-14: 5700MSC-IP Time Reference Sources

3.3.3.1. GNSS Time Reference

When GNSS is selected as the time reference, time and date are obtained from the GNSS receiver that is connected to the 5700MSC-IP. The GNSS time provided by the receiver is then converted to UTC time by adding leap seconds. This time reference is extremely accurate and once the **system clock** has been jammed to the GNSS receiver, it should remain in sync for a very long time without requiring further jams, provided the selected frequency reference is also accurate.

Of all the time reference sources, GNSS is the most accurate and reliable. When a difference of greater than 2 milliseconds is detected between the **system clock** and the time from the GNSS receiver, the 5700MSC-IP will generate a *jam* event or jam warning, depending on the Lock Type setting. Such a difference can be caused by accumulated stability errors or by the introduction of a leap second.

When the frequency reference has been set to GNSS, the time reference is also forced to GNSS.

3.3.3.2. LTC Time Reference

The 5700MSC-IP+AUX can obtain time and date from an LTC input present on the GPIO DB15 connector. All output frame rates in Table 3-7 are supported as references. Note that non real-time rates such as 23.98 and 29.97 nondropframe should be used with caution.

Date information can be decoded from the user bits (binary groups) of the LTC input. There are several date formats in use and the date decoding method can be selected using the *VitcLtc Date* menu item. Automatic detection of the date format is reliable for Legacy and SMPTE formats but may not work well for Production date formats. If the user bits of the incoming LTC are not defined, or do not contain date information the date decoder must be disabled (put into *No date* mode) to prevent false date decoding and spurious *jam* events. When date decoding is disabled, the date can be set manually using the *Set System Date* menu item located in the **GENERAL** root menu.

The 5700MSC-IP+AUX will continuously compare the **system clock** to the incoming LTC time and date. When a difference of more than 2 milliseconds is detected the 5700MSC-IP+AUX will generate a *jam* event, or a jam warning depending on the *Lock Type* setting. When a *jam* event occurs, the time read from the LTC input is jammed into the **system clock**. At the same time, the LTC input time is jammed into the timecode output clocks.

When the incoming LTC is jammed into a particular output timecode clock, it may be adjusted to maintain color frame alignment and to match the output frame rate. If a particular timecode output is the same frame rate as the incoming LTC, the time is copied directly into the output's clock. If the

timecode output is running at a different frame rate than the LTC input, then the time is rounded to the nearest frame before being jammed into the output's timecode clock.

3.3.3.3. VITC Time Reference

The 5700MSC-IP can read Vertical Interval Time Code (VITC) from a SMPTE ST 318 compliant color black signal that is applied to the reference loop input. The VITC can be on any line of the incoming color black video from line 6 to line 31. The VITC reader line is set by the *Vitc Line* menu item. The 5700MSC-IP can read 25Hz VITC extracted from a PAL-B reference signal, and 29.97Hz dropframe VITC extracted from an NTSC-M reference signal.

Date information can be decoded from the user bits of the VITC. The date format is selected using the *VitcLtc Date* menu item. The automatic detection mode works well for Legacy and SMPTE formats, but may not work reliably for Production date formats. If there is no date information on the incoming VITC or if the user bits are being used for another purpose, the date decoder must be disabled by setting it to *No Date*. This prevents false date decoding that may trigger spurious *time jam* events or warnings. When the date decoder is disabled, the date can be manually set using the *Set System Date* menu item in the **GENERAL** root menu.

The 5700MSC-IP will continuously compare the **system clock** to the incoming VITC timecode. When a difference of more than 2 milliseconds is detected the 5700MSC-IP will generate a *jam* event, or a jam warning depending on the *Lock Type* setting. When a *jam* event occurs, the time read from the VITC input is jammed into the **system clock**. At the same time, the VITC input time is jammed into the timecode output clocks.

When the incoming VITC is jammed into a particular output timecode clock, it may be adjusted to maintain color frame alignment and to match the output frame rate. If a particular timecode output is the same frame rate as the incoming VITC, the time is copied directly into the output's clock. If the timecode output is running at a different frame rate than the VITC input, then the time is rounded to the nearest frame before being jammed into the output's timecode clock.

In order to use VITC as a time reference, the frequency reference must be set to *Video*.

3.3.3.4. IRIG Time Reference

When the *IRIG* option is installed, the 5700MSC-IP+AUX will be able to read IRIG-B timecode that is applied to the LTC input on the GPIO connector. The IRIG type is auto-detected. Only the IRIG-B124 and IRIG-B127 formats supply complete date information. If other formats are used, the system date will have to be set manually using the *Set System Date* menu item in the **GENERAL** root menu.

The **system clock** is continuously compared with the incoming IRIG timecode. When a difference of more than 5.5 milliseconds is detected the 5700MSC-IP+AUX will flag that a time *jam* is required. The time *Lock Type* menu item controls how the 5700MSC-IP+AUX responds when a time *jam* is needed.

3.3.3.5. SNTP Time Reference

The 5700MSC-IP can jam its **system clock** to an external NTP server. Unlike with other time references, this synchronization is not continuous and happens once a day. The time *Lock Type* is forced to *Daily*, and the *Input Jam Time* control sets the time of day the synchronization happens. Up

to eight external NTP servers can be defined. All enabled NTP servers will be contacted and the server response with the best stratum and dispersion values will be chosen to jam the system clock.

3.3.3.6. No Time Reference

When the time reference source is set to *None*, the 5700MSC-IP will ignore all time reference sources and the **system clock** will freerun. The time and date must be set manually using the *Set System Time* and *Set System Date* menu items located in the **GENERAL** root menu. It is recommended to set the system clock time to UTC rather than to local time. Local time can then be specified using a time zone offset from UTC on the timecode outputs.

The “eyeball and wristwatch” method of setting the **system clock** cannot be considered accurate time. The NTP server will report an unlocked condition (LI_Alarm) unless spoofing is enabled.

3.3.4. LTC and VITC Timecode

The primary purpose of LTC and VITC timecode is to count frames. Each LTC count relates to one frame of video. The Linear Time Code output waveforms are aligned to video so that the end of the sync word lines up with the start of the field1 vertical sync. This occurs on line 4 for the NTSC standard, and line 1 for the PAL standard. Vertical Interval Time Code can be inserted onto any black burst sync output and is inserted onto a vertical blanking line once per field, twice per frame. See Figure 3-15 for LTC and VITC timing relationships. Note that VITC is inserted once per field allowing VITC timecode to count fields. LTC timecode has one count per frame and does not count fields.

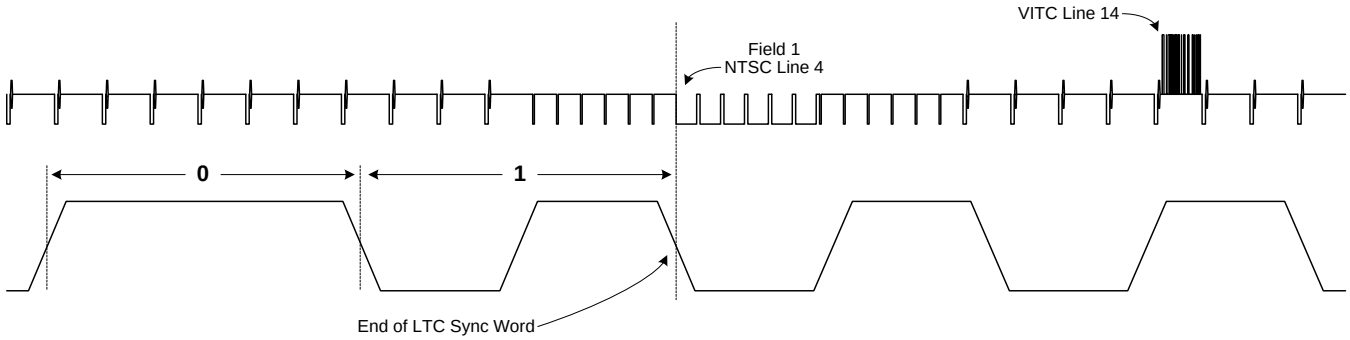


Figure 3-15: Detail of 29.97Hz LTC Waveform Alignment to NTSC Video

The LTC/VITC timecode rates supported by the 5700MSC-IP are summarized in Table 3-7. All of these rates maintain alignment to their respective video standards. When VITC is inserted onto a PAL black burst sync output, it runs at 25Hz. When VITC is inserted onto an NTSC black burst sync output it runs at 29.97Hz. In addition to video alignment, the LTC and VITC timecode for the 25Hz and 29.97Hz rates can be adjusted to maintain color frame alignment as per SMPTE ST 12-1.

Name	Counting Rate	Frame counts per second	Time to count one frame	Time to count one second worth of frames	Number of frame counts in a 24-hour period	Color frame Alignment
23.98 FPS	24/1.001 Hz	24	41.708 ms	1.001 seconds	2,073,600	No
24 FPS	24 Hz	24	41.67 ms	1 second	2,073,600	No
25 FPS	25 Hz	25	40 ms	1 second	2,160,000	PAL
29.97 FPS	30/1.001 Hz	30	33.367 ms	1.001 seconds	2,592,000	NTSC
29.97DF FPS	30/1.001 Hz	30	33.367 ms	1.001 seconds	2,589,408	NTSC
30 FPS	30 Hz	30	33.33 ms	1 second	2,592,000	No

Table 3-7: Supported LTC Frame Rates Summary

Relating LTC/VITC frame counts to real time can get quite complex. The LTC rates of 24Hz and 30Hz run at real-time and do not suffer from color frame alignment rules. They take exactly one second to reach their full count of either 24 or 30 frames. The 25Hz rate also runs at real-time but may be adjusted to maintain color frame alignment to PAL video (see section 3.3.4.5 for the implications of this).

The 23.98Hz and 29.97Hz rates run slightly slower than real-time. They take slightly longer than one second (1.001 seconds) to count a full second worth of frames. This means that every minute they will lag behind real-time by 0.06 seconds. Every hour they will be behind 3.6 seconds. After a 24-hour period they will be 86.4 seconds behind real-time. These rates are unsuitable for timekeeping purposes. They are only useful for counting frames.

3.3.4.1. Dropframe Counting

Because the 29.97Hz rate is used extensively as timecode for video reference signals, a method was developed to allow reasonably precise time keeping with the non real-time rate. This method involves dropframe counting. Since the 29.97Hz rate runs slower than real-time, dropframe counting skips over certain frame counts in order to periodically catch up to real time. Frame counts are always skipped over in pairs so as not to disrupt any color frame alignment. Two frame counts are skipped over at the beginning of every minute, except minutes 00, 10, 20, 30, 40, and 50. This pattern can be seen in Figure 3-16.

Dropframe counting ensures that 29.97Hz timecode accumulates just 86.4 milliseconds of error per day and always stays within 200 milliseconds of real-time. Figure 3-17 illustrates the drift and catch-up cycle that dropframe counting goes through over the course of a day. Real-time is represented by the solid X-axis in the graphs.

To maintain a long-term correlation to real time, all LTC and VITC timecode outputs are *jammed* to the **system clock** once per day. This limits the amount of accumulated error for non real-time rates. Daily jamming is also required for real-time rates to prevent accumulation of stability errors and to keep synchronized should a leap second occur. The time at which this daily jam occurs is controlled by the *Jam Time* menu item present in all LTC and sync output menus. The daily *jam* should be scheduled to occur at a time when it would be least likely to affect system operation. The timecode clock will *jam* when the LTC or VITC timecode count matches the *Jam Time* value.

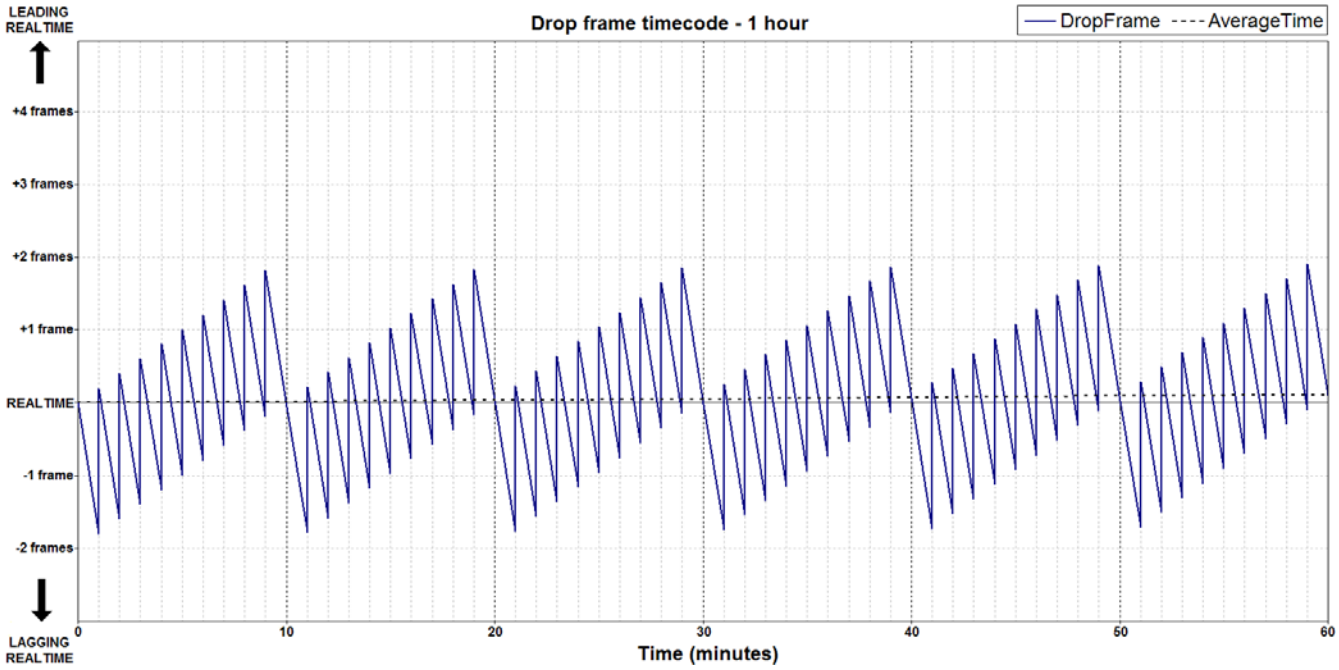


Figure 3-16: Dropframe Timecode with Respect to Real-time over a 1-Hour Period

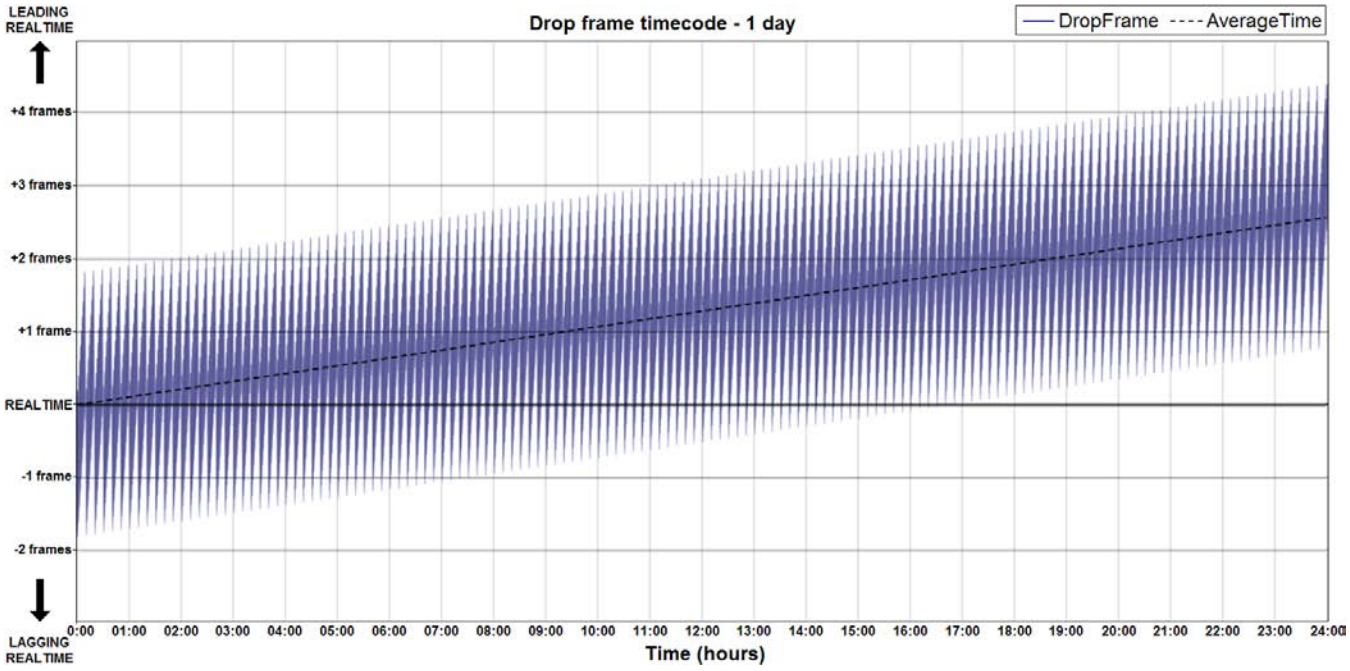


Figure 3-17: Dropframe Timecode with Respect to Real-time over a 24-Hour Period

3.3.4.2. LTC/VITC Timecode Color Framing

If the Color Frame control is turned on, the 25Hz and 29.97Hz LTC timecode rates will have their counts adjusted by the 5700MSC-IP so that they maintain color frame alignment to the selected frequency reference as per SMPTE ST 12-1. If a black burst sync output has its Color Frame control turned on, the VITC timecode is adjusted to same way to maintain color frame alignment to that particular black burst sync output. See the pulse diagrams in Figure 3-3 and Figure 3-4 for examples of timecode color frame alignment.

3.3.4.3. Color Frame Alignment to NTSC

Color frame alignment can be enabled for any NTSC sync output and for LTC timecode that runs at 29.97 frames per second. Even frame counts must coincide with color fields 1 and 2. Odd frame counts must coincide with color fields 3 and 4. When a system time jam event occurs, the timecode output clock is jammed to system time and then adjusted, if necessary, to match the color frame phase of the particular LTC or sync output.

The consequence of color frame alignment is that the LTC/VITC timecode may be jammed one frame count off of real-time, depending on the phase of the frequency reference and the phase of the LTC or sync output. See Figure 3-18 for an example of daily time jamming involving dropframe timecode.

3.3.4.4. Multiple LTC/VITC Outputs with Dropframe Counting

It should be evident that dropframe timecode maintains only a loose correlation to real-time, and cannot always be jammed exactly to real-time. Dropframe timecode counts an entire 24-hour period 86.4 milliseconds faster than real-time. This is the equivalent of 2.59 frames of video. At the daily jam event, when the timecode clock is jammed to the system clock, some extra frame counts will have to be inserted to bring the timecode closer to real-time. It is not possible to adjust by fractional frame counts. Either 2 or 3 frame counts must be added, which means the timecode output cannot be jammed exactly to the system clock and some error will occur. If color frame alignment is enabled, the extra frame counts can only be inserted in pairs. Therefore, 2 or 4 frame counts will be inserted, depending on the error accumulated from the previous daily jam.

See Figure 3-18 for an example of a daily *jam* event for LTC1 in 29.97Hz dropframe counting mode. When the timecode of LTC1 hits the daily jam time, a *jam* to the real-time **system clock** is performed. However, the number of extra counts inserted is adjusted to maintain color frame alignment to the frequency reference (either GNSS or NTSC). If the timecode output was VITC, the adjustment would also have to factor in any phase offset that may have been applied to the respective sync output.

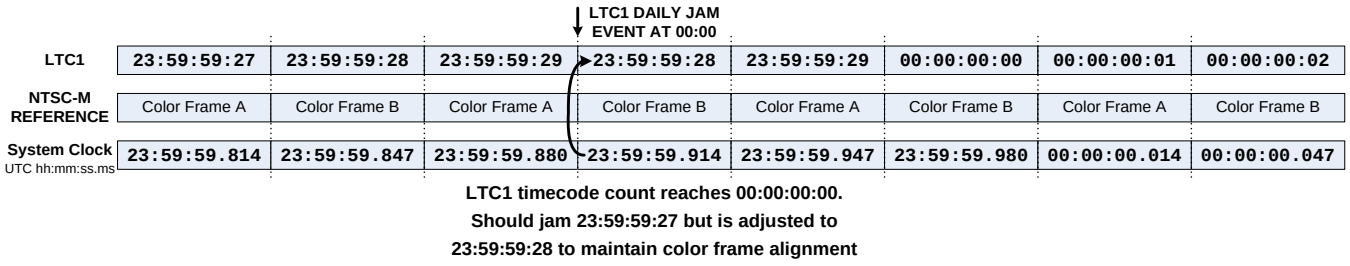


Figure 3-18: Daily Time Jam Event for 29.97Hz Dropframe Timecode

Every time the daily jam event occurs, the 5700MSC-IP will attempt to bring the dropframe timecode as close to system time as possible, while optionally maintaining color frame alignment. The amount of frames adjusted depends on the error accumulated from the previous daily time jam. See Figure 3-19

for an example of a week worth of daily time jams on a dropframe 29.97Hz timecode output. The pattern of 2 frame and 4 frame adjustments runs over a period of a couple months.

If multiple timecode outputs are set to dropframe counting mode, it is possible that they may jam differently from each other at the daily time jam event, even if they are set to jam at the exact same time. This can occur if they were initialized at different times. To prevent this from happening, use the "Jam all VitcLtc" menu item which forces all timecode outputs to jam at the same instant. This manual jam is typically done at an innocuous time of day. There is currently no method of forcing multiple units to jam together at the same time. It can be expected that eventually a 2-frame offset may appear between dropframe timecode across multiple 5700MSC-IP units.

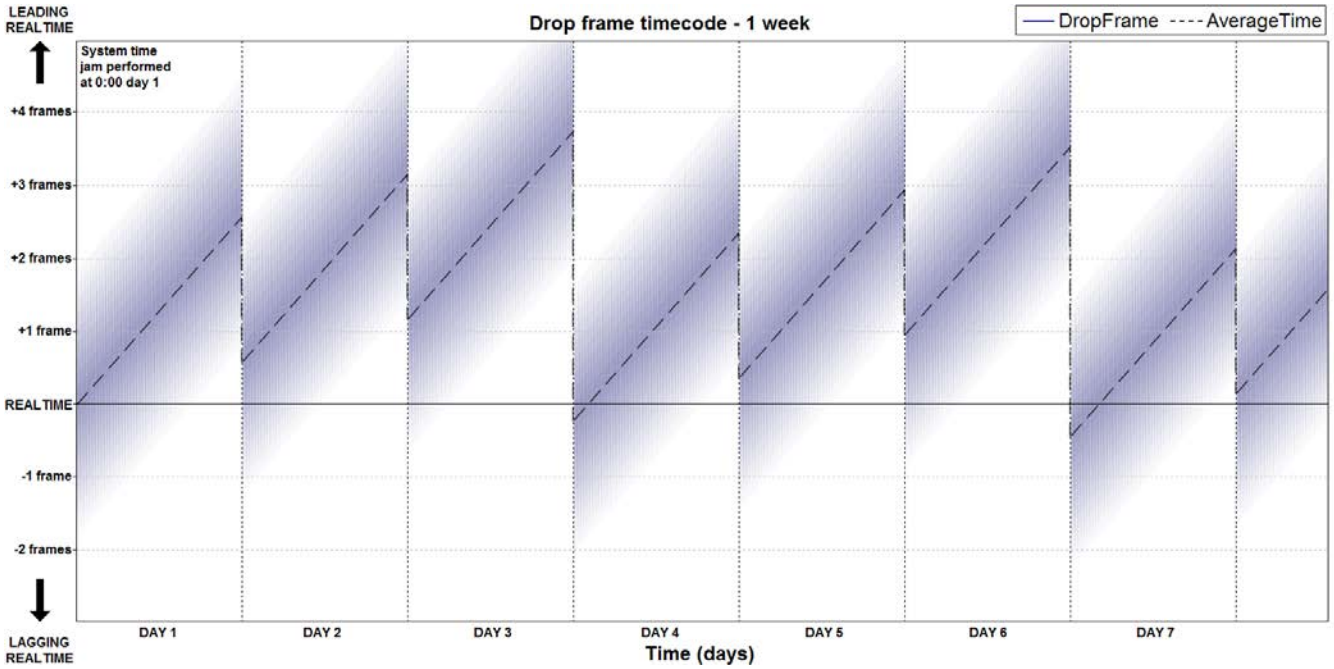


Figure 3-19: Dropframe Timecode with Respect to Real-time over One Week

3.3.4.5. Color Frame Alignment to PAL

Color frame alignment to PAL video can be enabled for 25Hz LTC timecode and for any PAL sync (VITC) output or PAL analog TG output (burn-in window). The 25Hz timecode runs at exactly real time which means it is always possible to *jam* the timecode output exactly to the **system clock**. However, the color frame alignment rule adds additional complexity. The color frame sequence in PAL runs over 4 frames (8 fields), which does not divide evenly into a 25 frame per second count. This means that color frame 1 lines up with the same frame count only once every four seconds. Therefore color frame alignment occurs once every 4 seconds.

When a time *jam* event occurs, the timecode output clock is jammed to the **system clock** and then may be adjusted up or down one or two frame counts to match the color frame phase of the reference or particular black burst sync output. If the frequency reference to the 5700MSC-IP is not phased correctly with respect to the time reference this can cause a static one or two frame shift for 25Hz timecode outputs, with respect to the **system clock**.

If the frequency reference of the 5700MSC-IP is set to GNSS, the time reference will also be forced to GNSS. The system phase reference is derived from GNSS time, but the **system clock** is set to UTC time, which is offset from GNSS time by the total number of leap seconds that have occurred since the

year 1980. Because the PAL color frame to timecode relationship runs over 4 seconds, this produces a unique problem when aligning UTC-locked timecode to the PAL color frame.

The **system clock** of the 5700MSC-IP is always set to UTC time. The PAL reference phase is tied to GNSS time which is not affected by leap seconds. Whenever a leap second occurs, UTC time counts an extra second, slowing it down. At the next *jam* event, the PAL timecode clock could *jam* to the system clock causing it to shift backwards by one second. If done this way, it would break the timecode to color frame relationship. However, the 5700MSC-IP must adjust the time that is jammed into the 25Hz LTC/VITC clocks in order to maintain color frame alignment. This means is that a static, positive or negative, 1 or 2 frame offset may be introduced between real time and 25Hz timecode even when the 5700MSC-IP is locked to GNSS. This static offset will change every time a leap second occurs.

3.3.5. IRIG Timecode

When equipped with the **IRIG** option, the 5700MSC-IP is capable of generating IRIG-B timecode from the LTC outputs and can also read IRIG-B timecode on the LTC input. The IRIG-B formats supported are shown in Table 3-8. All IRIG-B formats are based on 100-bit timecode that is amplitude modulated with a 1kHz sine wave carrier. The differences between the four formats are in what additional information is carried besides the Time-of-Year timestamp. All control flag bits, if present, are set to zero.

Format Name	Information Carried
IRIG-B120	Time-of-Year, Control Flags, Straight Binary Seconds
IRIG-B122	Time-of-Year
IRIG-B123	Time-of-Year, Straight Binary Seconds
IRIG-B124	Time-of-Year, Year, Control Flags, Straight Binary Seconds
IRIG-B127	Time-of-Year, Year, Straight Binary Seconds

Table 3-8: Supported IRIG Timecode Formats

The IRIG-B outputs are aligned to the IRIG Datum pulse as shown in Figure 3-20. For an overall view of the entire IRIG waveform, refer to Figure 3-1. The output waveform consists of a 1kHz carrier that is amplitude modulated to the IRIG pulse waveform. The frame reference bit (P_R) leading edge coincides with the IRIG Datum pulse output from the 5700MSC-IP. When locked to GNSS, IRIG will be aligned within 20 microseconds of the 1pps pulse from the GNSS receiver (with no global phase offset).

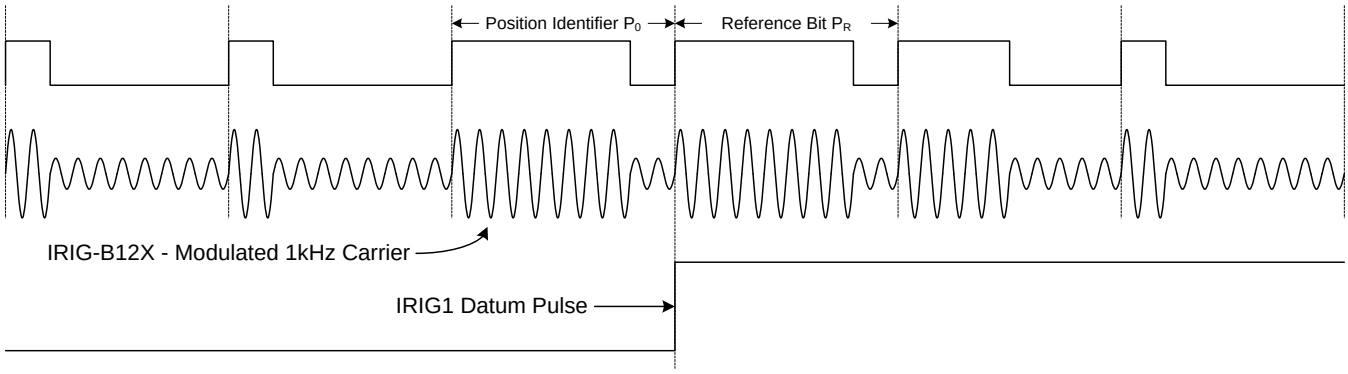


Figure 3-20: Detail of IRIG Alignment to IRIG Datum Pulse

Depending on the IRIG format selected, different types of information may be placed in the IRIG frame. The Time-of-Year portion is always present and indicates the current system clock time in seconds, minutes, hours, and day of the year. The IRIG-B120, IRIG-B123, and IRIG-B127 formats include a straight binary seconds counter which gives the current time of day in seconds. The IRIG-B127 format also includes the current year as a two-digit number (e.g. 2011 = 11). The IRIG timecode is generated directly from the system clock, which should be set to UTC.

The LTC outputs (with the 5700MSC-IP+AUX option) can be configured to one of the four IRIG formats in their respective menus. The IRIG signal amplitude can be controlled by the *Output Level* menu item. When an LTC output has been configured to an IRIG output mode, both primary and secondary outputs will provide the same IRIG signal.

The 5700MSC-IP can also be configured to the IRIG-B as a time reference. The time reference source must first be set to IRIG. The *Irig Mode* menu item selects which IRIG format to use as a reference and can also enable auto detection. Only IRIG-B127 can provide full date information.

Both IRIG input and output circuitry is balanced. To connect an unbalanced IRIG source to the LTC input, or to use the LTC outputs to drive an unbalanced IRIG cable, refer to Figure 3-21 for examples on how to make these connections.

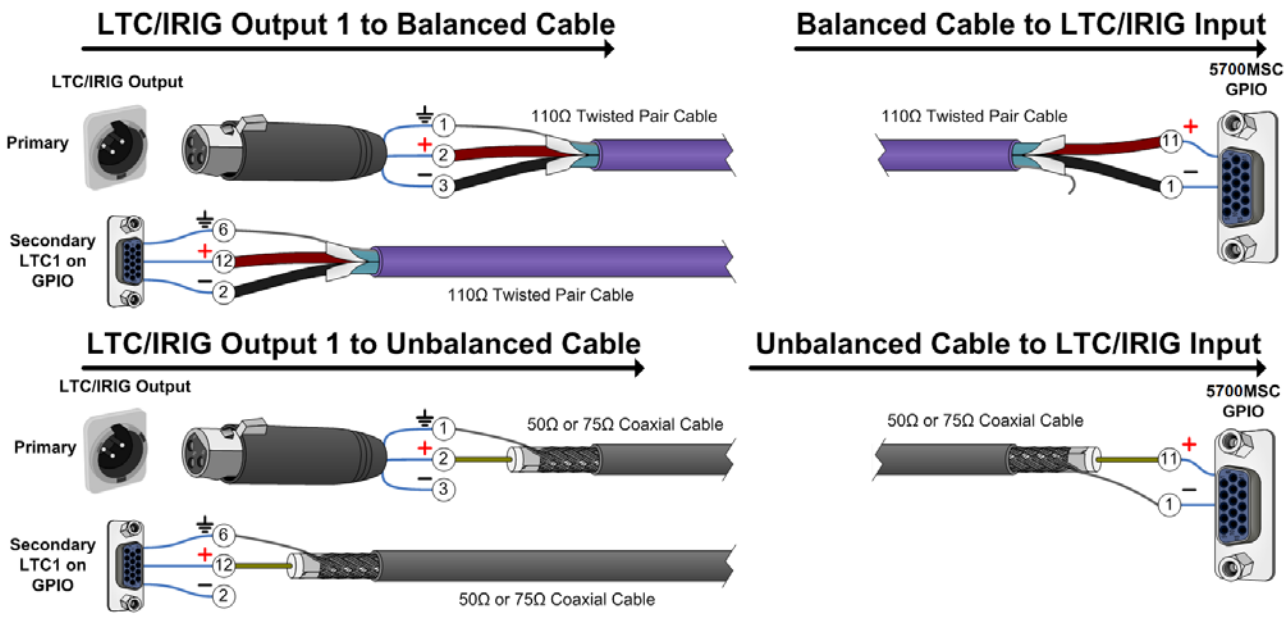


Figure 3-21: IRIG Input and Output Connections

3.4. NETWORK TIME PROTOCOL (NTP)

If the 5700MSC-IP has an available Network Time Protocol (NTP) server, it runs on the CONTROL Ethernet port using the IP address assigned to the port. The NTP features are configured in the *NTP Rules* menu located in the **GENERAL** root menu.

The 5700MSC-IP implements version 3 of the NTP protocol as defined in RFC 1305. The NTP server uses the **system clock** as its source of time. This requires the system clock to be set to UTC in order to generate a valid NTP timestamp. The contents of the packets are largely determined by the chosen time reference and the lock status.

If the 5700MSC-IP is not locked to the selected time reference, the LI_Alarm flag in all outgoing NTP packets will be set. This informs clients that the NTP reference clock in the 5700MSC-IP is not locked to a reference. This flag is also set when the time reference is set to *None*. When this flag is set, most clients will reject the time packet provided by the 5700MSC-IP. This flag can be deactivated by enabling NTP spoofing. NTP spoofing should only be used for testing and troubleshooting purposes as it technically breaks compliance with the NTP standard.

When an incoming client request for NTP time is received by the 5700MSC-IP, the source IP address is checked against a list of NTP restrictions. There are a total of eight restrictions and they are checked sequentially. If the incoming request passes all eight restrictions, the NTP server will respond.

It is possible to perform a quick validation of NTP operation using a Windows PC that is connected to the same network as the 5700MSC-IP. For Windows XP Home edition, right-click on the time display of the taskbar and select Adjust Date/Time. This will open up the Date and Time control panel. There should be three tabs at the top: “Date & Time”, “Time Zone” and “Internet Time”. If the “Internet Time” tab does not exist, use the command-line method below. Enter the IP address of the 5700MSC-IP into the Server text box and click on the “Update Now” button. If the PC communicates with the 5700MSC-IP NTP server, the time should update successfully.

Another method is to use the “w32tm” utility from the command prompt. It may be necessary to install the Windows Time Service before this command will be available. Open a command prompt window by going to START>Programs>Accessories or by going to START>Run and typing in “`cmd`”. Enter the command “`w32tm /monitor /computers:172.21.1.56`”. In this case 172.21.1.56 is the IP address of the 5700MSC-IP.

```
C:\WINDOWS>w32tm /monitor /computers:172.21.1.56
172.21.1.56 [172.21.1.56]:
    ICMP: 0ms delay.
    NTP: +35.0868750s offset from local clock
        RefID: 'GPS [71.80.83.0]
```

Figure 3-22: Testing the NTP Server

In the example above, the NTP server in the 5700MSC-IP at 172.21.1.56 was successfully contacted. The PC clock is 35 seconds advanced from the time provided by the 5700MSC-IP. The RefID indicates that the 5700MSC-IP is locked to GNSS time.

3.5. GLOBAL NAVIGATION SATELLITE SYSTEM

The 5700MSC-IP can be both frequency and time locked to the Global Navigation Satellite System (GNSS). The following section describes the basics of the GNSS system and the operation of the 5700MSC-IP when it is locking to the GNSS satellites.

3.5.1. Overview

The Global Positioning System (GPS) is a satellite based navigation system operated and maintained by the U.S. Department of Defence. There are currently 32 satellites in orbit providing worldwide 24 hour coverage. Presently GPS is the most accurate technology available for marine and land navigation and it is the technology of choice in timing applications including remote site and network synchronization.

Each GPS satellite Space Vehicle (SV) contains four onboard atomic clocks. These clocks are averaged and are used to transmit GPS time, along with the positions of all satellites (the almanac) and fine tracking data (the ephemeris). To acquire GPS time, the receiver only needs to track one satellite. The position of the satellite is known and the transmission delay can be subtracted to obtain GPS time with millisecond accuracy.

In order to obtain a three-dimensional position, the ranges from multiple satellites must be compared. If the receiver had perfect timing, three satellite ranges would be sufficient to calculate a position. In real-world applications, the clock in the receiver will not be an atomic clock and the smallest error in frequency will cause huge errors in positioning. Consequently, a fourth satellite range is incorporated to solve for timing error in the receiver. This allows the receiver to correct its clock and synchronize it to within nanoseconds of the GPS constellation. The 5700MSC-IP is more involved with this clock correction/synchronization feature of the GPS process than it is with the positioning aspect.

3.5.2. GNSS Lock Operation

The GNSS receiver is a Trimble Acutime 360 which is designed for maximum accuracy in static (antenna not moving) mounting applications. The receiver will also function when mobile with decreased precision.

When the GNSS receiver is first connected, it will try to track satellite signals using its stored almanac. The status display will report “GNSS Searching” during this initialization stage. If the receiver has been powered off for a while, or has been moved a significant distance, it may need to download a new almanac. This can require up to 15 minutes of continuously tracking a satellite to complete.

It should be noted here that when GNSS is being used for a time reference only, contact with just a single satellite is enough to provide accurate time. A GNSS time reference will start working as soon as a single satellite is tracked. For frequency synchronization, a more complex process is involved.

When the almanac is determined to be valid, the receiver will attempt to complete a self-survey. This is done by averaging up to 300 positional readings to obtain precise locational data for the antenna. This process can take up to 5 minutes.

Obtaining a position requires the receiver to track at least four satellites. Satellites which do not meet the minimum quality criteria (elevation, signal strength, dilution of precision) cannot be used during a self-survey. The status display will read “GNSS Poor Signal” if four healthy satellite signals cannot be found. These requirements are more stringent when performing a self-survey than they are when in normal operation.

When the self-survey is complete, the GNSS receiver will begin to send out a 1pps pulse to the 5700MSC-IP. The 5700MSC-IP will frequency-lock its ovenized oscillator to the pulse edges, and phase-lock to GNSS time. Once the GNSS receiver knows its precise location, it can substitute its position into the equation and solve only for clock error and clock bias. In this mode, it can operate with just one satellite and still provide accurate timing to the 5700MSC-IP.The status of the GNSS lock progress can be monitored in the *Lock Status* and *Inputs* status screens.

As more satellite signals are detected, the receiver will enter over determined clock mode. Up to 12 satellites can be tracked, using their signal strength and position in the sky to give them more or less weight in contributing to the solution. The quality criteria are more relaxed than when performing a self-survey and each available satellite will improve timing precision. If the receiver is moving, such as in a mobile application, the receiver will enter dynamic mode and still provide reasonably high precision.

After the 5700MSC-IP has locked to the GNSS receiver and is in a steady state condition for longer than 20 minutes the master oscillator will be phase locked to within 15ns to 90ns of the GNSS system time reference, depending on the number of healthy satellites that are tracked. When using multiple 5700MSC-IP units referenced to GNSS, it is important to make sure both receivers are mounted equally so that they detect a similar number of satellites, and that the antenna cable lengths are matched as closely as possible to limit signal path propagation delays to match their phases as closely as possible.

If the GNSS receiver is disconnected, the ovenized oscillator within the 5700MSC-IP may drift very slowly over time. The maximum frequency drift of the oscillator is less than 0.04Hz of subcarrier frequency after a day of the GNSS receiver being disconnected. The drift will be less than 0.3Hz if the GNSS receiver was disconnected or obscured from the sky for 1 year.

3.5.3. GNSS Re-Lock in *Slow Mode*

When the frequency lock mode is set to Slow, the 5700MSC-IP can provide a very smooth recovery of phase upon reconnection of the GNSS antenna. There will be a very smooth transition of the 5700MSC-IP's phase back to the GNSS system time reference. This transition is very gradual with no non-linear jumps. Because the phase period when locked to GNSS is very long (160 seconds – see Figure 3-12) this relock process can take a long time when the phase is considerably far off. The re-lock will take less then 40 minutes after an unspecified period of time (i.e. 1 year or more) of the GNSS receiver being disconnected or obscured from the sky. If the GNSS receiver is removed for 5 minutes and then returned, the unit will take nominally less then 5 minutes to fully re-lock. If the GNSS receiver is removed for 15 minutes and then returned, the unit will take nominally less than 20 minutes to fully phase-lock to the GNSS system time.

3.5.4. GNSS Position Insertion into Timecode

The 5700MSC-IP can insert the current position of the GNSS antenna into the user bits of the LTC and VITC outputs. This is controlled by the *VitcLtc dte fmt* menu item in the *GENERAL* root menu. Timecode with even numbered frames contain longitude in the user bits, and timecode with odd numbered frames contain latitude.

The format for latitude is wxxxyyzz where w is 1 for south (-), and 2 for north (+), xxx is degrees, yy is minutes, and zz is seconds.

The format for longitude is wxxxyyzz where w is 3 for west (-), and 4 for east (+), xxx is degrees, yy is minutes, and zz is seconds.

For example, at the Evertz Microsystems factory, the data is

latitude: 20432348 longitude: 30794623

This corresponds to:

North (+) 043 degrees, 23.48 minutes

West (-) 079 degrees, 46.23 minutes

It can be entered into Google maps using the format "+43 23.48 -79 46.23".

3.6. AUTOMATIC CHANGEOVER OPERATION

For critical infrastructure requirements a 5700ACO automatic changeover unit can be used to connect two 5700MSC-IP units in a dual redundant configuration. The automatic changeover unit monitors signal health to decide which of the 5700MSC-IP units will be connected to the downstream outputs.

The automatic changeover unit allows for a dual-redundant installation of two 5700MSC-IP units. Normally one of the 5700MSC-IP units is designated to the *master*, and its outputs are connected to the automatic changeover unit. The second 5700MSC-IP unit is designated as the *slave* (or backup), and its outputs are also connected to the automatic changeover unit. The automatic changeover unit then provides relay-protected outputs to feed downstream equipment. The automatic changeover unit can be switched manually (locally via front panel or remotely via SNMP), or can be put into automatic mode where the outputs will be switched to the slave unit if a problem is detected with the master.

In order for a seamless switch to occur, redundant signals from both 5700MSC-IP units must be running at the same frequency and phase and ideally locking both units to the same reference. It is possible to lock the slave unit to the master but this reduces the protection offered by the automatic changeover unit should a problem develop with the master unit. Additionally, it is required that both 5700MSC-IP units are configured identically so that their outputs settings match. For this to occur, an IP *syncro* connection needs to be configured between one 5700MSC-IP acting as the IP Syncro Master, and one or more other 5700MSC-IP units acting as slaves. This is done over the Ethernet GigE-1 interfaces of all 5700MSC-IP Master Clocks that are intented to share the same settings.

The automatic changeover unit simplifies wiring by providing a single point of entry for an LTC reference, and GPIs for both 5700MSC-IP units. The LTC input to the automatic changeover unit is internally split to both Bank A and Bank B 5700MSC-IP units. Similarly, the GPI inputs are split to both units, allowing any GPI trigger to affect both units simultaneously.

The automatic changeover unit uses latching relays to provide a fail-safe signal path. These relays will maintain their last state should the automatic changeover unit experience a power supply failure or main board failure. This ensures glitch-free failure events and glitch-free recovery from failure.

All inputs from both 5700MSC-IP units are *passively* monitored by the automatic changeover unit. There are no active components in the signal path. This is accomplished by splitting a small portion of the incoming signal to the control/monitoring circuitry of the automatic changeover unit.

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4. INSTALLATION

4.1. REAR PANEL

Figure 4-1 provides an illustration of the 5700MSC-IP rear panel.

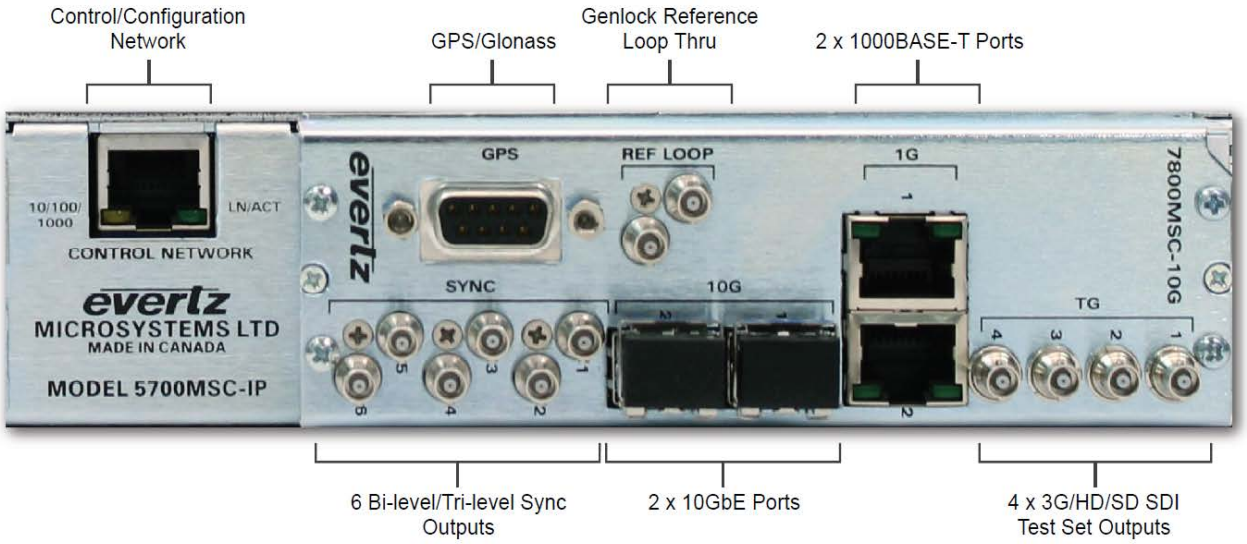


Figure 4-1: 5700MSC-IP Rear Panel

4.1.1. Reference Loop Connections

The two **REF IN LOOP** HD-BNC connectors provide a reference loop input for black burst, tri-level, and 5MHz/10MHz signals. The HD-BNCs are isolated from chassis ground. The frequency reference source must be set to *Video* in order to genlock to black burst or tri-level video signals. It must be set to *10MHz* in order to lock to 5MHz or 10MHz reference signals. The loop is high impedance and will need to be properly terminated with 75 ohms using an external termination.

4.1.2. Sync Outputs

SYNC 1 to 6 - These HD-BNC connectors provide six independent programmable sync outputs that are configured by the SYNC 1 to SYNC 6 group of sub-menus in the OUTPUT setup menu. The 5700MSC-IP+AUX provides two additional HD-BNC connectors: SYNC 7 and SYNC 8. Each output can be configured for any format of sync output from black burst, to tri-level, to 5MHz/10MHz, to wordclock, and more.

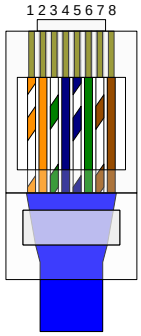
10 MHz OUT (SYNC 7) - This HD-BNC connector provides a 10MHz frequency reference but can also be programmed as another sync output. It is recommended that this output be configured as a 10MHz output when used in conjunction with an automatic changeover unit to simplify wiring. It is configured using the 10 MHz sub-menu in the OUTPUT setup menu.

WORDCLOCK (SYNC 8) - This HD-BNC connector provides a 48kHz wordclock signal but can also be programmed as another sync output. It is recommended that this output be configured as a wordclock output when used in conjunction with an automatic changeover unit to simplify wiring. It is configured using the Wordclock sub-menu in the OUTPUT setup menu.

4.1.3. Ethernet Connections

The 5700MSC-IP is equipped with 5 interfaces, of which one is furnished through the 1G copper frame controller port (called the FP), two 1G copper ports on the rear plate, and two 10G SFP ports on the rear plate. All ports can do PTP, PCR, NTP, FTP and SNMP. Additionally, the two 10G SFP ports also provide three IP Test Generator signals. The 1G ports can be used with 10Base-T (10 Mbps), 100Base-TX (100 Mbps) or 1000Base-TX (1000Mbps) twisted pair Ethernet cabling systems. When connecting for 10Base-T systems, category 3, 4, or 5 UTP cable as well as EIA/TIA – 568 100Ω STP cable may be used. When connecting for 100Base-TX systems, category 5 or better UTP cable is required. The cable must be "straight through" with an 8-pin modular connector at each end. Make the network connection by plugging one end of the cable into the CONTROL receptacle of the 5700MSC-IP and the other end into an Ethernet hub or switch. The CONTROL port hosts an NTP server (with periodic broadcasts) and an SNMP server for remote monitoring and control.

The straight-through Ethernet cable can be purchased or can be constructed using the pinout information in Table 4-1. A color code wiring chart is provided in Table 4-1 for the current Ethernet standards (AT&T 258A or EIA/TIA 258B color coding shown). Also refer to the notes following the table for additional wiring guide information.



Pin #	Signal	EIA/TIA 568A	AT&T 258A or EIA/TIA 568B	10BaseT or 100BaseTX	1000BaseT
1	Transmit +	White/Green	White/Orange	X	X
2	Transmit –	Green	Orange	X	X
3	Receive +	White/Orange	White/Green	X	X
4	Bi-Directional +	Blue	Blue	Not used (required)	X
5	Bi-Directional –	White/Blue	White/Blue	Not used (required)	X
6	Receive –	Orange	Green	X	X
7	Bi-Directional +	White/Brown	White/Brown	Not used (required)	X
8	Bi-Directional –	Brown	Brown	Not used (required)	X

Table 4-1: Standard 8-pin Modular Connector Wiring Color Codes

Note the following cabling information for this wiring guide:

- Only two pairs of wires are used in the 8-pin modular connector to carry Ethernet signals for 10BaseT and 100BaseTX. 1000BaseT uses all four pairs.
- Even though pins 4, 5, 7 and 8 are not used for 10BaseT and 100BaseTX, it is mandatory that they be present in the cable.
- 10BaseT and 100BaseTX use the same pins; the same crossover cable will work with both.
- Pairs may be solid colors and may not have a stripe.
- Category 5 cable must use Category 5 rated connectors.

The maximum cable run between the 5700MSC-IP and the supporting switch is 328 ft (100 m). The maximum combined cable run between any two end points (i.e. 5700MSC-IP and PC/laptop via Ethernet switch) is 656 feet (200 m) when using **copper** cable.

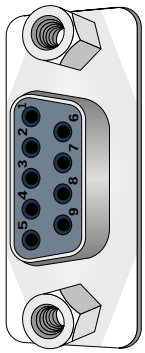
Devices on the Ethernet network continually monitor the receive data path for activity as a means of checking that the link is working correctly. When the network is idle, the devices also send a link test signal to one another to verify link integrity. The 5700MSC-IP rear panel is fitted with two LEDs to monitor the Ethernet connection.

10/100/1000: This Amber LED is ON when a 100Base-TX link is detected. The LED is OFF when a 10Base-T link is detected.

LN/ACT: This dual purpose Green LED will turn on to indicate a valid link. This gives a good indication that the segment is wired correctly. The LED will BLINK when sending or receiving data. The LED will be OFF if there is no valid connection. The link status can also be seen in the *ControlEthernet* status screen.

4.1.4. Serial Port Connection

There are two serial ports provided, connections are accomplished by removing the front panel and using the Evertz standard rainbow cable. The COM connector is a 9-pin female 'D' connector for RS-232 serial communications. This port is configured for a ‘straight through’ RS-232 connection to a PC COM port and can be used for uploading firmware to the unit. Table 4-2 shows the pinout of the serial port in its default RS-232 DCE configuration. The connections are found at the front of the 7800MSC-IP card, to the left of the LED status display. The front-most connector (J24) is the traditional console COM port. Immediately behind the LED status display and to the right is the Front Panel Emulation port (J16), which allows a serial terminal with VT220 emulation to substitute for the front control panel on the 5700MSC-IP. Communication settings are 460,800 baud, no parity, 8 data bits and 1 stop bit.

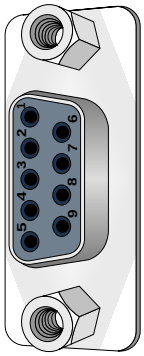


Pin #	Name	Description
1		
2	TxD	RS-232 Transmit Output
3	RxD	RS-232 Receive Input
4		
5	Signal Gnd	RS-232 Signal Ground
6		
7	RTS	RS-232 RTS Input
8	CTS	RS-232 CTS Output
9		

Table 4-2: COM Port Pin Definitions

4.1.5. GNSS Connection

A 9-pin female 'D' connector for connecting the GNSS receiver. Table 3-3 shows the pinout of the port. See section 4.5 for information about mounting and connecting the GNSS receiver.



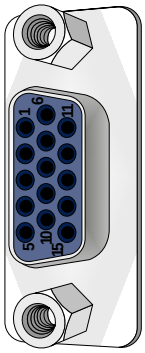
Pin #	Name	Description
1	GND	Chassis ground
2	Tx-	Transmit A (Tx-) Output
3	Rx+	Receive B (Rx+) Input
4	PPS+	1 PPS + Input
5	+VDC	+ 12 Volts DC out to supply GNSS receiver
6	PPS-	1 PPS - Input
7	Tx+	Transmit B (Tx+) Output
8	Rx-	Receive A (Rx-) Input
9	GND	Chassis ground

Table 4-3: GNSS Serial Port Pin Definitions

4.1.6. AUX Connections (available with 5700MSC-IP+AUX option)

4.1.7. GPIO, LTC Input, Secondary LTC Outputs

These connections are available with the 5700MSC-IP+AUX option. A 15-pin female 'D' connector provides two general purpose inputs, two general purpose outputs, secondary LTC1 and LTC2 outputs, and an LTC input. A 15-pin male-male cable is used for this purpose. The pinout of the GPIO connector is shown in Table 4-4.



Pin #	Name	Description
1	LTC Input -	Linear Time Code Input -
2	LTC1 Out -	Secondary Linear Time Code Output 1 -
3	LTC2 Out -	Secondary Linear Time Code Output 2 -
4	GPO 1	General Purpose Output 1
5	GPO 2	General Purpose Output 2
6	GND	Signal Ground
7	GND	Signal Ground
8	Syncro Tx	Syncro Transmit
9	Syncro Rx	Syncro Receive
10	GND	Signal Ground
11	LTC Input +	Linear Time Code Input +
12	LTC1 Out +	Secondary Linear Time Code Output 1 +
13	LTC2 Out +	Secondary Linear Time Code Output 2 +
14	GPI 1	General Purpose Input 1
15	GPI 2	General Purpose Input 2

Table 4-4: GPIO Pin Definitions

4.1.8. Unbalanced Audio Connections AES 1, 2 and 3 (available with 5700MSC-IP+AUX option)

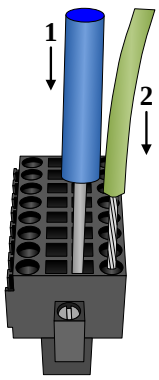
These three connectors provide unbalanced 48kHz AES audio compatible with the AES3-1992 and SMPTE 276M standards. Balanced versions of these signals are available on the AUDIO 16-pin terminal strip. The *AES Audio* sub-menu in the *OUTPUT* root menu is used to configure the AES audio outputs.

4.1.9. DARS OUT (available with 5700MSC-IP+AUX option)

This HD-BNC connector has an unbalanced 48kHz Digital Audio Reference signal (DARS) output compatible with the AES3-1992 and SMPTE 276M standards. A balanced version of this signal is available on the AUDIO 16-pin terminal strip. The *AES Audio* sub-menu in the *OUTPUT* root menu is used to configure the phase of the AES and DARS outputs.

4.1.10. Balanced Audio Connections (available with 5700MSC-IP+AUX option)

The **AUDIO** 16-pin terminal strip provides balanced versions of the AES1/AES2 and DARS signals as well as two balanced analog audio signals. The output audio cables can be secured into the removable portion of the terminal strip using a small screwdriver. The removable terminal block (Weidmuller part #174822) is then inserted into the rear panel and secured using the flange screws. The pinout of this connector is shown in Table 4-5.



Right +			Left +
Right -			Left -
GND			GND
SNSA			SNSB
GND			GND
AES 1 +			AES 1 -
AES 2 +			AES 2 -
DARS +			DARS -

Table 4-5: AUDIO Removable Terminal Block Pin Definitions

The *ANALOG AUDIO* sub-menu in the *OUTPUT* root menu is used to configure the analog audio outputs.

4.1.11. Test Generator Connections (SDTG, HDTG, 3GTG options)

There are four independent SDI test generators with a HD-BNC output. These produce SMPTE ST 259 serial digital video. The +**SDI-TG** and **+10G-TG** option adds support for HD video and 3G 3G Level-A and Level-B (SMPTE ST 424) to all four test generators.

HD-BNCs: SDI Test Generator 1 HD-BNC is labeled TG1
SDI Test Generator 2 HD-BNC is labeled TG2
SDI Test Generator 3 HD-BNC is labeled TG3
SDI Test Generator 4 HD-BNC is labeled TG4

4.1.12. Power Connections

The 5700MSC-IP has one or two (redundant supply is optional: 5700MSC-IP+2PS) auto-ranging power supplies that operate on either 95-125 or 185-260 volts AC at 50Hz or 60Hz. Power should be applied by connecting a 3-wire grounding type power supply cord to the power entry modules on the rear panel. The power cord should be minimum 18 AWG wire size; type SVT marked VW-1, maximum 2.5 m in length.

The IEC 320 power entry modules combine a standard power inlet connector and an EMI line filter.

CAUTION - TO REDUCE THE RISK OF ELECTRIC SHOCK, GROUNDING OF THE GROUND PIN OF THE MAINS PLUG MUST BE MAINTAINED

The EMI line filters in the 5700MSC-IP use the chassis ground as part of the circuit. This generates a small amount of AC leakage current to ground. In order to reduce risk of electric shock, the unit MUST be grounded properly through the ground connections on the AC power supply inlets.

4.1.13. M4 Grounding Stud

The M4 grounding stud is used to provide a ground point to the 5700MSC-IP chassis. It is located under the **REF IN LOOP** connectors. It can be used for protective earthing in installations that require it. An M4 or #8 ring terminal can be used with the provided M4 nut and lock washer.

4.2. MOUNTING AND COOLING

The 5700MSC-IP is equipped with rack mounting ears and fits into a standard 19 inch by 1 ¾ inch (483 mm x 45 mm) rack space. An optional rear support kit is available for rear mounting in a rack. The main board and power supplies are forced-air cooled by two fans in each power supply (or fan module). Both power supply slots must be occupied by a power supply or fan module at all times to ensure proper operating temperatures inside the unit. The air is drawn in through perforations along the edges of the front panel and exhausted out the sides of the unit. Ensure that the exhaust holes along the side of the unit are not blocked by rack supports or cabling otherwise the unit may overheat. A system fault is activated when the temperature inside the unit exceeds operating limits.

4.3. CONNECTING THE GENERAL PURPOSE INPUTS AND OUTPUTS

The 15-pin female **GPIO** connector on the 5700MSC-IP+AUX has 2 general purpose inputs and 2 general purpose outputs. The GPI inputs are active low. This means that if an input is floating (not connected) then it will not be activated. The GPIs can be activated by connecting the GPI input pin to Ground using a button, switch, relay or an open collector transistor. The GPIs can be configured to send out SNMP traps on activation.

The GPO outputs are internally pulled up to +5 volts DC. When a GPO activates, the GPO pin is pulled to ground. Care must be taken to limit the sink current to less than 50mA or damage to the GPO will result. The functions of the general purpose outputs are set using the *GPO 1 Mode* and *GPO 2 Mode* menu items on the *GENERAL* Setup menu. Note that in event of power being removed from the 5700MSC-IP, the GPOs will appear to be a 20K sink to ground.

4.4. CONNECTING TWO 5700MSC-IP UNITS IN SYNCRO MODE

When two 5700MSC-IPs are connected in a redundant configuration with an automatic changeover unit, it is necessary that both 5700MSC-IP units have the same timing and output settings. Identical timing for the 5700MSC-IPs is assured by locking both to the same frequency and phase source (e.g. GNSS or by genlocking one unit to the other). Ensuring that both 5700MSC-IPs have the same output configuration and time can be accomplished by implementing *syncro* between the two units.

The syncro link is automatically made when the GPIO connector of both 5700MSC-IP units is connected to the automatic changeover unit using male-to-male DB15 cables. Once the two units are connected, one must be designated the master unit and the other the slave. The slave unit will copy all the output menu settings from the master unit so that any change done on the master (such as changing a test pattern or phase offset) will also be applied to the slave. Additionally, the master 5700MSC-IP can be used as a time reference by the slave unit, with the time and date being transmitted through the syncro link.

To use syncro, the master 5700MSC-IP must be set to one of the master syncro modes. Likewise, the slave 5700MSC-IP must be set to a slave mode. When the master 5700MSC-IP has been configured to send syncro information and the slave 5700MSC-IP has been configured to receive it, the state of the link can be viewed on the slave unit by pressing the STATUS button and selecting the *Inputs* status screen. The slave unit will indicate *Syncro link ok*. When the link has been established, the slave unit can also set its time reference source to Syncro and will obtain time through the link as well as menu settings.

When syncro menu mode is active, all of the menu settings in the OUTPUT root menu are copied from the master 5700MSC-IP to the slave unit. The menu settings in the INPUT and GENERAL menus are not affected by syncro. In the OUTPUT menu the SDI TGs can be excluded from syncro. This can be done individually for each test generator.

4.5. GNSS RECEIVER INSTALLATION

The 5700MSC-IP unit is designed to work with the Trimble Acutime 360 antenna. The Smart Antenna houses the GNSS receiver, antenna, power supply and other support circuitry in a sealed, shielded, self-contained unit with a digital interface to the main unit. The GNSS Smart Antenna also receives power from the main unit through the connection cable.

4.5.1. Mounting the GNSS Smart Antenna

The smart antenna's enclosure is completely waterproof and is designed for outdoor installation. It is protected against interfering signals and thus is suitable for reliable operation in most environments. Select an outdoor location for the antenna, like the roof of your building that has a relatively unobstructed view of the sky. Dense wood and concrete or metal structures will shield the antenna from satellite signals. The antenna can receive satellite signals through glass, canvas and thin fibreglass; thus it may be mounted inside a skylight, if an outdoor location is not possible.

The smart antenna is an active-head antenna. For optimal performance, locate the smart antenna as far as possible from transmitting antennas, including radar, satellite communication equipment and cellular transmitters. When locating the antenna near a radar installation, ensure that the antenna is positioned outside of the radar's cone of transmission. Follow the same guidelines when installing the antenna near satellite communication equipment. For best results, mount the antenna at least ten feet away from satellite communication equipment. Do not mount the antenna near high vibration areas such as fan or motor housings, or near sources of heat such as exhaust stacks.

When mounting two or more smart antennas they must be spaced at least 3 feet (1 meter) apart to prevent interference.

Consider the length of the cable run when selecting the location. A 50 foot cable is supplied; however, longer cables are available on special order from the factory. You may also wire a straight-through extender cable to extend the able distance up to 200 feet. The smart antenna is designed for a pole mount with a 1" - 14 straight thread, which is a common marine antenna mount. For stationary installations a 3/4" pipe thread can be used, but a 1"-14 straight thread is recommended. Pole mounting is illustrated in Figure 4-2. Secure the mounting pole to a solid structure so that it is oriented vertically. Thread the smart antenna onto the pole or pile and hand tighten until snug.

CAUTION: Over-tightening the smart antenna on the pole or using a tool could damage the threaded socket in the base of the antenna. In addition, do not use thread-locking compounds, since they can dissolve or embrittle plastic.

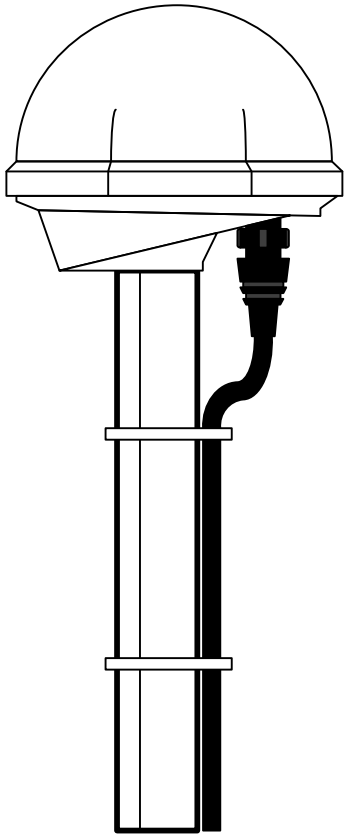


Figure 4-2: Pole Mounting the Smart Antenna

4.5.2. Connecting the GNSS Smart Antenna to the 5700MSC-IP

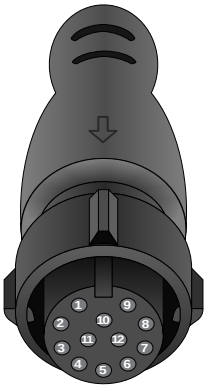
A standard 50 foot long interface cable (Evertz part WA-T09) is provided with the 5700MSC-IP and the smart antenna. One end of this cable is fitted with a weather-tight 12-pin Deutsch IMC21 connector. The other end is fitted with a 9-pin male sub-miniature D connector and should be connected to the GNSS connector on the rear panel of the 5700MSC-IP. The pinout of the cable is shown in Table 4-6. If you require a longer cable, a 100 foot (Evertz part WA-T76), 200 foot cable (Evertz part WA-T10), 400 foot cable (Evertz part WA-T11), 800 foot cable (Evertz part WA-08) or 1200 foot cable (Evertz part WA-T12) may be ordered from the factory. Custom length weatherproof cables can also be special ordered. Alternately, you can wire a 9-pin Extender cable as shown in Table 4-7.

Connect the 12-pin connector on the interface cable to the smart antenna. The connector on the interface connector has a locking ring for securing the connection.

CAUTION: Over tightening the locking ring can damage the connector on the smart antenna. Fasten finger-tight until snug. Using tools will damage it.

Route the interface cable to the location of the 5700MSC-IP unit using the most direct path. Avoid routing the cable near hot surfaces, sharp or abrasive surfaces, or corrosive fluids or gases. Avoid sharp kinks or bends in the cable. Additional protection such as heat shrink tubing may be required to protect the cable jacket at points where the cable enters the building, especially if the opening is rough or sharp. Once the cable is run, use cable-ties to secure the cable to the pole and to provide strain relief for the connections. When securing the cable, start at the antenna and work towards the 5700MSC-IP unit. Connect the 9-pin male D connector to the GPS connector on the rear panel of the 5700MSC-IP. Power is provided from the 5700MSC-IP along the interface cable to the smart antenna.

It is best to keep the antenna cable run as short as possible. If two 5700MSC-IP units are being used, each with their own GNSS antenna, the antenna cable lengths should be matched as closely as possible.



Trimble Antenna Deutsch IMC-series 12-pin (female)		Cable Wire	Evertz 5700MSC-IP 9-pin D-Sub (male)	
DC Ground	9	Black	1	Chassis Ground
Receive Port (Rx-)	2	Violet	2	Tx A -
Transmit Port (Tx+)	5	Yellow	3	Rx B +
Timing Pulse (1pps+)	11	Orange+White	4	1pps + in
DC Power	1	Red	5	+12 V DC
Timing Pulse (1pps-)	12	Black+White	6	1pps - in
Receive Port (Rx+)	3	Orange	7	Tx B +
Transmit Port (Tx-)	4	Brown	8	Rx A -
	----	Drain Wire	shell	

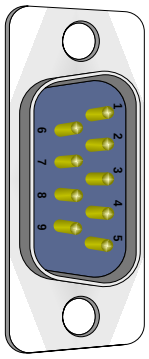
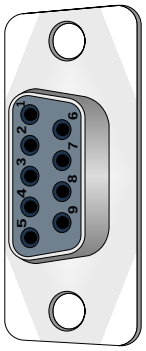


Table 4-6: Evertz-provided GNSS Cable (part WA-T09) Internal Wiring



9-pin Female D-Sub Pin	Cable Pair	9-pin Male D-Sub Pin	Description
7	1	7	TX B +
2		2	TX A -
8	2	8	RX A -
3		3	RX B +
4	3	4	1 PPS +
6		6	1 PPS -
5	4	5	+12 V DC
1		1	Ground
----------	Drain	----------	Shield

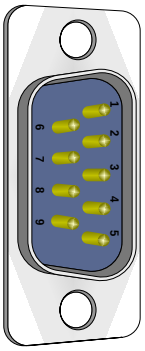


Table 4-7: Accutime Gold Extender Cable

When making your own extender cable be sure to use low capacitance twisted pair cable and adhere to the pairing shown in Table 4-7.

4.5.3. System Start-Up

At power up, the smart antenna will automatically begin to acquire and track the GNSS satellite signals. From a cold start, the smart antenna will normally take from 2 to 5 minutes to lock on to sufficient satellites to accurately determine the time. During this time the *Lock Status* and *Inputs* status screens on the front panel will show the various stages of initialization.

5. OPERATION

This section of the manual is currently under development and is subject to change. Missing heading and field descriptions will be added in the upcoming revision.

The model 5700MSC-IP IP Network Grand Master Clock and Video Master Clock System combines the latest LSI technology with sophisticated embedded microcontroller firmware to provide a powerful, flexible, and upgradeable system. This combo IP Network Grand Master Clock and Master Sync Generator is ideal for timing today's IP based video broadcast, production, and distribution facilities. It provides all of the future timing needs of an IP based plant while providing precision reference to any baseband SDI/Analog systems.

5.1. FRONT PANEL CONTROLS

Figure 5-1: Model 5700MSC-IP Front Panel Layout

The front panel controls consist of two color LCD displays, 10 pushbuttons and a control knob. The buttons are used to navigate the front panel menu system, view status information, and to change various settings on the unit. The control knob can also be used to navigate the menu system and make changes to settings. Pressing in the control knob is equivalent to pressing the **SELECT** button in most cases. Press the **HELP** button at any time to view information on any currently selected menu item.

The two color LCD displays are used to display the menu system and the current position within the menu tree. There are also messages on the left LCD that indicate system status.

5.1.1. Front Panel Buttons

There are four buttons to the right of the control knob that are used to select the four main root menus. These buttons are labelled **INPUT**, **OUTPUT**, **GENERAL**, and **STATUS**. These buttons will illuminate to show which menu is currently active. The control knob and the four green buttons to the left, ↑, ↓, **SELECT**, and **ESC**, are used to navigate the menu system and change settings. The **PANEL LOCK** button can be used to lock the front panel to prevent accidental button presses after the unit has been configured. The **HELP** button can be pressed at any time to display online help about the currently selected menu or menu item.

INPUT - Enters the *INPUT* menu that contains various menus for configuring the frequency and time references of the 5700MSC-IP and how to lock to them.

OUTPUT - Enters the *OUTPUT* menu that is used to configure the Sync and test generator outputs of the 5700MSC-IP.

GENERAL - Enters the *GENERAL* menu that contains controls for configuring the Syncro, GPOs, DST, SNMP, and NTP features of the 5700MSC-IP.

SELECT - In the menu system the **SELECT** button is used to enter a sub-menu or to select a menu parameter that is to be changed.

ESC - When in a sub-menu the **ESC** button is used to exit the next higher menu level. It is also used to abort changing the setting of a menu item.

↑, ↓ - The arrow buttons are used to navigate through the menu system. The currently selected menu item is indicated by the **>** character. The arrow buttons are used to select the next or previous menu item. When changing a menu item's value, the arrow buttons are used to select the next or previous items in a list, or for a numerical value are used to increment or decrement the current value.

CONTROL - The control knob can be used as an alternative to the ↑ and ↓ buttons and allows quicker navigation and setting of menu items. Turning the control knob clockwise (to the right) has the same effect as pressing the ↑ button. Turning the control knob counter-clockwise (to the left) has the same effect as pressing the ↓ button. Depressing the control knob inwards has the same effect as pressing the **SELECT** button. When changing a numerical value (such as when phasing an output) depressing the knob while turning allows changing the numerical value in steps of 16. This makes it easier to change large numerical values.

When in the menu or a selection list, pressing the control knob has the same effect as pressing the SELECT button. When adjusting a numerical value, depressing the control knob while turning it will increment or decrement in larger steps of 16.

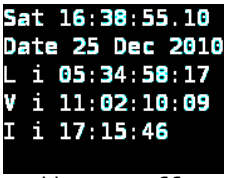
5.1.2. The Status Screens

There are several status screens available on the 5700MSC-IP that can be accessed by pressing the **STATUS** button on the front panel. Each screen displays relevant information about the subsystem it represents. At the root level, the screens are listed just like menu items. Press the ↑ and ↓ buttons or turn the control knob to move the selection cursor to the desired status screen. Press **SELECT** to view the status screen. The **ESC** button will return to the status screen list.

The status screens are still accessible even when the front panel is locked.

The status screen list can be used to quickly locate the source of a fault within the 5700MSC-IP. By scrolling through the status screen list, any faults can be quickly identified. The status screens are described in detail below. Each status screen can display multiple messages depending on the configuration of the 5700MSC-IP.

System / In time



hh:mm:ss:ff

The *System/In time* status screen shows the system clock time and date on the first two lines.

The third line, prefixed with "L i", shows the current LTC timecode being read from the LTC/IRIG input (if present). If the LTC input is lost, the time shown here will be replaced with "--:--:--:--". If drop frame is detected, the last colon ':' will

be replaced with a period '.'.

The fourth line, prefixed with "V i", shows the current timecode being read from VITC on the reference input. If the VITC input is lost, the time shown here will be replaced with "--:--:--:--". If drop frame is detected, the last colon ':' will be replaced with a period '.'.

The fifth line, prefixed with "I", shows the current IRIG timecode being read from the LTC/IRIG input (if present). If the IRIG input is lost, the time shown here will be replaced with "--:--:--:--".

Sync 1-6

The *Sync 1-6* status screen shows the VITC clocks for the sync outputs in "hours:minutes:seconds:frames" format. The delimiter between the hours and minutes indicates whether Daylight Saving Time is being applied to that output. It will be a period "." when DST is enabled and a colon ":" otherwise. The delimiter between the seconds and frames indicates whether dropframe counting is being used on the VITC output. It will be a period "." when dropframe counting is enabled, and a colon ":" otherwise.

hh:mm:ss:ff

In the example to the left, the VITC on sync output 1 has been set to Eastern Standard Time (Time Zone to UTC –5:00) and has DST enabled (1 hour advanced). Sync outputs 1 to 3 are all in dropframe counting mode. The timecode clocks for sync outputs 5, 6, and 7 are dimmed because they are set to an output mode which doesn't support VITC. Although VITC is not being inserted onto these sync outputs, the timecode clocks continue running.

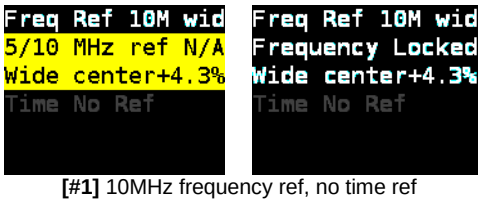
SDI TG 1-4

Image will be added in upcoming release

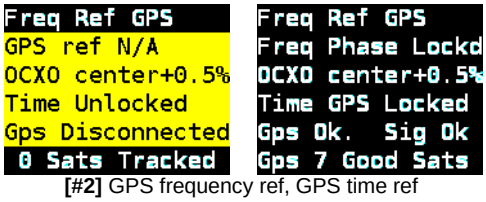
The *SDI TG 1-4* status screen shows the clocks for each of the test generator burn-in displays in "hours:minutes:seconds:frames" format. The delimiter between the hours and minutes indicates whether Daylight Saving Time is being applied to that output. It will be a period "." when DST is enabled and a colon ":" otherwise. The delimiter between the seconds and frames indicates whether dropframe counting is being used on the time output. It will be a period "." when dropframe counting is enabled, and a colon ":" otherwise.

Lock status

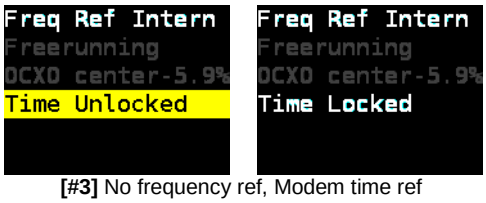
Unlocked → Locked



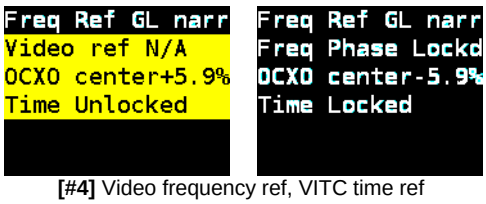
[#1] 10MHz frequency ref, no time ref



[#2] GPS frequency ref, GPS time ref



[#3] No frequency ref, Modem time ref



[#4] Video frequency ref, VITC time ref

The *Lock Status* screen displays the current status of the selected frequency and time references for the 5700MSC-IP.

The first line indicates which frequency reference has been selected, and if the unit is using the narrow or wide oscillator.

The second line shows the overall lock status of the 5700MSC-IP to the selected frequency reference. This line will display "`Lock progrs x%`" while locking to show the current progress in locking the oscillator to the reference. This line also indicates if the 5700MSC-IP has locked to frequency only, or has both frequency and phase locked to the reference.

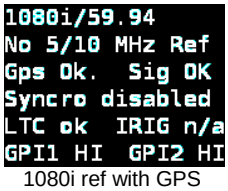
The third line indicates the current tuning position of the selected oscillator when locked to the reference.

The fourth line displays the current lock status of the system clock to the time reference.

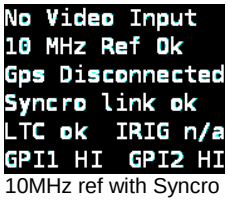
The fifth and sixth lines display the status of the GNSS receiver when GNSS has been selected as a frequency or time reference. The fifth line displays the current GNSS lock state, and the sixth line displays how many healthy satellite signals the GNSS antenna is receiving.

Inputs

NTSC ref with GPS



1080i ref with GPS



10MHz ref with Syncro

The *Inputs* status screen displays the status of the reference inputs, syncro link, and General Purpose Inputs.

The first line displays the name of the detected video reference that is present on the reference loop input.

For NTSC-M and PAL-B black burst references, an approximate Subcarrier to Horizontal (SCH) measurement of the input will be shown. If the SCH error is greater than 35º, this line will alternate between "`(SCH>35)`" and "`H-lock`" to indicate that the 5700MSC-IP has fallen back to locking to horizontal sync only. If the burst phase cannot be measured reliably, it will display "`unlockable`".

The second line displays the detection of a 10MHz or 5MHz continuous wave (CW) frequency on the reference loop input.

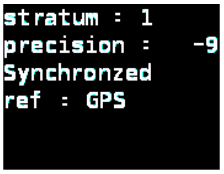
The third line displays the current status of the GPS receiver. This is the same status that is displayed on line 5 of the *Lock Status* screen.

The fourth line shows the current status of the syncro link (if enabled) that is available when two 5700MSC-IP units are connected through an automatic changeover unit.

The fifth line displays the status of the LTC/IRIG input. If LTC is present it will show "`LTC ok  IRIG n/a`". If IRIG is present it will show "`LTC n/a IRIG ok`"

The sixth line shows the status of the General Purpose Inputs. These GPI inputs are activated by connection to ground. The status will be "`GPI1 LO`" or "`GPI2 LO`" when either GPI has been activated.

NTP



The *NTP* status screen displays information about the NTP server. It shows stratum, precision, lock status, and reference.

It will also show if there are issues with the NTP. The HELP button will offer suggestions if there is a configuration issue. If the NTP server is Not Synchronized the lock indicator alarm bit (LI_ALARM) will be set in outgoing packets. This may cause clients to refuse to synchronize to the NTP server.

Press HELP for more information on the current status.

Options Firmware

Image will be added in upcoming release

The *Options Firmware* status screen displays information about the installed options in the 5700MSC-IP as well as the current firmware version.
The last line shows the current firmware version and build number that is installed in the 5700MSC-IP in the format of: `Version X.X Build XX`.

5.1.3. Panel Lock Function

Pressing the **PANEL LOCK** button will lock the front panel. The **PANEL LOCK** button will illuminate indicating that the front panel keys are disabled. This is used to prevent accidental changes to the unit once it has been configured. While the front panel is locked, the STATUS screens will still be accessible. It will still be possible to press the STATUS button and view the various status screens but it will not be possible to enter any other menu or change menu items. To unlock the panel, press the **PANEL LOCK** button while holding the SELECT button. The front panel will return to normal operation and the **PANEL LOCK** button LED will turn off. Note that pressing HELP and **PANEL LOCK** at the same time will also turn off the panel lock.

5.1.4. Front Panel LCD Displays

There are two full color LCD displays on the front panel. The left LCD indicates the current position in the menu structure as well as system health status. The right LCD is used to display the menu system and status screens.

The left LCD display shows the current position in the menu tree. In the bottom-left corner the system status is shown. A critical fault will appear in red blinking text. The possible system status messages are summarized in Table 5-1 in order of severity:

Message	Description
Hw fail	Appears blinking red in the bottom-left corner. Indicates that an internal hardware problem has been detected. It is advisable not to remove power from the unit and to contact the factory immediately.

Temp Hi	Appears blinking red in the bottom-left corner. Indicates the internal temperature of the unit has exceeded operating limits. Requires immediate attention. May be due to excessive ambient temperature, fan failures, missing power supply or fan module, or blocked exhaust vents on the side of the unit.
Ps fail	Appears blinking red in the bottom-left corner. Indicates that one of the power supplies is not producing the correct voltage. Only applicable for dual power supply installations. If only a single power supply is in use, make sure the *Number PS* menu item is set correctly.
Warning	Appears in yellow text in the bottom-left corner. Indicates a non-critical fault in the unit such as frequency or time reference missing, or fan failure.
Sys Ok	Appears in green text in the bottom-left corner. Indicates no system fault.

Table 5-1: System Status Messages

In the bottom-right corner of the left LCD the frequency reference status is shown. When ***Ref Ok*** is displayed this means the currently selected frequency reference is present and the 5700MSC-IP has locked to it properly. This will be ***Ref unlk*** with a yellow background if the frequency reference is missing or the 5700MSC-IP is unable to lock to the supplied reference.

Other messages are possible on the left LCD. These messages require a manual user jam, or mode change to clear. Such messages include ***REF JAM NEEDED***, which will be displayed if the 5700MSC-IP is in *Slow* mode and is in the process of gradually relocking to a change in the frequency reference. If the time reference lock type has been set to *USER*, then ***TIME JAM NEEDED*** will be displayed when the system time and reference time mismatch.

5.2. FRONT PANEL MENU SYSTEM

The 5700MSC-IP menu system consists of three root menus. The **INPUT, OUTPUT**, and **GENERAL** buttons allow you to quickly go to each of the three main menus, while the **SELECT, ESC, ↑** and **↓** buttons and control knob are used to navigate the menu.

To enter the Input menu, press the **INPUT** button, which will then illuminate to show that it is now the active menu. Likewise the Output or General menus can be entered by pressing the **OUTPUT** or **GENERAL** buttons. The menu selections will be displayed on the right LCD. The **>** character is used as a selection cursor to show which menu item is currently selected. Use the **↑** and **↓** buttons or turn the control knob to move the **>** character beside the desired sub-menu and press the **SELECT** button to enter it. The menu tree is shown on the left LCD and identifies which menus have been entered. Press the **ESC** button to return to the previous level in the menu structure.

When a menu item is selected, there can be several different formats to modifying the value of the selected setting. The most common is the selection list. In a selection list, the currently active value is highlighted in white. The **>** character can be moved to select a new value, but the change won't take effect until the **SELECT** button is pressed, after which the new value will become highlighted to show it is now active. Press the **ESC** button at any time to exit from the selection list. Other formats are used for changing numeric items.

When accessing some menu items, the message ***LIVE CONTROL*** will be displayed on the left LCD with a red background. This message is a warning that pressing SELECT on the menu item will perform an immediate task such as jamming a reference. Use caution with such menu items.

When adjusting the value of some settings, the message LIVE CONTROL will be displayed on the left LCD with a yellow background. This message is a warning that any change made with the ↑ and ↓ buttons or control knob will immediately be applied to the output without requiring the **SELECT** button to be pressed. An example is when adjusting phase of the sync outputs or when adjusting the analog audio levels. Proceed with caution and press the **ESC** button to return to the previous menu without making a change.

5.3. CONFIGURING THE INPUT REFERENCES

The *INPUT* menu is used to set up various items related to the input references of the 5700MSC-IP. The chart below shows the items available in the *INPUT SETUP* menu.

Frequency Ref	Contains items controlling the frequency reference and how to lock to it
Time	Contains items related to the time reference and how to lock to it
Jam Input	Contains live controls that can force the 5700MSC-IP to lock immediately to the frequency or time reference

Table 5-2: Root Level of the *INPUT* Menu

5.3.1. Configuring the Frequency Reference

5.3.1.1. Selecting the Reference Source

INPUT
Frequency Ref
Reference Src
GNSS Mobile
GNSS Fixed
Ten MHz
Video
Internal
1588

The *Reference Src* menu item in the *Frequency Ref* menu is used to select the frequency reference that the 5700MSC-IP will use to lock its internal oscillator. All outputs are driven from a common oscillator and therefore are clock locked to each other (i.e. they do not drift with respect to each other). When set to the different possible reference sources and the appropriate reference is supplied, the phasing of the video and DARS outputs is affected.

When set to *GNSS* the 5700MSC-IP will lock its ovenized oscillator to the 1pps pulse from the GNSS smart antenna. Selecting this option forces the *Genlock Range* to Narrow. All outputs are phased with respect to a specific date in GNSS time. This forces the time reference to GNSS time. The GNSS-disciplined internal oscillator will maintain superb long-term accuracy.

When set to *Ten MHz* the 5700MSC-IP will look for a 10MHz or 5MHz frequency reference on the reference loop input. It will lock in either Narrow or Wide mode, depending on the *Genlock Range* setting. The 10MHz or 5MHz reference supplies no phase information and the phase of the outputs will change if the unit is powered down and rebooted. The phase between different 5700MSC-IP units locked to 5MHz or 10MHz will not be the same.

When set to *Video* the 5700MSC-IP will lock to a valid black burst or tri-level video signal applied to the reference loop inputs. The *Genlock Range* menu item is used to select the tolerance of the master oscillator lock range. Note that the 5700MSC-IP requires a colorburst on NTSC and PAL references, with a SCH error of less than 35º. Burst is not required for Slo-PAL bi-level references.

When set to *Internal* the 5700MSC-IP will free-run on its internal ovenized oscillator. This forces the *Genlock Range* to Narrow. The stability of this ovenized oscillator is 0.01ppm, which corresponds to a time drift of about 0.31 seconds per year.

5.3.1.2. Configuring the Genlock Capture Range

INPUT
Frequency Ref
Genlock Range
Narrow
Wide

The *Genlock Range* menu item is used to select the type of oscillator to use when locking to video or 5/10MHz references.

Set this to *Narrow* to use the ovenized oscillator when the frequency stability of the reference is tightly controlled and within ±0.1 ppm. The ovenized oscillator provides excellent stability and enables use of the *Slow* lock mode. The *Slow* lock mode allows the 5700MSC-IP to recover smoothly from a loss of reference or reference shift condition. The Narrow range is superior to the Wide range in every way except in lock time and lock range. It is the default setting and does not normally need to be changed.

Select the *Wide* range only when a wide locking range of ±15ppm is required and when very fast lock times are needed. This may be required in some post-production facilities where the input reference is changing occasionally and a fast relock time is desired. Low freerun stability and slightly higher jitter are the drawbacks of the wide range.

5.3.1.3. Selecting the Frequency Reference Lock Type

INPUT
Frequency Ref
Lock Type
Slow
Abrupt

The *Lock Type* menu item is used to select how the 5700MSC-IP will relock to its frequency reference when the reference is lost and then regained, or experiences a change.

In *Abrupt* mode, whenever the 5700MSC-IP detects that its internal oscillator is no longer synchronized to the reference it will make a sudden change to bring it back into lock. This may cause disturbances to the outputs as the unit shifts its frequency and phase.

In *Slow* mode, when the 5700MSC-IP detects that its internal oscillator is not synchronized to the reference it will report *REF JAM NEEDED* on the LCD display and optionally send an SNMP trap. The unit will then slowly adjust its internal oscillator to bring it back into lock with the reference. This gradual correction will not cause any disturbances to the outputs as they re-phase. This adjustment may take a long time, depending on the size of the discrepancy between the internal oscillator and reference. If the unit is required to lock to its reference without delay the user can perform a manual jam by selecting the *Jam Input* menu item. The *Slow* lock type is only available if the *Genlock Range* is set to *Narrow*.

If a large shift in the reference occurs while Slow lock mode is enabled, the outputs of the 5700MSC-IP may be out of phase for a long time while relocking. The 5700MSC-IP will gradually slew its oscillator to bring it back into phase with the reference. This slewing action combined with the phase shift may seem to indicate that the unit is completely unlocked to the reference. This is not a fault and a manual jam can be performed to force the 5700MSC-IP to lock immediately.

5.3.2. Configuring the Time Inputs

5.3.2.1. Selecting the Time Reference

INPUT
Time
Reference Src
GNSS
LTC
VITC
None
IRIG
SNTP
1588

The *Reference Src* menu item in the *Time Reference Src* menu is used to select the time reference that the 5700MSC-IP will use to lock its internal clock. All outputs are driven from this common time source

When set to GNSS, time data is obtained from the GPS and / or GLONASS satellite constellations. This is the most accurate source of time reference available

When set to LTC, the 5700MSC-IP obtains time from an LTC clock wired to its LTC input.

When set to VITC, the 5700MSC-IP obtains time from Video reference wired to the Reference Loop Thru HD-BNC connectors, or Frame Reference 1 or Frame Reference 2 BNC connectors, depending on how the Frequency Reference Genlock Source is configured. Note that this Video reference can only be NTSC-M or PAL format, and must have VITC time code present.

When set to None, the internal clock of the 5700MSC-IP is in “free run” state, and regulated by the extremely accurate ovenized oscillator, resulting in a drift of less than one millisecond per day.

When set to IRIG, the 5700MSC-IP obtains time from the LTC input using the IRIG protocol.

When set to SNTP, the 5700MSC-IP obtains time via any of its network interfaces (Gigabit Ethernet 1, Gigabit Ethernet 2, 10G Ethernet 1, 10G Ethernet 2 and Frame Ethernet) from the first available configured SNTP server.

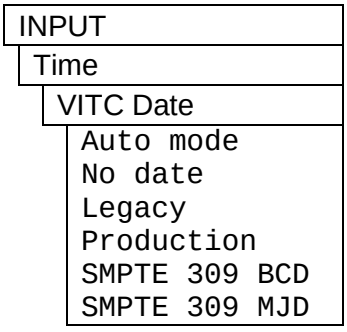
When set to 1588, the 5700MSC-IP obtains time from the best available PTP Master found on its network interfaces: Gigabit Ethernet 1, Gigabit Ethernet 2, 10G Ethernet 1, 10G Ethernet 2 and Frame Ethernet. The PTP BMCA (Best Master Clock Agorithm) is used to establish which PTP clock in each PTP domain assumes the role of active PTP Master, while all other potential masters enter into a passive state. The network interface on this 5700MSC-IP that is used to lock to a PTP Master will enter into Slave state.

5.3.2.2. Setting the VITC Reader Line

INPUT
Time
VITC Line
New Value
Set Value

This menu item is used to specify which line on the black burst reference input the VITC will be read from. The VITC that is read from the reference input can be viewed in the STATUS menu on the *System/In time* status screen.

5.3.2.3. Setting the VITC Date



This menu item is used to select how the 5700MSC-IP will decode date information from the user bits of the VITC inputs. It is only valid when the time reference source is set to VITC.

When set to *Auto mode*, the 5700MSC-IP will analyze the incoming user bits to try to find the best date format. Use caution with this as some random data, including all 0s will look like a valid Legacy date format.

Select *No date* to ignore the user bits of the incoming VITC. This means that if the time reference is set to VITC the date must be set manually in the GENERAL menu.

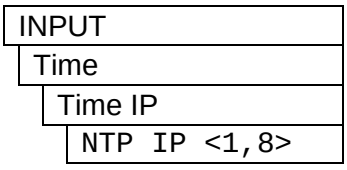
Select *Legacy* to decode the date in a format compatible with Leitch master clock systems.

Select *Production* to decode the date in a format compatible with timecode smart slates used in film and television production. In this mode the date is encoded as yymmddrr, where rr is the nominal frame rate of the respective output (30 for 29.97Hz outputs).

Select *SMPTE 309 BCD date* to decode the date in the SMPTE ST 309 standard Binary Coded Decimal mode. In this mode the date is encoded as zzyymmdd, where zz is the time zone of the respective output.

Select *SMPTE 309 MJD date* to decode the date in the SMPTE ST 309 standard Modified Julian Date mode. In this mode the date is encoded as zzdddddd, where zz is the time zone of the respective output and dddddd is the date expressed in its Modified Julian Date representation.

5.3.2.4. Setting the Time IP



This menu item enables or disables the eight servers that can be used as an SNTP time reference. These are valid only when the time reference has been set to SNTP.

Up to 8 servers can be set up. During the daily time sync to SNTP, the 5700MSC-IP will contact each server that is enabled and chose the one with the best time, based on the data provided by the servers.

5.3.2.5. Setting the Time Reference Lock Type

```
INPUT
  Time
    Lock Type
      User
      Never
      Always
      Daily
```

The *Lock Type* menu item is used to control how and when the 5700MSC-IP updates its system time to match the time reference. This decision is made whenever the system time is in disagreement with the time reference.

Select *User* when user intervention is required before updating system time. When the 5700MSC-IP system time does not match the time reference a warning will be displayed on the front panel (TIME JAM NEEDED), which can optionally trigger an SNMP trap. The user must initiate a manual jam of reference time into system time using the *Jam Time* menu item in order to get system time to match the time reference.

Select *Never* to ignore the time reference completely unless the user performs a manual jam. No warnings are generated in this mode.

When set to *Always* the system time of the 5700MSC-IP will constantly track the time reference. Any change in the time reference will be immediately applied to the system time of the 5700MSC-IP.

If *Daily* is selected, the 5700MSC-IP system clock will run independently from the time reference and *jam* once daily at the time of day specified by the *Input Jam Time* control.

If the time reference has been set to SNTP, the time lock type is forced to Daily, no matter what this control has been set to.

5.3.2.6. Setting the Daily Jam Time for the Time Reference

```
INPUT
  Time
    Input Jam Time
      Input Jam Time

         0:00
```

When the *Lock Type* is set to *Daily*, the 5700MSC-IP system time will run independently from the time reference and *jam* to it once a day. This menu item is ignored if the *Lock Type* is set to anything other than *Daily*.

If the time reference is set to SNTP then this sets the time to do a daily SNTP synchronization, and the Lock Type is not applicable.

Enter the time of day in 24-hour format that the 5700MSC-IP should perform this daily jam. When the jam occurs, the update will ripple to all output timecode clocks. The NTP server and IRIG outputs will also be affected. The time specified should be during a period when it will have a minimum effect on system operation.

5.3.3. Configuring the Jam Input

These menu items allow the user to initiate an immediate forced synchronization of the master system oscillator to its frequency reference, or the system time to its time reference.

CAUTION: These controls perform an immediate action once the SELECT button is pressed. The text "Live control" will be shown on the left LCD with a red background as a warning.

5.3.3.1. Synchronizing the System Oscillator to the Reference Immediately

INPUT
Jam Input
`Jam Reference`

This action will only be required when the frequency lock type has been set to *Slow*. In *Slow* mode, the 5700MSC-IP can only gradually adjust its internal oscillator if it becomes unsynchronized to the frequency reference. This can occur if the frequency reference is disconnected for a period of time. The internal oscillator will drift slightly and upon reconnection a slight difference will exist between the two.

The slow lock process can take a long time. To resolve this discrepancy immediately, the user can initiate a manual jam of the frequency reference. The word *jam* here is used in the context that the timing and phase measured on the reference will be jammed into the system oscillator forcing it into synchronization. This can cause glitches on all outputs of the 5700MSC-IP and should be used with caution.

To perform a jam of the frequency reference, select the *Jam Reference* menu item and press the **SELECT** button.

5.3.3.2. Synchronizing the System Time to the Reference Immediately

INPUT
Jam Input
`Jam Time`

Performing a manual jam of the time reference will only be required when the time lock type is set to *User* or *Never*. In User mode the 5700MSC-IP will warn whenever system time does not agree with the time reference. When the lock type is *Never*, the 5700MSC-IP will ignore the time reference completely and not generate any warnings. Performing a manual jam with this menu item is the only way to synchronize the system clock to the time reference. The word *Jam* is used in the context that the time and date provided by the time reference will be jammed into the system time clock to synchronize them.

Note that if the time reference is set to SNTP then this forces an immediate SNTP synchronization.

To perform a jam of reference time/date into system time, select the *Jam Time* menu item and press the **SELECT** button.

When performing a frequency or time reference jam, allow 10 seconds for any jam warning messages to clear.

5.4. CONFIGURING THE OUTPUTS

The *OUTPUT* menu is used to configure the various outputs of the 5700MSC-IP. The chart below shows the items available in the *OUTPUT* menu.

SYNC 1
SYNC 2
SYNC 3
SYNC 4
SYNC 5
SYNC 6
TG 1-4 Settings
TG 1
TG 2
TG 3
TG 4
IP TG Settings
TG5, IP 1a
TG6, IP 1b
TG7, IP 1c
TG8, IP 2a
TG9, IP 2b
TG10, IP 2c
Global Pedestal
Waveform Anchor
Global Phasing
WC Lock
WC Phase

Table 5-3: Top Level of the Output Setup Menu

5.4.1. Configuring the Sync Outputs

5.4.1.1. Selecting the Standard of the Sync Outputs

OUTPUT
- Sync <1,6>
  - Mode
    - PAL-B
    - NTSC-M
    - 1080i/50
    - 1080i/59.94
    - 1080i/60
    - 1080p/23.98
    - 1080p/28.98sf
    - 1080p/24
    - 1080p/24sf
    - 1080p/25
    - 1080p/29.97
    - 1080p/30
    - 1080p/50
    - 1080p/59.94
    - 1080p/60
    - 720p/24
    - 720p/30
    - 720p/50
    - 720p/59.94
    - 720p/60
    - 625i/48
    - 625i/47.95
    - 480p/59.94
    - 576p/50
    - PAL color farme
    - 1 Hz
    - 1/1.001 Hz
    - 6/1.001 Hz
    - IRIG datum
    - 5 MHz
    - 10 MHz
    - NTSC-M subcar.
    - PAL-B subcar.
    - Wordclock
    - Test Be
    - Test Cha
    - Test Delt
    - Test Echos
    - Test S/W DDS

This menu item sets the format of the sync output. All sync outputs are fully configurable.

The PAL-B and NTSC-M selections are black burst outputs compliant with SMPTE ST 318. When either of these standards is selected, Vertical Interval Time Code can be inserted onto two lines of the VBI. A ten-field reference can also be inserted onto line 15 of the NTSC-M color black output.

There are numerous HD tri-level standards that can be output compliant with SMPTE ST 274, SMPTE ST 296, and SMPTE ST 292-1.
For 1080p/25sF use the 1080i/50 format
For 1080p/29.97sF or 1035i/59.94 use the 1080i/59.94 format
For 1080p/30sF or 1035i/60 use the 1080i/60 format

The 625i/48 and 625i/47.95 selections are “slow PAL” signals, which are sync only bi-level formats synchronous to 24Hz and 23.98Hz rates.

The pulse formats consist of various timing signals that can be used to line up signals with different timing. The *PAL color frame* pulse occurs during field 1 of the PAL-B 8-field color sequence. The *1Hz* pulse occurs once per second at the beginning of the second and indicates the point where the vertical syncs of 60Hz and 50Hz HD sync formats are coincident. The *1/1.001 Hz* pulse occurs nominally once per second at the beginning of the second and indicates the point where the vertical syncs of 59.94Hz and 23.98Hz HD sync formats are coincident and is also aligned with NTSC color field 1. The 6*/1.001 Hz* pulse occurs nominally six times per second and indicates the point where the vertical syncs of 59.94Hz and 23.98Hz HD sync formats are coincident. The *IRIG datum* pulse will be aligned with the IRIG outputs and the rising edge indicates the start of the IRIG reference bit. The pulse type is controlled by the *Pulse type* menu item.

Wordclock is a 48kHz sampling rate clock that can be phased separately to the AES/DARS outputs.

The continuous wave formats output a sine wave at different frequencies. If the unit is locked to a black burst frequency reference the subcarrier outputs will be lined up with the reference.
NTSC-M subcarrier = NTSC CW subcarrier frequency at 3.58MHz nominal.
PAL-B subcarrier = PAL-B CW subcarrier frequency at 4.43MHz nominal.
5 MHz = Continuous sine wave at 5MHz.
10 MHz = Continuous sine wave at 10MHz.

5.4.1.2. Configuring the VITC Generator for the Color Black Outputs

5.4.1.2.1. Enabling VITC on the Video Output

```
OUTPUT
  Sync <1,6>
    Vitc Ctl
      Off
      On
```

This menu item controls whether Vertical Interval Time Code will be inserted into the vertical blanking interval of the sync output.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will disabled for other formats (shown in dark text).

5.4.1.2.2. Selecting the VITC Insertion Lines

```
OUTPUT
  Sync <1,6>
    Vitc Line 1
      line 1 = 14
    Vitc Line 2
      line 2 = 16
```

These menu items select the lines onto which the VITC will be inserted when the *Vitc Ctl* menu item is set to *On*. If only one line of VITC is desired, set both menu items to the same line.

The default line values for NTSC-M are lines 14 and 16.
The default line values for PAL-B are lines 17 and 17 (same line).

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will be disabled for other formats (shown in dark text).

5.4.1.2.3. Enabling Dropframe Counting for NTSC VITC

```
OUTPUT
  Sync <1,6>
    Dropframe Ctl
      Off
      On
```

This menu item allows the user to control whether the dropframe counting mode will be used for the VITC inserted onto the sync output.

This menu item is only applicable to the NTSC-M format and will be disabled for all other formats (shown in dark text).

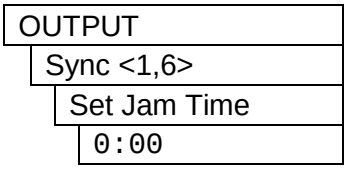
5.4.1.2.4. Enabling Colorframe Alignment of VITC

```
OUTPUT
  Sync <1,6>
    Color Frame
      Color Frame Off
      Color Frame On
```

This menu enables or disables color frame alignment of VITC timecode to the black burst sync it is being embedded on. This menu item is only applicable when the sync mode is NTSC-M or PAL-B.

When turned on, the Color Frame bit in VITC will be set to indicate that color frame alignment is being performed. The VITC timecode count will be adjusted to maintain a correlation to the color field it is inserted on according to SMPTE ST 12-1.

5.4.1.2.5. Selecting When the VITC Time is Synchronized to the System Time



This menu item allows the user to set the time of day when the VITC on the sync output will be synchronized to the system time. This synchronization is necessary once per day to maintain a long-term correlation between the VITC time and system time for the NTSC-M sync format.

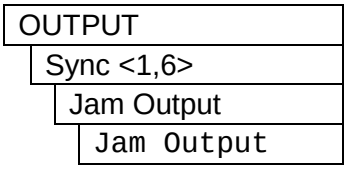
When the time reference is set to *GPS*, the VITC output time will have to be synchronized to the system time to correct for leap seconds. This affects both NTSC-M and PAL-B formats.

Enter the hour and minute with the ↑ and ↓ buttons or by turning the control knob.

The VITC can also be synchronized to system time immediately using the *Jam Output* menu item. All LTC and VITC timecode outputs can be synchronized to system time in one shot using the *Jam all VitcLtc* menu item.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will disabled for other formats (shown in dark text).

5.4.1.2.6. Synchronizing the VITC to System Time Immediately



This menu item allows the user to synchronize the VITC on the sync output to system time immediately. This synchronization will also happen once per day at the time specified using the *Set Jam Time* menu item. **Caution: This menu item is a live control**.

To synchronize the VITC on the sync output to system time immediately, select the *Jam Output* menu item and press the **SELECT** button. The left LCD screen will display *TIME JAMMED* in yellow for 2 seconds.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will disabled for other formats (shown in dark text).

When the time reference is set to VITC or LTC and the frame rate of the time reference is the same as the sync output, the time will be jammed directly from the time reference rather than from system time.

5.4.1.2.7. Synchronizing all the VITC, LTC, and Burn-In Clocks to System Time Immediately

OUTPUT
SYNC <1,6>
Jam all VITC
Jam Output

This menu item allows the user to synchronize both LTC outputs and all the VITC output times to system time immediately. **Caution: This menu item is a live control.**

To synchronize all the LTC and VITC times immediately, select the *Jam all VITC* menu item and press the **SELECT** button. The left LCD panel will display *ALL TIMES JAMMED* in yellow for 2 seconds.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will be disabled for other formats (shown in dark text).

5.4.1.2.8. Setting the VITC Frame Offset

OUTPUT
Sync <1,6>
Time offset
New Value: 0 frames
Set Value: 0 frames

This menu item allows the user to set an offset between the system time and the VITC time. This feature is commonly used to compensate for video path delays common within a television facility. The offset value will be added along with the time zone offset and Daylight Saving Time correction to obtain the final VITC time. To advance the VITC earlier than the system time, set the offset to a negative (-) value.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will be disabled for other formats (shown in dark text).

5.4.1.2.9. Selecting the VITC Time Zone Offset

OUTPUT
Sync <1,6>
Time zone
-12:00 hours
to
+12:00 hours

This menu item allows the user to set a time zone offset between the system time and the VITC time on the sync output. The time zone offset value is set in 30-minute increments. The system time should be running at UTC. This time zone offset will be added to the system time along with the Daylight Saving Time correction and the VITC frame offset to obtain the final VITC time.

Use the ↑ and ↓ buttons or turn the control knob to move the cursor to select the desired time zone offset. Press the **SELECT** button to choose the indicated value. It will then become highlighted to show it is the active value.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will be disabled for other formats (shown in dark text).

5.4.1.2.10. Enabling Daylight Saving Time for the VITC on the Sync Output

OUTPUT
Sync <1,6>
DST Ctl
Off
On
On Legacy Aux

This menu item allows the user to control whether Daylight Saving Time (DST) compensation will be applied to the VITC time on the sync output.
When set to *Off*, Daylight Saving Time compensation will not be applied to the VITC time on the sync output.

When set to *On* the rules set by the *DST rules* menu in the *GENERAL root* menu will be used to adjust the VITC time.

This menu item is only applicable when the Sync *Mode* is set to the *PAL-B* or *NTSC-M* formats and will be disabled for other formats (shown in dark text).

5.4.1.2.11. Enabling Insertion of the Ten Field Reference

OUTPUT
Sync <1,6>
Ten field Ctl
Off
On

This menu item controls insertion of a SMPTE ST 318 compatible ten field pulse sequence on line 15 of NTSC-M black burst formats. This pulse sequence is commonly used to synchronize the AES audio sample distribution over ten fields of NTSC video.

When set to *Off*, the ten field pulse sequence is not inserted.
When set to *On,* a ten field pulse sequence will be inserted onto line 15 of the NTSC-M black burst format.

This menu item is only applicable to the NTSC-M format and will be disabled for all other formats (shown in dark text).

5.4.1.3. Setting the Phase of the Sync Outputs

The phase of the sync outputs is set independently of each other. There are four menu items that are used to set the phase. Figure 5-2 and Figure 5-3 show the default video sync alignment (V phase = 1, H phase = 1, fine phase = 0.0%) for 59.94Hz and 50Hz systems respectively.

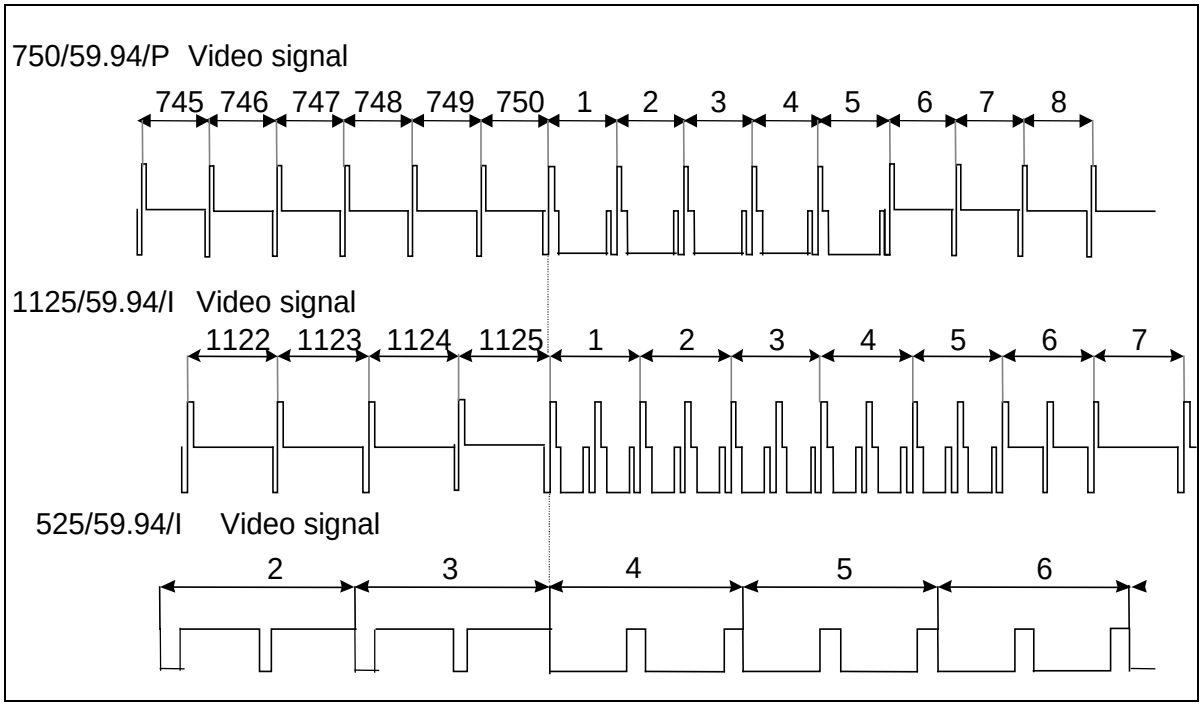


Figure 5-2: Video Sync Phase Alignment in 59.94Hz Field Rate Systems

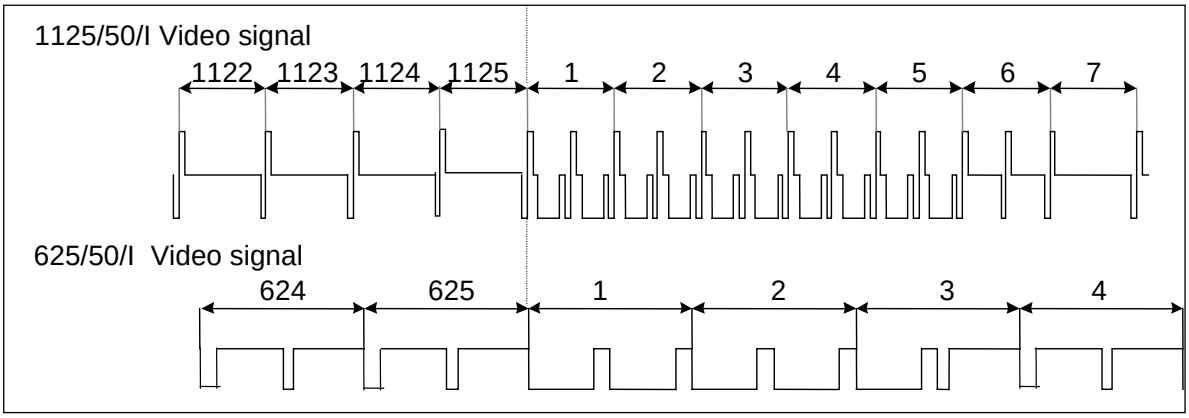
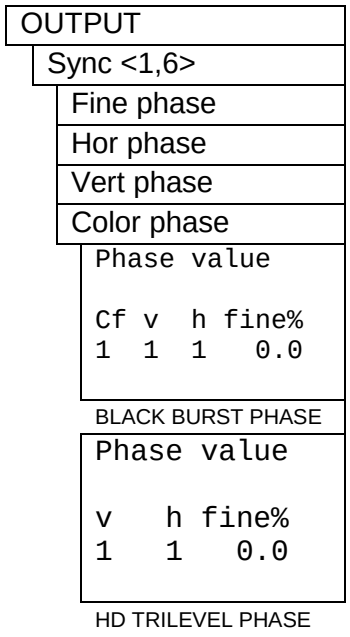


Figure 5-3: Video Sync Phase Alignment in 50Hz Field Rate Systems

The front panel display will show `LIVE CONTROL` on the left LCD screen in green to indicate that adjusting the sync output phase menu items will affect the phasing of the respective sync output immediately. You do not have to press the SELECT button to accept the new values. Use these controls with caution, as they will affect the overall timing of devices connected to the sync outputs.



There are four menu items that are used to adjust the phase of the sync output. Only the black burst (NTSC-M and PAL-B) and HD tri-level output modes can be phased. The pulse and subcarrier sync formats will always remain in phase with the frequency reference. The wordclock phase is controlled in the AES Audio menu.

When any of the four phase adjustments is selected, the right LCD panel will display a phase control screen that can be used to view all four adjustments simultaneously. The active adjustment will be highlighted and the other adjustments will be shown in dark text. For HD tri-level and Slo-PAL bi-level sync modes the color frame adjustment will not be shown. Turn the control knob or press the ↑ and ↓ buttons to adjust the phase value.

Tip: Pressing in the control knob while turning will make adjustments in steps of 16 allowing large adjustments to be done quickly.

The phase adjustments are wrapping. This means that when the smaller phase control is adjusted beyond its maximum, it will wrap back to 0 and the next larger phase control will automatically be incremented by one. Similarly, when the smaller phase control is adjusted below 0, it will wrap to its maximum value and the next larger phase control will be decremented by one. This can be used to make very gradual phase adjustments by continually adjusting the fine phase control until the horizontal and vertical phases reach their desired values (may take a long time).

Caution: These menu items are live controls. Changing their values will immediately affect the sync output and all downstream devices.

Note: Increasing a phase value (↑) **delays** the respective output. Decreasing a phase value (↓) **advances** the respective output.

The *Fine phase* menu item is used to adjust the phase of the sync output in fractions of a sample. 100.0% is equivalent to one sample period.

The *Hor phase* menu item is used to adjust the phase of the sync output in steps of samples.

The *Vert phase* menu item is used to adjust the phase of the sync output in steps of lines.

The *Color phase* menu item is the largest phase control that is used to adjust the sync output in steps of whole frames. It is normally used to align the color frame sequence for the black burst outputs. It is only available for the NTSC-M and PAL-B sync modes and will be disabled (shown in dark text) for HD tri-level and Slo-PAL bi-level modes.

5.5. GENERAL CONFIGURATION ITEMS

Menu description to be included in upcoming manual revision.

5.6. SNMP REMOTE CONTROL WITH VISTALINK

Menu description to be included in upcoming manual revision.

6. UPGRADING THE FIRMWARE

6.1.1. Uploading the Firmware

More information will be included in upcoming manual revision. Contact Evertz customer service at +1 905-335-7570 or service@evertz.com for more information.

6.1.2. Uploading the Firmware using FTP over Ethernet.

More information will be included in upcoming manual revision. Contact Evertz customer service at +1 905-335-7570 or service@evertz.com for more information.

6.2. SERVICING INSTRUCTIONS AND TROUBLESHOOTING

CAUTION: These servicing instructions are for use by qualified service personnel only. To reduce risk of electric shock, do not perform any servicing instructions in this section of the manual unless you are qualified to do so.

CAUTION: If the unit is fitted with dual power supplies, make sure that power is removed from both supplies before performing any work on the unit. There is no power switch so the power cords must be unplugged.

6.2.1. Changing the Fuses

CAUTION: For continued protection against the risk of fire, replace only with the same type and rating of fuse.

ATTENTION: Pour éviter les risques d'incendie, remplacer le fusible avec un fusible de même calibre.

Each power supply module contains a fuse. The fan module does not have a fuse. Remove the front panel to gain access to the mounting screw on the front of the power supply module. Unscrew the Phillips screw and remove the module by pulling on the handle. The fuse is located at the rear of the supply behind the rear connector and fan. Pull out the blown fuse being careful not to bend or damage the diode and place a fuse of the correct value in its place. Use a slow-blow (time delay) 5x20mm fuse rated for 250 Volts with a current rating of 1 Amp. Carefully reinsert the module, checking to make sure the diode doesn't impact the chassis. Secure the power supply module using the Philips mounting screw and replace the front panel.

6.2.2. Replacing the Battery

The 5700MSC-IP is fitted with a 3V 20mm diameter Lithium battery type CR2032. This battery is used to power the clock while power is removed from the unit. If the unit is not keeping time properly when it

is powered down, the battery should be replaced according to the procedure outlined in section 6.2.2.1.

Before attempting to change the battery remove power from the 5700MSC-IP.

CAUTION Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type.

6.2.2.1. Safety Guidelines and Precautions Concerning the Use of 3V Lithium Batteries

Please observe the following warnings strictly. If misused, the batteries may explode or leak, causing injury or damage to the equipment.

- The batteries must be inserted into the equipment with the correct polarity (+ and -).
- Do not attempt to revive used batteries by heating, charging or other means.
- Do not dispose of batteries in fire. Do not dismantle batteries.
- Do not short circuit batteries.
- Do not expose batteries to high temperatures, moisture or direct sunlight.
- Do not place batteries on a conductive surface (anti-static work mat, packaging bag or form trays) as it can cause the battery to short.

6.2.2.2. Procedure for Replacing the Battery

- Remove the front panel
- Eject the main board by unlatching the ejectors on each side and pulling outwards
- The battery is located on the left side of the main board behind the metal shield
- Carefully lift out the old battery
- Insert the new battery with the + side facing up. Make sure it is firmly inserted into the socket
- Reinsert the board by carefully lining it up on the card guides and push until both ejectors latch
- Reinstall the front panel back onto the unit