Tables

REVISION HISTORY

REVISION	DESCRIPTION	DATE
1.0	Original Version	Mar 00
1.1	Table 1 updated, Section 5.2 added	Apr 00
1.2	Table 2 updated to add new signals and genlock phasing Genlock Phase adjustments added	Jun 00
1.2.1	Minor Typographical fixes	Feb 01
1.3	Table 2 updated to add new signals supported in software version 2.2 build 22	May 01
1.3.1	Notice re unsupported signals in Table 2	Jan 02
1.4	Table 2 updated to add new signals supported in software version 3.0 build 1	Feb 02
1.4.1	Table 2 updated to add new signals supported in software version 3.0 build 2	May 02
1.4.2	Table 2 updated to signal 29supported in software version 3.0 build 2 Minor typographical and formatting changes	Dec 02

This page left intentionally blank

1. OVERVIEW

The 7750SRG-HD generates various analog bi-level and tri-level sync signals for both HD and SD applications. The 7750SRG-HD provides an analog genlock input that allows you to synchronize the sync signals to your plant horizontal and vertical timing.

The 7750SRG-HD generates all analog sync signals defined by SMPTE 274M (1080i/p) and 296M (720p) as well as those required for NTSC, PAL and slow PAL (625i/48) applications. The four independent sync outputs can be configured to output different sync signals. The common combinations of HDTV and SD analog sync outputs can be selected via card edge control.

In conjunction with the 7700ADA-HD Analog Distribution Amplifier and the 7750TG-HD HDTV Test Signal Generator, this module will fulfill all of your slave sync generation requirements. (PKG7752RGTS-HD system brochure for details on our HDTV Reference Generator Test Set System applications)

Features:
- NTSC or PAL colour black gen lock or free-runs with no gen lock reference
- Phase adjustment of outputs with respect to gen lock input
- Selectable frame rate divisor of 1 or 1/1.001
- Wide variety of 1080I, 1035I, 1080p, 720p, NTSC, PAL and slow PAL sync output sync signals
- HSDL tri level sync for 2K data transfers
- 4 separate analog sync signal outputs
- 8 position DIP switch selects combinations of sync signals available
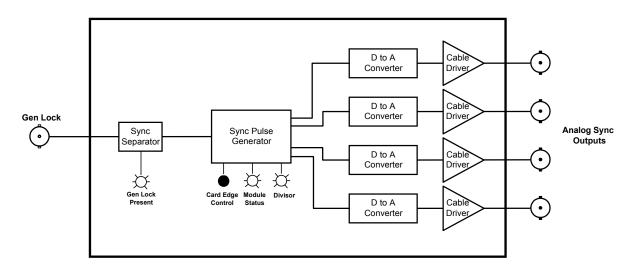- Front panel LEDs indicate gen lock presence, module fault

Figure 1: 7750SRG-HD Block Diagram

2. INSTALLATION

The 7750SRG-HD module comes with a companion rear plate that has 5 BNC connectors. For information on mounting the rear plate and inserting the module into the frame see the 7700FR chapter section 3.

Figure 2: 7750SRG-HD Rear Panel

GEN LOCK   Input BNC connector for analog Gen Lock reference. The genlock signal may be an NTSC or PAL colour black video or 0.3 V bi-level sync. Table 2 gives a list of the valid reference signal types for the output signal combination you have selected, and whether the outputs will be phase locked or clock locked to the genlock reference. DIP switches 6 and 7 select whether the outputs will be genlocked, and whether the default phasing or user set phasing will be used. Jumper J2 on the 7700REF submodule selects whether the reference input is terminated or high impedance. (See section 6.3)

SYNC OUTPUT   There are four BNC connectors with various combinations of analog sync outputs. The output signals available are selected using DIP switches 1 to 5 (See Table 2)

3.   SPECIFICATIONS

3.1.   GEN LOCK INPUT

Type: Depends on output video format (see Table 2)
                            NTSC or PAL Colour Black 1 V p-p
                            Composite Bi-level sync (525i/59.94 or 625i/50) 300 mV
Connector: 1 BNC per IEC 169-8
Termination: 75 ohm (jumper selectable)

3.2.   ANALOG SYNC OUTPUTS

Number of Outputs: 4.
Standard: SMPTE 274M, 296M, HSDL, NTSC, PAL, 6Hz TTL Pulse
                          - Selectable as per Table 2
Connectors: 4 BNC per IEC 169-8
Signal Level: HD Sync outputs: 600 mV nominal tri-level
                          SD Sync outputs: 300 mv nominal bi-level
                          6 Hz output: TTL

3.3.   ELECTRICAL

Voltage: + 12VDC
Power: 6 Watts.
EMI/RFI: Complies with FCC Part 15, class A and EU EMC directive.

4.   STATUS LEDS

4.1.   MODULE STATUS LEDS

The location of the status LEDs is shown in Figure 5.

MODULE OK   This Green LED will be On when the module is operating properly.

LOCAL FAULT   This Red LED will blink on and off if the microprocessor is not running. The LED will
                          be on solid when there is a fault in the module power supply**.**

SIGNAL PRESENT: This Green LED will be On when there is a valid genlock signal present at the
                          module genlock input.

> **This LED does not necessarily indicate that the genlock signal is the correct frame rate for the selected sync output format. For example, if a 59.94 Hz signal is required for the selected output video format, but a 50 Hz signal is present at the genlock input, the SIGNAL PRESENT LED will be On. In this case the output video will NOT be properly referenced but will constantly try to re-sync to the genlock frame reference.**

DIVISOR: This Green LED will be On when the Slave Reference generator is operating with the 1/1.001 Divisor enabled. This mode is selected when DIP switch 1 in On.

5. CARD EDGE CONTROLS

The 7750SRG-HD is equipped with an 8 position DIP switch to allow the user to select various output signals available formats. It is also used to select the genlock reference type and phase alignment, and whether the system rate divisor is 1 or 1/1.001. The On position is down, or closest to the printed circuit board. Table 1 gives an overview of the DIP switch functions.

DIP Switch	Function
1	1/1001 Divisor Enable
2	
3	Output Signal Selection
4	
5	
6	Genlock/ Free Run Selection
7	Genlock phasing
8	Reserved

Table 1: DIP Switch Functions

A three position, return to center toggle switch is used in conjunction with a momentary pushbutton to adjust the phase of the outputs with respect to the genlock reference.

5.1. SELECTING THE OUTPUT SYNC SIGNALS

DIP switches 1 to 5 are used to select the combination of sync output signals present on the four BNC outputs of the 7750SRG-HD. The On position is down, or closest to the printed circuit board. Table 2 shows the settings of the DIP switches for selecting the video output formats, and the types of genlock signals that can be used with each.

Outputs 1 and Output 2 usually contain tri-level sync pulses for the various high definition formats. Outputs 3 and 4 contain either bi-level standard definition sync pulses or a 6Hz or 1 Hz sequence pulse. The sequence pulses are one field (of the higher frame rate) in duration and occur when line 1 of output 1 and line 1 of output 2 coincide.

		DIP Switch				Output				Genlock		
#	1	2	3	4	5	1	2	3	4	Type	Lock	Phased Outputs
1	Off	Off	Off	Off	Off	1080i/60	1080p/24sF	625i/48	6Hz Pulse	NTSC	Clock	---
2	On	Off	Off	Off	Off	1080i/59.94	1080p/23.98sF	625i/47.96	6Hz Pulse	NTSC	Phase	1
3	Off	On	Off	Off	Off	1080i/50	1080p/24sF	625i/48	1Hz Pulse	PAL	Phase	1
4	On	On	Off	Off	Off	Reserved	Reserved	Reserved	Reserved	---	---	---
5	Off	Off	On	Off	Off	1080p/30	1080p/24sF	625i/48	6Hz Pulse	NTSC	Clock	---
6	On	Off	On	Off	Off	1080p/29.97	1080p/23.98sF	625i/47.96	6Hz Pulse	NTSC	Phase	1
7	Off	On	On	Off	Off	1080p/25	1080p/24sF	625i/48	1Hz Pulse	PAL	Phase	1
8	On	On	On	Off	Off	Reserved	Reserved	Reserved	Reserved	---	---	---
9	Off	Off	Off	On	Off	1080p/24	1080p/24sF	625i/48	625i/48	NTSC	Clock	---
10	On	Off	Off	On	Off	1080p/23.98	1080p/23.98sF	625i/47.96	625i/47.96	NTSC	Clock	---
11	Off	On	Off	On	Off	1080p/24sF	1080p/24sF	625i/48	625i/48	NTSC	Clock	---
12	On	On	Off	On	Off	1080p/23.98sF	1080p/23.98sF	625i/47.96	625i/47.96	NTSC	Clock	---
13	Off	Off	On	On	Off	720p/60	720p/24	625i/48	6Hz Pulse	NTSC	Clock	---
14	On	Off	On	On	Off	720p/59.94	720p/23.98	625i/47.96	6Hz Pulse	NTSC	Phase	1
15	Off	On	On	On	Off	1035i/60	1080p/24sF	625i/48	6Hz Pulse	NTSC	Clock	---
16	On	On	On	On	Off	1035i/59.94	1080p/23.98sF	625i/47.96	6Hz Pulse	NTSC	Phase	1
17	Off	Off	Off	Off	On	1080i/60	720p/60	525i/59.94	525i/59.94	NTSC	Clock	---
18	On	Off	Off	Off	On	1080i/59.94	720p/59.94	525i/59.94	525i/59.94	NTSC	Phase	1,2,3,4
19	Off	On	Off	Off	On	60 V drive	1080p/24sF	625i/48	6 Hz Pulse	NTSC	Clock	---
20	On	On	Off	Off	On	59.94 V drive	1080p/23.98sF	625i/47.96	6 Hz Pulse	NTSC	Phase	1
21	Off	Off	On	Off	On	1080p/24	1080p/24sF	625i/48	625i/48	PAL	Phase	1
22	On	Off	On	Off	On	1080i/59.94	1080p/23.98sF	625i/50	625i/50	NTSC	Clock	
23	Off	On	On	Off	On	1080i/50	1080p/24sF	525i/59.94	525i/59.94	PAL	Clock	
24	On	On	On	Off	On	Reserved	Reserved	Reserved	Reserved	---	---	---
25	Off	Off	Off	On	On	1980i/30	1650i/38.30	625i/50	625i/50	PAL	Clock	
26	On	Off	Off	On	On	1980i/29.97	1650i/38.26	525i/59.94	525i/59.94	NTSC	Clock	
27	Off	On	Off	On	On	1080i/59.94	1080p/23.98sF	525i/59.94	6 Hz Pulse	NTSC	Phase	1
28	On	On	Off	On	On	1080i/59.94	1080p/23.98sF	525i/47.69	6 Hz Pulse	NTSC	Phase	1
29	Off	Off	On	On	ON	1080p/25	1080i/50	625i/50	625i/50	PAL	Phase	1,2,3,4

(rows 13, 14 marked with * ; rows 25, 26 marked with ‡)

Table 2: Sync Output Selection Switch Settings

*Note 1: sync output selections 13 an 14 in table 2 are not implemented at this time.
‡Note 2: sync outputs for High Speed Dual Link 2K Data Transfers

5.2.   SELECTING THE GEN LOCK REFERENCE

The 7750SRG-HD will free run on its internal crystal oscillator or be referenced to a genlock signal applied to the GEN LOCK input. The genlock signal is a standard definition colour black video or 0.3 V bi-level sync. DIP switch 6 selects if the 7750SRG-HD will free run or be referenced to the genlock Reference video as shown in Table 3.

DIP 6	FUNCTION	DESCRIPTION
Off	Free Run (default)	The 7750SRG-HD will free run on its internal crystal oscillator.
On	Gen Lock	The 7750SRG-HD sync outputs will be phase locked, or clock locked to a Standard Definition colour black video or bi-level sync signal as shown in Table 2.

Table 3: Gen Lock Reference Switch Settings

5.3. SELECTING FACTORY PRESET OR USER ADJUSTABLE TIMING OF THE OUTPUTS WITH RESPECT TO THE GEN LOCK INPUT

DIP switch 7 selects if the 7750SRG-HD will use the factory default phasing of its outputs to the reference genlock, or the user defined phase adjustments. Phasing of the outputs is only possible when the genlock lock is of the *phase* type as shown in Table 2. In most cases only the phase of output 1 is adjustable and the phase of the remainder of the outputs is locked to the phase of output 1. In the case where multiple outputs can be phased (as shown in Table 2) then the phase of each output can be adjusted independently. Figure 4 shows the default phase alignment of Output 1 to the genlock reference.

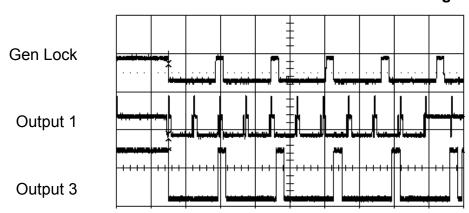| DIP 7	FUNCTION	DESCRIPTION
Off	Factory Phase (default)	The phase of the outputs is determined by factory settings when a genlock phase lock is possible (see Table 2)
On	User Preset Phase	The phase of the outputs is determined by user settings when a genlock phase lock is possible (see Table 2).

Table 4: Gen Lock Reference Switch Settings

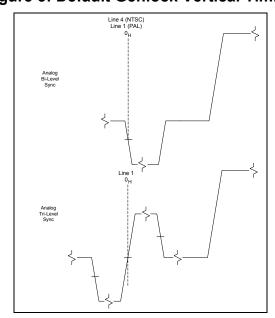**Figure 3: Default Genlock Vertical Timing**

Figure 4: Default Genlock Horizontal Timing

5.3.1. Adjusting the Timing of the Output Video with Respect to the Gen Lock Input

The toggle switch and push button are used to set the timing of the output signals to the Gen Lock Reference. Individual V and H phase adjustments allow you to control the timing of the outputs with respect to the beginning of the Gen Lock reference frame. (0_H time of line 1 field 1 for PAL references or 0_H time of line 4 field 1 for NTSC References). The 0_H time of line 1 of output 1 is aligned to this point when the factory default phasing is used.

The V phase adjust provides a coarse adjustment of timing and sets the line number of the output video that will be aligned with beginning of the reference frame. The H phase adjust provides a fine adjust of timing and sets the pixel number of the line on the output video set by the V parameter that will be aligned with the beginning of the reference frame. If adjustments to the H parameter cause it roll through the pixel number at the start of a new line (the EAV) then the V parameter will change to the next higher or lower line. The factory default is to align the EAV of Line 1 of the output video with the beginning of the reference frame.

The three position, return to center toggle switch is used in conjunction with a momentary pushbutton to adjust the phase of the outputs with respect to the genlock reference. Four LEDs located on the lower end of the module (opposite the DIP switch) are used to indicate when the module is in phase adjust mode. The Output 1 Phase adjust LED is located closest to the center of the module. The LED will be On or flashing, indicating that you are adjusting the V or H phase of the specific output respectively.

To enter the phase adjust mode, press the pushbutton. The Output 1 Phase adjust Led will come on solid, indicating that the toggle switch can be used to adjust the V phase of output 1. Pressing the toggle switch up will advance the phase and pressing the toggle switch down will delay the phase. Press the pushbutton again to adjust the horizontal phase of output 1. The Output 1 Phase adjust Led will come on flashing, indicating that the toggle switch can be used to adjust the H phase of output 1. Pressing the toggle switch up will advance the phase and pressing the toggle switch down will delay the phase. Press the pushbutton again to adjust the phase of the next output, or to exit phase adjust mode if only one output can be phase adjusted.
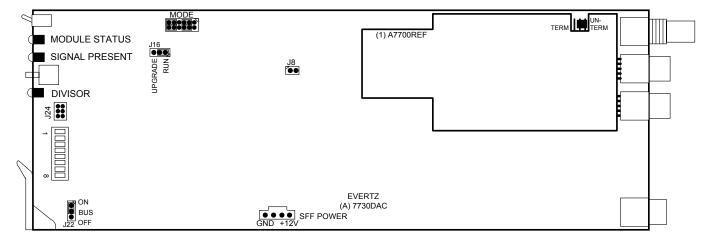
6. JUMPERS

Figure 5 : Location of Jumpers

6.1. SELECTING WHETHER LOCAL FAULTS WILL BE MONITORED BY THE GLOBAL FRAME STATUS

BUS   The BUS jumper J22 located at the front of the module determines whether local faults (as shown by the Local Fault indicator) will be connected to the 7700FR frame's global status bus.

To monitor faults on this module with the frame status indicators (on the PS FRAME STATUS LED's and on the Frame's Fault Tally output) install this jumper in the On position. (Default)

When this jumper is installed in the Off position, local faults on this module will not be monitored.

6.2. CONFIGURING THE MODULE FOR FIRMWARE UPGRADES

UPGRADE   The UPGRADE jumper J16 located at near the top of the module near the MODE jumper block, is used when firmware upgrades are being done to the module. For normal operation it should be installed in the *RUN* position. See the *Upgrading Firmware* section of this manual for more information.

To upgrade the firmware in the module unit pull it out of the frame. Move Jumper J16 into the *UPGRADE* position. Install the Upgrade cable provided (located in the vinyl pouch in the front of this manual) onto header J24 at the card edge. Re-install the module into the frame. Run the upgrade as described in the *Upgrading Firmware* section of this manual. Once the upgrade is completed, remove the module from the frame, move J16 into the *RUN* position, remove the upgrade cable and re-install the module. The module is now ready for normal operation.

6.3. SELECTING WHETHER THE GENLOCK REFERENCE INPUT IS TERMINATED

TERM/UNTERM   The TERM/UNTERM jumper J2 located on the A7700REF gen lock sub-module is used to terminate the gen lock input. Then it is in the TERM position a 75 ohm terminating resistor will be connect the input to ground. When it is in the UNTERM position the gen lock input will be high impedance.