Model 8950 Digital VITC Reader

Instruction Manual

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INFORMATION TO USERS IN EUROPE

NOTE

CISPR 22 CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to the European Union EMC directive. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

INFORMATION TO USERS IN THE U.S.A.

NOTE

FCC CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

WARNING

Changes or Modifications not expressly approved by Evertz Microsystems Ltd. could void the user's authority to operate the equipment.

Use of unshielded plugs or cables may cause radiation interference. Properly shielded interface cables with the shield connected to the chassis ground of the device must be used.

REVISION HISTORY

REVISION	DESCRIPTION	DATE
1.0	Original issue	January 96
1.1	Added Chapter 5, Technical Description	October 96
	Updated Chapter 2, Installation	November 96
	Updated Chapter 5	May 97

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1. OVERVIEW

The 8950 is a multi-purpose Digital VITC Reader that extracts the vertical interval timecode directly from the digital bitstream. The model 8950 VITC reader's line range can be easily programmed from the front panel, thus permitting recovery of specific VITC data where multiple sets have been recorded.

Features:

- Standard unit is equipped for component digital video.
- Serial digital video input provides automatic cable equalization on cable lengths up to 200 meters of low loss coax such as Belden 8281
- Serial digital video output provides two separate outputs
- Passes embedded audio and other ancillary data signals
- Rack mountable
- 8 or 10 bit resolution
- 12 digit Alpha-numeric display, with 10 pushbuttons
- Serial Remote Control for connection to a computer - Broadcasts reader data or sends it on request.

1.1. HOW TO USE THIS MANUAL

This manual is organized into 5 chapters: Overview, Installation, Operation, Serial Remote Control Protocol and Technical Description.

Items of special note are indicated with a double box like this.

1.2. DEFINITIONS

AES: (Audio Engineering Society): A professional organization that recommends standards for the audio industries.

AES/EBU: Informal name for a digital audio standard established jointly by the Audio Engineering Society and the European Broadcasting Union organizations.

ANALOG: An adjective describing any signal that varies continuously as opposed to a digital signal that contains discrete levels representing digits 0 and 1.

A-TO D CONVERTER (ANALOG-TO-DIGITAL): A circuit that uses digital sampling to convert an analog signal into a digital representation of that signal.

BIT: A binary representation of 0 or 1. One of the quantized levels of a pixel.

BIT PARALLEL: Byte-wise transmission of digital video down a multi-conductor cable where each pair of wires carries a single bit. This standard is covered under SMPTE 125M, EBU 3267-E and CCIR 656.

BIT SERIAL: Bit-wise transmission of digital video down a single conductor such as coaxial cable. May also be sent through fiber optics. This standard is covered under SMPTE 259M and CCIR 656.

BIT STREAM: A continuous series of bits transmitted on a line.

BNC: Abbreviation of "baby N connector". A cable connector used extensively in television systems.

BYTE: A complete set of quantized levels containing all the bits. Bytes consisting of 8 to 10 bits per sample are typical in digital video systems.

CABLE EQUALIZATION: The process of altering the frequency response of a video amplifier to compensate for high frequency losses in coaxial cable.

CCIR (International Radio Consultative Committee) An international standards committee. (This organization is now known as ITU.)

CCIR-601: (This document now known as ITU-R601). An international standard for component digital television from which was derived SMPTE 125M and EBU 3246-E standards. CCIR-601 defines the sampling systems, matrix values and filter characteristics for both Y, B-Y, R-Y and RGB component digital television signals.

CCIR-656(This document now known as ITU-R656).The physical parallel and serial interconnect scheme for CCIR-601. CCIR-656 defines the parallel connector pinouts as well as the blanking, sync and multiplexing schemes used in both parallel and serial interfaces. It reflects definitions found in EBU Tech 3267 (for 625 line systems) and SMPTE 125M (parallel 525 line systems) and SMPTE 259M (serial 525 line systems).

CLIFF EFFECT (also referred to as the ‘digital cliff’) This is a phenomenon found in digital video systems that describes the sudden deterioration of picture quality when doe to excessive bit errors, often caused by excessive cable lengths. The digital signal will be perfect even though one of its signal parameters is approaching or passing the specified limits. At a given moment

however, the parameter will reach a point where the data ca no longer be interpreted correctly, and the picture will be totally unrecognizable.

COMPONENT ANALOG: The non-encoded output of a camera, video tape recorder, etc., consisting of the three primary colour signals: red, green, and blue (RGB) that together convey all necessary picture information. In some component video formats these three components have been translated into a luminance signal and two colour difference signals, for example Y, B-Y, R-Y.

COMPONENT DIGITAL: A digital representation of a component analog signal set, most often Y, B-Y, R-Y. The encoding parameters are specified by CCIR-601. The parallel interface is specified by CCIR-656 and SMPTE 125M.

COMPOSITE ANALOG: An encoded video signal such as NTSC or PAL video, that includes horizontal and vertical synchronizing information.

COMPOSITE DIGITAL: A digitally encoded video signal, such as NTSC or PAL video, that includes horizontal and vertical synchronizing information.

D1: A component digital video recording format that uses data conforming to the CCIR-601 standard. Records on 19 mm magnetic tape. (Often used incorrectly to refer to component digital video.)

D2: A composite digital video recording format that uses data conforming to SMPTE 244M. Records on 19 mm magnetic tape. (Often used incorrectly to refer to composite digital video.)

D3: A composite digital video recording format that uses data conforming to SMPTE 244M. Records on 1/2" magnetic tape.

EBU (European Broadcasting Union): An organization of European broadcasters that among other activities provides technical recommendations for the 625/50 line television systems.

EBU TECH 3267-E: The EBU recommendation for the parallel interface of 625 line digital video signal. This is a revision of the earlier EBU Tech 3246-E standard which was in turn derived from CCIR-601.

EDH Error Detection and Handling (EDH) is defined in SMPTE RP-165 as a method of determining when bit errors have occurred along the digital video path. According to RP-165, two error detection checkwords are used, one for active picture

samples, and the other on a full field of samples. Three sets of flags are used to convey information regarding detected errors, to facilitate identification of faulty equipment or cabling. One set of flags is associated with each checkword, and the third is used to evaluate ancillary data integrity. The checkwords and flags are combined into a special error detection data packet which is included as ancillary data in the serial digital signal.

EMBEDDED AUDIO: Digital audio is multiplexed onto a serial digital video data stream.

ITU: The United Nations regulatory body governing all forms of communications. ITU-R (previously CCIR) regulates the radio frequency spectrum, while ITU-T (previously CCITT) deals with the telecommunications standards.

ITU-R601: See CCIR601

PIXEL: The smallest distinguishable and resolvable area in a video image. A single point on the screen. In digital video, a single sample of the picture. Derived from the words *picture element*.

RESOLUTION: The number of bits (four, eight, ten, etc.) determines the resolution of the signal. Eight bits is the minimum resolution for broadcast television signals.

4 bits = a resolution of 1 in 16.
8 bits = a resolution of 1 in 256.
10 bits = a resolution of 1 in 1024.

SERIAL DIGITAL: Digital information that is transmitted in serial form. Often used informally to refer to serial digital television signals.

SMPTE (Society of Motion Picture and Television Engineers): A professional organization that recommends standards for the film and television industries.

SMPTE 125M: The SMPTE standard for bit parallel digital interface for component video signals. SMPTE 125M defines the parameters required to generate and distribute component video signals on a parallel interface.

SMPTE 244M: The SMPTE standard for bit parallel digital interface for composite video signals. SMPTE 244M defines the parameters required to generate and distribute composite video signals on a parallel interface.

SMPTE 259M: The SMPTE standard for 525 line serial digital component and composite interfaces.

TRS: Timing reference signals used in composite digital systems. (It is four words long).

TRS-ID: Abbreviation for "Timing Reference Signal Identification". A reference signal used to maintain timing in composite digital systems. (It is four words long.)

4:2:2 A commonly used term for a component digital video format. The details of the format are specified in the CCIR-601 standard. The numerals 4:2:2 denote the ratio of the sampling frequencies of the luminance channel to the two colour difference channels. For every four luminance samples, there are two samples of each colour difference channel.

4Fsc Four times subcarrier sampling rate uses in composite digital systems. In NTSC this is 14.3 MHz. In PAL this is 17.7 MHz.

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2. INSTALLATION

2.1. REAR PANEL

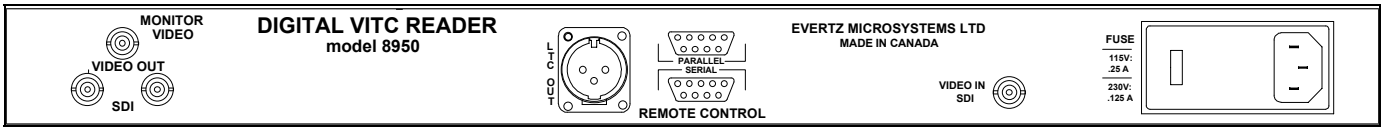

Figure 2-1: 8950 Rear Panel

The following sections describe the purpose of the rear panel connectors of the 8950. Sections 2.1.1 to 2.1.3 describe the specific signals that should be connected to the 8950.

2.1.1. Digital Video Connections

VIDEO IN SDI: A BNC connector for input of 10 bit serial digital video signals compatible with the SMPTE 259M standard.

VIDEO OUT SDI: Two BNC connectors for output of 10 bit serial digital video signals compatible with the SMPTE 259M standard. This video will be the video input with characters inserted onto it.

2.1.2. Linear Time Code Connections

LTC OUT: A male XLR connector for output of SMPTE / EBU linear timecode from the VITC to LTC translator.

2.1.3. Analog Monitor Connections (8950-MON option)

The analog composite monitor output is optional and may not be fitted on your unit.

MONITOR VIDEO: A BNC output of the optional composite analog encoder.

2.1.4. Remote Control Connections

SERIAL: A 9 pin female 'D' connector for RS232/422 communications to a computer

Pin	Description
1	Ground
2	RS-422 Transmit A(-)
3	RS-422 Receive B(+)
4	Receive Common
5	RS-232 Transmit
6	Transmit Common
7	RS-422 Transmit b(+)
8	RS-232 Receive and RS-422 Receive A(-)
9	Ground

PARALLEL: A 9 pin female 'D' connector for connection to 'closure to ground' remote control signals for the character inserter. Each input has an internal 47 K ohm pull-up to +5 volts.

Pin	Description
1	Ground
2	n/c
3	n/c
4	Time VCG Window On/Off
5	UB VCG Window On/Off
6	VCG Keyer On/Off
7	Front Panel Time/UB Display
8	not used
9	Ground

2.1.5. Power Connections

LINE: The 8950 may be set for either 115v/60 Hz or 230v/50 Hz AC operation. The voltage selector switch is accessible on the rear panel. The line voltage connector contains an integral slow blow fuse (and a spare one).

2.2. MOUNTING

The 8950 Digital VITC Reader is equipped with rack mounting angles and fits into a standard 19 inch by 1 3/4 inch (483 mm x 45 mm) rack space. The mounting angles may be removed if rack mounting is not desired.

2.3. POWER REQUIREMENTS

2.3.1. Selecting the Correct Mains Voltage

Power requirements are 115 or 230 volts AC at 50 or 60 Hz, switch selectable on the rear panel. Power should be applied by connecting a 3 wire grounding type power supply cord to the power entry module on the

rear panel. The power cord should be minimum 18 AWG wire size, type SST marked VW-1, maximum 2.5 m in length.

Before connecting the line power, be sure to select the proper line voltage. Also, check that the line fuse is rated for the correct value marked on the rear panel.

The power entry module combines a standard IEC 320 power inlet connector, voltage selector switch, two 5 x 20 mm fuse holders (one active, one spare) and an EMI line filter.

To change the mains voltage setting, open the cover of the power entry module using a small screwdriver. Remove the drum selector switch, and re-insert it so that the desired voltage is visible through the opening on the mains connector cover. Check that the correct fuse is in use as shown in section below.

2.3.2. Changing the Fuse

The fuse holder is located inside the power entry module. To change the fuse, open the cover of the power entry module using a small screwdriver. The fuse holder on the bottom contains the active fuse. The one at the top contains a spare fuse. Pull the bottom fuse holder out and place a fuse of the correct value in it. Use slo blo (time delay) 5 x 20 mm fuses rated for 250 Volts with the following current ratings:

For 115 Volt operation	250 mA
For 230 Volt operation	125 mA

Make sure that the arrow is pointing down when you replace the fuse holder. Close the door on the power entry module and connect the mains voltage.

Never replace with a fuse of greater value.

2.4. CONNECTING THE DIGITAL VIDEO

2.4.1. Video Input

The 8950 requires that a digital video source be connected to the VIDEO IN SDI video input. The 8950 may be configured to accept either 525 or 625 line digital video in the component (4:2:2) format or 525 line digital

video in the composite (4Fsc) format. The VIDEO TYPE parameter on the front panel menu must be set correctly to match the video input. See section 3.3.1 for information on changing the video type setting.

The 4:2:2 and 4 Fsc LED's indicate which input is active. The VIDEO LED indicates that there is video present. When it is blinking it indicates that there is no video present.

2.4.2. Video Output

The VIDEO OUT SDI outputs contain the input video with VITC (with timecode, source ID and VTR status encoded), and character data keyed in by the keyer. Connect one of these outputs to any input on your system that accepts 8 or 10 bit SERIAL digital video. Two identical VIDEO OUT SDI digital video outputs are provided.

2.5. LINEAR TIME CODE TRANSLATOR OUT

The 8950 provides a fully decoded and regenerated play speed LTC output containing the time and user bits of the VITC Reader. The output is available on an XLR connector at the rear panel. Output level is adjustable from approximately 0.5 V to 4 V using a trim pot inside the unit. The code output should be connected to the record input of the time code channel of your video recorder. Pin 1 of the XLR is ground. Pins 2 and 3 provide a balanced output.

2.6. TYPICAL APPLICATION

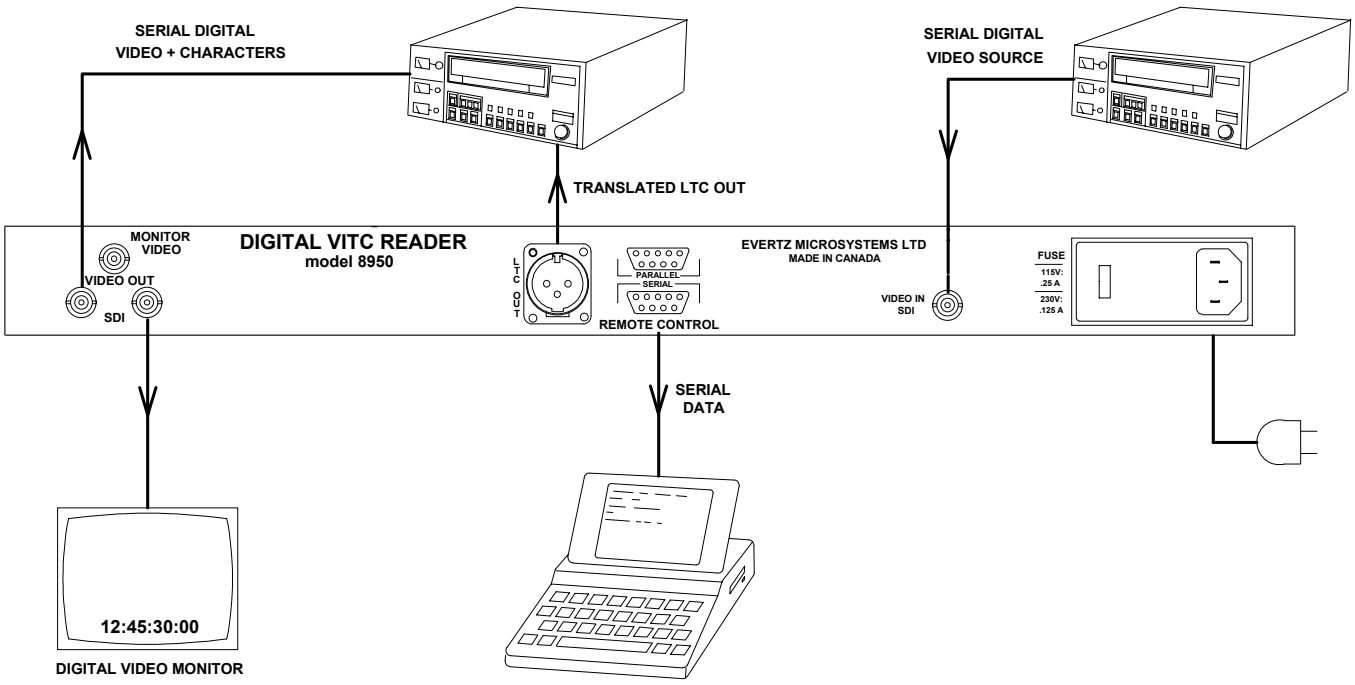

Figure 2-2: Typical Application of 8950 for Character Generation and Translation to LTC

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3. HOW TO OPERATE THE DIGITAL VITC READER

3.1. AN OVERVIEW OF KEY AND DISPLAY FUNCTIONS

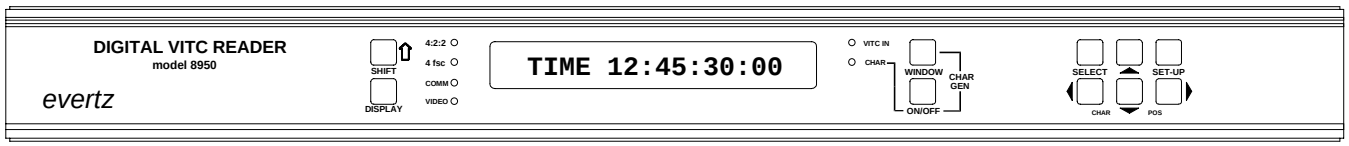


Figure 3-1: Front Panel Layout

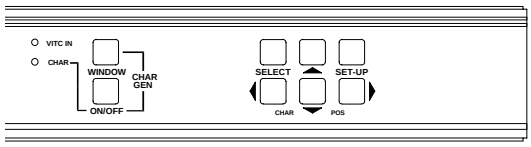
The display area consists of an 16 digit alphanumeric display, 6 LED status indicators and a 10 pushbutton keypad.

The keypad is used to control the front panel menu system, to position the character display windows, and to provide control of the front panel display. When the **SHIFT** key is held down, the meanings of some of the keys are modified, gaining quick access to a wider variety of functions. (Throughout this manual **SHIFT +** indicates that you should hold down the **SHIFT** key while pressing the second key.)

A front panel programming menu provides a quick and simple method of configuring the 8950 Digital VITC Reader for your application.

Section 3.3 gives detailed information on the specific operations required to control the 8950.

3.1.1. The Setup Push-button Group



The Setup key group consists of the **SELECT, SETUP** and ←, →, ↑, ↓ keys and is used to navigate the front panel programming menu system, to position character windows and to enter the source ID message.

SETUP Enters the Setup mode which is used to set up various modes of operation. Pressing SETUP again while in this mode exits the Setup mode. (See also section 3.3.)

SELECT When in the Setup mode the SELECT key is used to activate the current choice for the selected item**.**
When in the Source ID programming mode, the SELECT key is used to accept the Source ID message that has been entered.

↑ ↓ ← → When in the Setup mode, the ↑ & ↓ arrow keys are used to move up and down the main items in the menu system and the ← & → arrow keys are used to show the menu choices for the current item. (See also section 3.3.)

When in the VCG window select mode, the arrow keys are used to position the individual character windows on the screen. (See also section 3.5.1.)

When not in either the Setup mode or the VCG window select mode, the arrow keys are used to position all the character windows on the screen. (See also section 3.5.2.) SHIFT + arrow keys are used to provide fine adjustment of the character generator raster.

3.1.2. The Character Window-Button Group

CHAR GEN WINDOW Initiates VCG window select mode and highlights the selected window. Use the arrow keys to move the window, use the CHAR GEN ON/OFF key to turn the window on or off. Press the MODE key again to select the next VCG window. Press the MODE key a third time to return to the normal VCG display mode.

CHAR GEN ON/OFF Turns the character generator ON and OFF. When in the VCG window select mode the CHAR GEN ON/OFF key is used to turn individual windows ON and OFF.

3.1.3. The Display-Button

DISPLAY Selects what data is being displayed on the front panel. Each time it is pressed it cycles to the next display data. Currently there are two types of display data:

TIME 12:34:56:00	Time information
UB 12 34 56 78	User Bit information

3.1.4. An Overview of the SHIFT Key functions

When the **SHIFT** key is held down, the meanings of some of the keys are modified, gaining quick access to a wider variety of functions. Following is a summary of the shifted key functions

SHIFT+SETUP Enters the Engineering Setup menu system

SHIFT+SELECT Resets the 8950 to factory defaults when you are in the FACTORY RESET menu item of the Engineering Setup Menu.

SHIFT+WINDOW Displays the current settings of most of the Setup menu items.

SHIFT+↑ & SHIFT+ ↓ Fine adjustment of character vertical raster position

SHIFT+← & SHIFT+ → Fine adjustment of character horizontal raster position

3.1.5. An Overview of the Status Indicators

There are 6 status indicators located on the front panel that show operational status of the 8950 at a glance.

4:2:2 Indicates that 8950 is configured for component digital signals

4 fsc Indicates that 8950 is configured for NTSC composite digital signals.

COMM Indicates that the 8950 is communicating with an external computer device.

VIDEO Indicates that serial digital video is present. If it is blinking, it indicates a valid digital video signal is not present.

VITC IN Indicates that VITC data is being read.

CHAR Indicates that the character generator keyer is enabled. (future)

3.2. AN OVERVIEW OF THE FRONT PANEL PROGRAMMING MENU

The key to the operational flexibility of the 8950 Digital VITC Reader lies in the front panel programming menu system. The programming menu system uses the 12 digit alphanumeric display and provides a quick, intuitive method of configuring 8950 Digital VITC Reader, guiding you to the correct setup for your application. The six keys in the Setup key group (**SELECT**, **SETUP,** ← → ↑ ↓) are used to cycle through the various items on the programming menu.

The 8950 menu system consists of a main menu with two or more choices for each menu item. The sub menu items are shown in lower case to allow them to be easily distinguished from the main level items. Figure 3-2 is an overview of the front panel menu system, and shows all the menu items and where you will find the menu choices.

To enter the front panel programming menu, press the **SETUP** key.

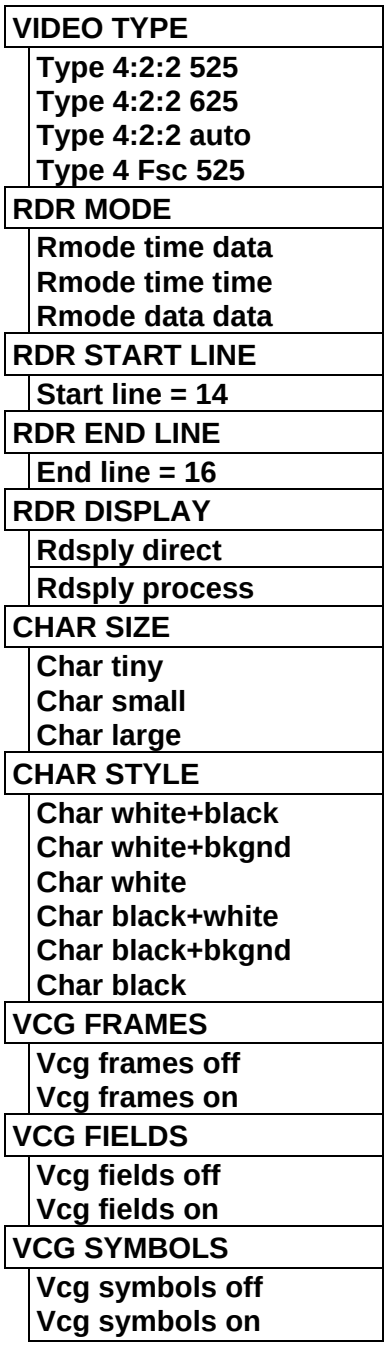


Figure 3-2: Overview of the 8950 Programming Menu System

The two vertical arrow keys (↑, ↓) allow you to move vertically within the menu tree. When you have selected the desired menu item, press the → key to reveal the choices for that item. The choice that is currently selected will be blinking. When you have selected the desired sub menu choice press the **SELECT** key to save your choice.

When you have made all the desired changes, press the **SETUP** key to return to the normal display mode.

To aid in finding the descriptions of the various menu items in sections 3.3 to 3.4, the drop down menu items and its sub menu items are shown in the margin of the manual, next to the description as shown.

Each of the menu items is described in section 3.3, with an explanation of what each choice does.

3.2.1. Engineering Setup Menu

The Engineering Setup menu allows the advanced user to change various internal parameters of the 8950, or to invoke several advanced modes.

This menu should be used by advanced users only, as improper use can overwrite user setups.

The 8950 Engineering Setup menu consists of a main menu with two or more choices for each menu item. The sub menu items are shown in lower case to allow them to be easily distinguished from the main level items. Figure 3-3 is an overview of the Engineering Setup menu, and shows all the menu items and where you will find the menu choices. To enter the Engineering Setup menu, press the **SHIFT+SETUP** keys. Each of the menu items is described in section 3.3, with an explanation of what each choice does.

SERIAL BAUD RATE
Baud rate 2400
Baud rate 9600
Baud rate 19200
Baud rate 38400
SERIAL FORMAT
Fixed to 8-N-1
SERIAL TEST
Serial test off
Serial test on
DISPLAY LEVEL
Display level 6
FACTORY RESET
Shift+sel=reset
SOFTWARE VERSION
DR89D8.M U960430

Figure 3-3 Overview of the 8950 Engineering Menu

3.3. PROGRAMMING THE 8950 OPERATIONAL MODES

The front panel menu is used to configure the basic operational modes of the 8950 Digital VITC Reader such as selecting which keyer is active, etc.

3.3.1. Selecting the Video Type

VIDEO TYPE
Type 4:2:2 525
Type 4:2:2 625
Type 4:2:2 auto
Type 4 Fsc 525

The **VIDEO TYPE** menu item is used to program the 8025 for the digital video format.

Select **422 525** for operation with component video with a line rate of 525 lines per field. Conforming to SMPTE 125M.

Select **422 625** for operation with component video with a line rate of 625 lines per field. Conforming to EBU Tech 3267-E (1992) or the 4:2:2 level of CCIR recommendation 601.

Select **422 auto** for operation with component video with a line rate of either 525 or 625 lines per field. The 8950 will auto detect the line rate and automatically reconfigure itself. Press SHIFT+WINDOW when you are not in the SETUP menus to display the standard that is currently active.

Select **4Fs 525** for operation with composite video formats conforming to the SMPTE 244M.

3.3.2. Selecting the Format of the Time and User Bit Data

RDR MODE
TIME DATA TIME TIME DATA DATA

The **READER MODE** menu item is used to select the type of information that is contained in the time and user bits of the reader.

Select **time data** when the time contains normal time information and the user bits contain numeric data.

Select **time time** when both the time and the user bits contain time information.

Select **data data** when both the time and the user bits contain numeric data.

3.3.3. Setting The VITC Reader Line Range

RDR START LINE
Start line = 10

The **RDR START LINE** and **RDR END LINE** menu items are used to select the lines which are enabled for VITC reading.

The **RDR Start line** menu items used to set the first line that VITC will be read from. To view the current setting press the ➔ key. The current line number will be blinking. To set a different line use the ← or ➔ keys. To accept the new value press the **SELECT** key.

RDR END LINE
End line = 20

The **RDR End Line** menu item is used to set the second line that VITC will be read from. To view the current setting press the ➔ key. The current line number will be blinking. To set a different line use the ← or ➔ keys. To accept the new value press the **SELECT** key.

RDR START LINE and RDR END LINE determine a range of lines that the 8950 will look for VITC on. It will attempt to read VITC from the lower number to the higher number.

3.3.4. Controlling the Reader 'Look ahead' Compensation

RDR DISPLAY
Rdsply process Rdsply direct

The **RDR DISPLAY** menu item is used to select whether the normal 'look ahead' compensation for reader dropouts is active or not. Normally, the data is read in one frame and displayed with an 'add 1 frame' compensation. This method helps to cover any minor reader disturbances. In some operational modes it is desirable to disable this feature and to display exactly what is being read. When reading VITC, it is possible to read and display the information in the same video field, thus maintaining field accuracy even in DIRECT mode. The topmost positions of the character generator are not available when in the direct mode.

Select **Rdsply process** to enable normal 'look ahead' compensation. Displays from VITC reader will be 'on time' but will **NOT** follow code discontinuities immediately.

Select **Rdsply direct** to enable DIRECT display mode. Data is displayed exactly as it is read without 'look ahead' compensation. Displays from the VITC reader will be 'on time' but cannot be positioned at the very top of the raster.

3.3.5. Selecting the Character Size

CHAR SIZE
Char tiny
Char small
Char large

The **CHAR SIZE** menu item is used to select one of three sizes for the character generator's display. The on screen format menus always use the small character size.

The **Char tiny** character size occupies 8 lines per field for each character row. This permits 28 vertical positions on the raster in NTSC.

The **Char small** character size occupies 16 lines per field for each character row. This permits 14 vertical positions on the raster in NTSC.

The **Char large** character size occupies 32 lines per field for each character row. This permits 7 vertical positions on the raster in NTSC.

3.3.6. Selecting the Character Style

CHAR STYLE
Char white
Char white+black
Char white+bkgnd
Char black
Char black+white
Char black+bkgnd

The **CHAR STYLE** menu item is used to select whether the background mask will be used and whether the characters will be white or black. The on screen format menus are always white characters keyed into a black background mask.

Select **Char white** to disable the background and key white characters directly into the picture.

Select **Char white + black** to key white characters on a black background mask into the picture.

Select **Char white + bkgnd** to key white characters on a transparent gray background mask into the picture.

Select **Char black** to disable the background and key black characters directly into the picture.

Select **Char black + white** to key black characters on a white background mask into the picture.

Select **Char black + bkgnd** to key black characters on a transparent white background mask into the picture.

3.3.7. Selecting whether the Frames, Fields and Symbols will be displayed on the VCG

VCG FRAMES
- **Vcg frames off**
- **Vcg frames on**

The **VCG FRAMES** menu item is used to select whether the frames will be shown when the time is displayed in the character inserter.

Select **Vcg frames off** to hide the timecode frames.

Select **Vcg frames on** to show the timecode frames.

VCG FIELDS
- **Vcg fields off**
- **Vcg field on**

The **VCG FIELDS** menu item is used to select whether the fields will be shown when the time is displayed in the character inserter.

Select **Vcg fields off** to hide the timecode fields.

Select **Vcg fields on** to show the timecode fields.

VCG SYMBOLS
- **Vcg symbols off**
- **Vcg symbols on**

The **VCG SYMBOLS** menu item is used to select whether the **T** and **U** symbols will be shown in front of the time and user bit displays of the VCG.

Select **Vcg symbols off** to hide the symbols.

Select **Vcg symbols on** to show the symbols.

3.4. PROGRAMMING THE ENGINEERING SETUP FUNCTIONS

The Engineering Setup Menu is used to set the serial port baud parameters, front panel display brightness, reset the 8950 to factory defaults, etc.. The Engineering Setup menu items are normally required only during installation. See section 3.2.1 for information on using the Engineering Setup menu system.

3.4.1. Selecting the Serial Port Baud Rate

SERIAL BAUD RATE
- **Baud rate 2400**
- **Baud rate 9600**
- **Baud rate 19200**
- **Baud rate 38400**

The **SERIAL BAUD RATE** menu item is used to set the baud rate of the remote control serial port. The 8950 supports four different baud rates from 2400 to 38400 baud. Select the highest baud rate that you computer can use for best results.

3.4.2. Selecting the Serial Port Data Format

SERIAL FORMAT
- **Fixed to 8-N-1**

The **SERIAL FORMAT** menu item is used to set the word length, parity and number of stop bits of the remote control serial port. The 8950 currently supports only 8 bits, no parity, 1 stop bit.

3.4.3. Testing the Serial Port

SERIAL TEST
Serial test off Serial test on

The **SERIAL TEST** menu item is used to turn on a serial port test message. Then the serial test is on, the 8950 outputs a message similar to:

```
EVERTZ DTCR  8950  SOFTWARE VERSION DR89D8.M U960430
```

3.4.4. Adjusting the Front Panel Display Brightness

DISPLAY LEVEL
Display Level = 2

The **DISPLAY LEVEL** menu item is used to adjust brightness of the front panel display. Use the ← and →keys to adjust.

3.4.5. Resetting the 8950 to Factory Defaults

FACTORY RESET
Sh+sel = reset

The **FACTORY RESET** menu item is used to return the 8950 to its factory defaults. When you press the ← or → keys, the display shows **Sh+sel = reset**. When you press **SHIFT + SELECT** the 8950 will reload its factory defaults and show the message

```
Reset done
```

3.4.6. Displaying the 8950 Software version

SOFTWARE VERSION
DR89D8.M U960430

The **SOFTWARE VERSION** menu item is used to display the 8950's software version. When you press the ← or → keys, the display shows the software version which will be something like:

```
DR89D8.M U960430
```

3.5. CHARACTER GENERATOR FUNCTIONS

Two separately positionable character windows displaying time or (user bits are available. The four arrow keys (↑, ↓, ←, →) control the position of all the windows . The **CHAR GEN ON/OFF** key selects whether the video character generator (VCG) keyer is on or off. The use of these keys in combination with the **CHAR GEN WINDOW** key selects which windows are displayed and their position on the screen. The CHAR SIZE item of the Setup menu is used to select character size.

3.5.1. Selecting and Positioning the Individual Character Inserter Windows

Press **CHAR GEN WINDOW** to enable the window select mode. All the character windows will appear on the screen with the window for the Time highlighted. Use the arrow keys (↑, ↓, ←, →) to position the Time window on the screen. Use the **CHAR GEN ON/OFF** key to turn the Time window on or off. Press the **CHAR GEN WINDOW** key to highlight the User Bits window. Use the **CHAR GEN ON/OFF** key to turn the User Bits window on or off and the arrow keys to move it to the desired location. Press the

CHAR GEN WINDOW key to highlight the Status window. Use the **CHAR GEN ON/OFF** key to turn the Status window on or off and the arrow keys to move it to the desired location. Press the **CHAR GEN WINDOW** key to return to normal display mode.

For example, to move only the Time window down, leaving the User Bits window in the same place, press **CHAR GEN WINDOW** and press the 🡻 key. Press the **CHAR GEN WINDOW** key two times to return to the normal display mode.

3.5.2. Positioning the Overall Character Display

In the normal VCG display mode, when none of the windows are highlighted, the arrow keys (🡹, 🡻, 🡸, 🡺) move all the displayed windows by the same relative amount. For example, to move the time and source ID/status windows both down by one line, press the 🡻 key.

3.5.3. Making Fine Adjustments To The Character Generator Raster Position

In the normal VCG display mode, when none of the windows are highlighted, holding down the shift key while pressing the arrow keys (🡹, 🡻, 🡸, 🡺) move the complete character raster in fine increments on the picture. The range of fine adjustment is limited when the character windows are positioned near the edges of the screen.

3.5.4. Character Generator On/ Off Controls

There are two factors that control whether the character generator will be turned on or off. In order of priority these are:

1. The **CHAR GEN ON/OFF** key on the front panel alternately turns the characters on and off. The VCG keyer On/Off remote control input can be used to perform this function remotely.

2 The individual windows can be turned off using the **CHAR GEN ON/OFF** key in window select mode. The Time On/Off and User Bits On/Off remote control inputs can be used to perform this function remotely.

3.5.5. Special VCG Indicators

The following special indicators are used between the seconds and frames digits of the time window in the character inserter to identify non drop frame and drop frame code (NTSC only)

Non Drop Frame Colon (:)
Drop Frame (NTSC) Period (.)

3.6. PARALLEL REMOTE CONTROL FUNCTIONS

A 9 pin D connector located on the rear panel labelled REMOTE CTL provides 6 parallel control inputs for remote control of some of the model 8950 functions. The pinout of the D connector is as follows:

Pin		Description
1		Frame Ground
	6	VCG Keyer On/Off
2		n/c
	7	Front Panel Time/UB Display
3		n/c
	8	not used
4		Time VCG Window On/Off
	9	Ground
5		UB VCG Window On/Off

TIME VCG WINDOW ON/OFF Provides an alternate method of turning the Time VCG window On and Off. The Time window is turned On by a high to low transition on this input, and turned Off by a low to high transition.

USER BIT VCG WINDOW ON/OFF Provides an alternate method of turning the User Bit VCG window On and Off. The User Bit window is turned On by a high to low transition on this input, and turned Off by a low to high transition.

VCG KEYER ON/OFF Provides an alternate method of turning the character inserter keyer On and Off. The character inserter is turned On by a high to low transition on this input, and turned Off by a low to high transition.

FRONT PANEL TIME/UB DISPLAY Provides an alternate method of selecting whether Time or User Bit data will be displayed on the front panel. Time is displayed by a high to low transition on this input, and User Bits is displayed by a low to high transition.

4. SERIAL REMOTE CONTROL PROTOCOL

4.1. OVERVIEW

- Four wire communications channel utilized - RS-422 levels. Alternate 2 wire interface using RS-232C levels
- Data transmitted asynchronously, bit serial, word serial with data exchange between the devices being digital.
- Transmission rate is selectable 38.4 K, 19.2K, 9600 Baud supported
- Data words utilized by the interface shall be as follows:

1 START bit + 8 DATA bits +1 PARITY bit + 1 STOP bit.
The parity bit shall denote EVEN parity

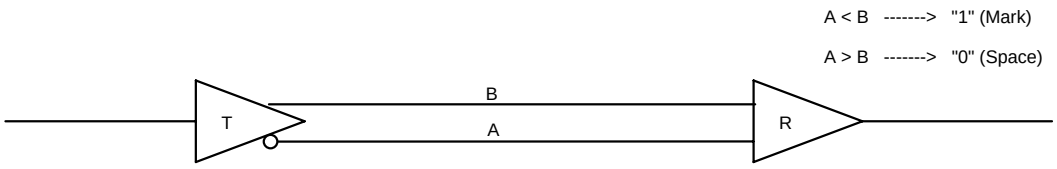
4.1.1. Connector Pin Assignment

Interface Connector: 9 pin D-subminiature female (DB-9S)

The pin assignment for the serial port shall be as follows:

Pin	Function
1	Frame Ground
2	Transmit A (-)
3	Receive B (+)
4	Receive Common
5	RS-232 Transmit (Optional)
6	Transmit Common
7	Transmit B (+)
8	Receive A (-)
9	Frame Ground

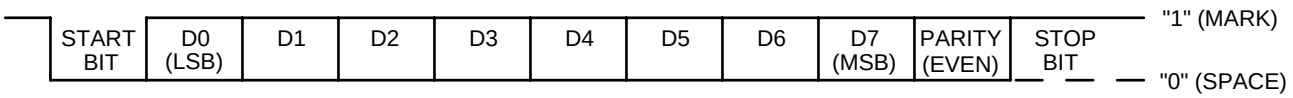
A and B are defined as follows:



4.1.2. Data Format

The serial port provides drivers which allow communications in either RS-232C or RS-422 electrical standards. The composition of the bit serial data format is as follows:

1 START + 8 DATA + 1 PARITY + 1 STOP



One of four baud rates is selected using the Engineering SETUP menu. When using the RS-422 standard the preferred baud rate is 38.4 KBaud. When using the RS-232 standard the preferred baud rate is 19.2ÜKBaud.

4.2. COMMUNICATIONS PROTOCOL

The Controller shall be denoted as the normal sender of a command (usually a computer). The Device shall be denoted as the normal sender of a Response (the Evertz unit).

All command values, arguments and data values shown in this document are expressed in hexadecimal format unless otherwise noted.

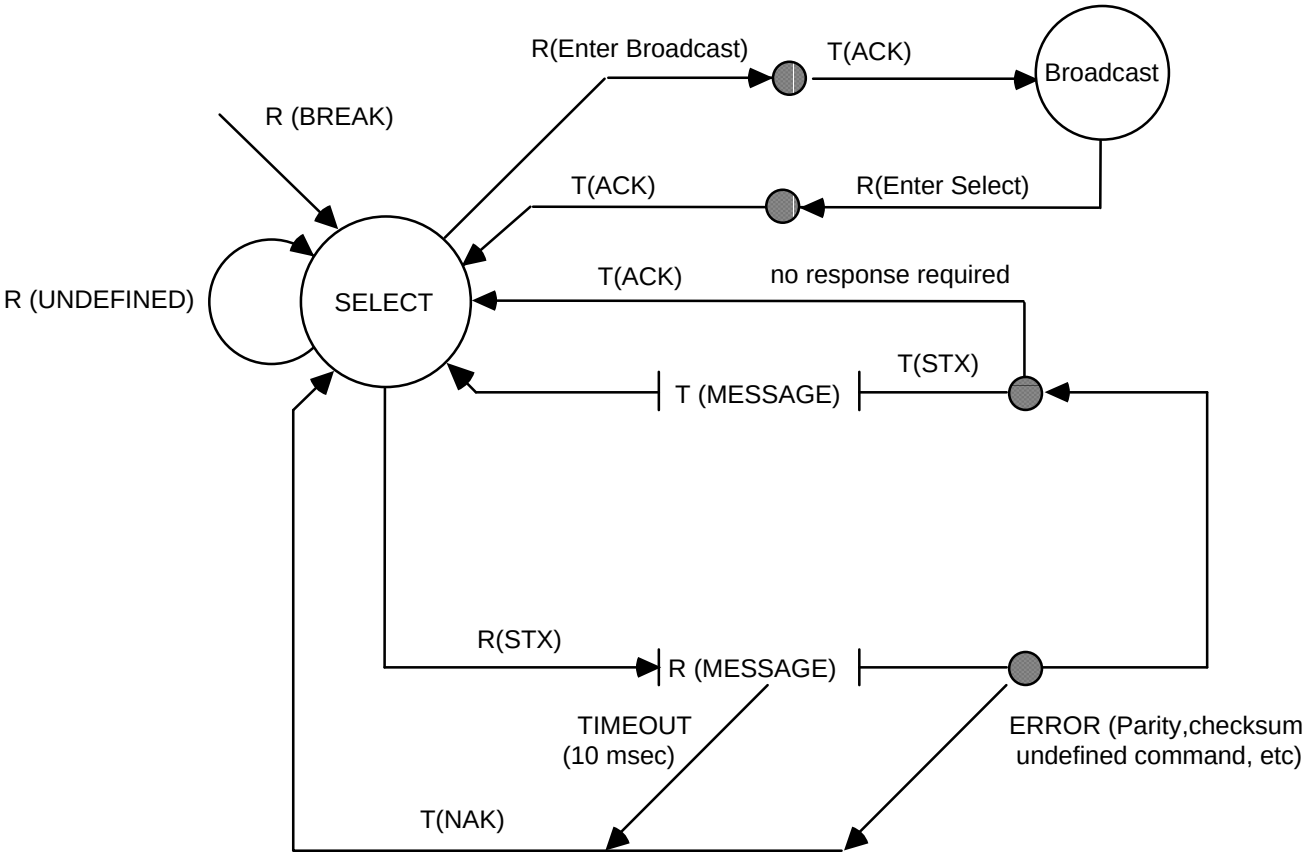


Figure 4-1: Communications Protocol State Diagram

The communications protocol is described in Figure 4-1. The Evertz unit (Device) immediately enters the select state upon power-up and remains there unless directed by an Enter Broadcast Cmd (02 hex)

to the broadcast communications state. The diagram shows the various states of the device. The designation R( ) indicates the data received from the controller, while the designation T( ) indicates the data transmitted by the Device.

4.3. MESSAGE BLOCK FORMAT

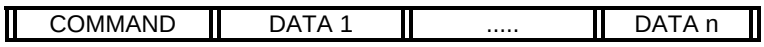
Once communications have been established command messages may be sent to the Device.

Each control message starts with the STX character and ends with a checksum. The message blocks are structured as follows:

STX	start of message character (02 hex)
BYTE COUNT	count of command message not including the STX, BYTE COUNT or CHECKSUM.
MESSAGE	variable length command message.
CHECKSUM	the two's complement of the one byte sum of the MESSAGE and the BYTE COUNT.

The purpose of the checksum is to verify that all the bytes in the message that contain variable data have been received properly. The STX is the only byte that has a fixed value, so it is the only byte not included in the checksum calculation. The checksum is calculated by adding all the variable bytes together. The least significant byte of this sum is then subtracted from 100 hex to compute the checksum. To verify that the checksum is computed correctly, add all the bytes including the checksum but excluding the STX together. The least significant byte of the sum should be zero if the checksum is computed correctly.

The MESSAGE consists of a command and optional bytes of data and is structured as follows:



COMMAND	single byte command directed to device.
DATA 1...DATA n	variable length, any arguments required by COMMAND.

If the command message was not accepted by the Device due to a checksum error, parity error or an invalid command the Device will respond with an **NAK** (05 hex) character and re-enter the SELECT state.

If the command message is accepted by the Device and there is no data response required, it will respond with an **ACK** (04 hex) character and re-enter the SELECT state.

If the command message requires a data response, the Device will transmit a response message structured as follows:

STX	start of message character (02 hex)
BYTE COUNT	count of response message not including STX, BYTE COUNT or CHECKSUM.
COMMAND ECHO	Command message echoed

MESSAGE — variable length response message consisting of the data requested by the command message.

CHECKSUM — The two's complement of the one byte sum of the COMMAND ECHO, MESSAGE and the BYTE COUNT.

For example, to request the current time code data in BCD format from the reader, the command message would be transmitted as follows:

02	02	66	01	97
STX	BYTE COUNT	SENSE RDR	BLOCKS	CHECKSUM

If the current LTC reader time code was 12:45:30:00 Drop Frame the response message would be received as follows:

02	07	66	01	00	30	45	12	01	0A
STX	BYTE COUNT	CMD (SENSE RDR)	CMD DATA (BLOCKS)	DATA 1 (FRMS)	DATA 2 (SECS)	DATA 3 (MINS)	DATA 4 (HRS)	DATA 5 (FLAGS)	CHKSUM

4.4. COMMANDS

Command from Controlling Device	**Return to Controlling Device**

CMD	DATA BYTES	DESCRIPTION	CMD ECHO BYTES	DATA BYTES	NAME
00		Sense Current Mode	1	1	Current Mode
01		Enter Select Mode			ACK
02		Enter Broadcast Mode			ACK
0B	1	Select Video Standard			ACK
11	1	PROM Version request	2	20	PROM Name & Version
1B		Sense Video Standard	1	1	Video Standard

Table 4-1: Systems Commands and their Valid Responses

Command from Controlling Device			Return to Controlling Device		
CMD	**DATA BYTES**	**DESCRIPTION**	**CMD ECHO BYTES**	**DATA BYTES**	**NAME**
20	1	Select Char Gen Size			ACK
21	3	Preset Char Gen Window Pos'n			ACK
22	2	Select Char Gen Window On/Off			ACK
23	1	Select Char Gen Global On/Off			ACK
24	1	Select Char Gen Style			ACK
25	1	Select Char Gen Frames			ACK
26	1	Select Char Gen Fields			ACK
27	1	Select Char Gen Symbols			ACK
28	2	Preset Char Gen Raster Pos'n			ACK
30		Sense Char Gen Size	1	1	Char Size
31	1	Sense Char Gen Window Pos'n	2	3	Char Gen Window Pos'n & Len
32	1	Sense Char Gen Window On/Off	2	1	Char Gen Window On/Off
33		Sense Char Gen Global On/Off	1	1	Char Gen Global On/Off
34		Sense Char Gen Style	1	1	Char Gen Style
35		Sense Char Gen Frames	1	1	Char Gen Frames
36		Sense Char Gen Fields	1	1	Char Gen Fields
37		Sense Char Gen Symbols	1	1	Char Gen Symbols
38		Sense Char Gen Raster Pos'n	1	2	Char Gen Raster Pos'n

Table 4-2: Character Generator Commands and their Valid Responses

Command from Controlling Device			Return to Controlling Device		
CMD	**DATA BYTES**	**DESCRIPTION**	**CMD ECHO BYTES**	**DATA BYTES**	**NAME**
40	1	Select Reader Assignment			ACK
41	2	Select Reader Mode			ACK
42	3	Select VITC Reader Lines			ACK
44	2	Select Reader Display			ACK
45	1	Define Broadcast Mode			ACK
60		Sense Reader Assignment	1	1	Reader Assignment
61	1	Sense Reader Mode	2	1	Reader Mode
62	1	Sense VITC Reader Lines	2	2	VITC Reader Lines
64	1	Sense Reader Display	2	1	Reader Display
65		Sense Reader Broadcast Mode	1	1	Reader Broadcast Mode
66	1	Sense Reader	2	x	Reader Data
67		Sense Reader Broadcast Block	1	x	Reader Broadcast Block

Table 4-3: Reader Commands and their Valid Responses

4.5. DATA FORMATS

4.5.1. Time Format Block

10 Frm	1 Frm	10 Sec	1 Sec	10 Min	1 Min	10 Hr	1 Hr	Flags

The Flags byte is a bitmapped byte of the timecode flag bits as follows:

Bit 0	Drop Frame Flag	0 = Non Drop Frame, 1 = Drop Frame
Bit 1	Colour Frame Flag	0 = Non Colour Frame, 1 = Colour Frame
Bit 2	VITC Field Flag	0 = Field 1, 1 = Field 2
Bit 3	User Bit Group Flag 0	
Bit 4	User Bit Group Flag 1	
Bit 5	User Bit Group Flag 2	
Bit 6	LTC Flag	1 = LTC Active
Bit 7	VITC Flag	1 = VITC Active

The Binary group flag bits are defined as follows:

	Bin Grp Flag 2	Bin Grp Flag 1	Bin Grp Flag 0
Character set unspecified	0	0	0
Eight bit Alpha-numeric Character set	0	0	1
Unassigned	0	1	0
Unassigned	0	1	1
Unassigned	1	0	0
Page/Line (SMPTE 262M)	1	0	0
Unassigned	1	1	0
Unassigned	1	1	1

4.5.2. Data Format Block

UB grp 2	UB grp 1	UB grp 4	UB grp 3	UB grp 6	UB grp 5	UB grp 8	UB grp 7

4.6. COMMAND AND RESPONSE DESCRIPTIONS

4.6.1. System Commands

01 Enter Select Mode

02 Enter Broadcast Mode

11 Sense PROM Version 1 byte 00 = PROM version
01 = Flash PROM version

Returns the control byte from the command +16 bytes PROM name + 16 bytes PROM version

0B Select Video Standard 1 byte Presets the Video Standard that is being used
00 = 4:2:2 Auto
01 = 4:2:2 525

02 = 4:2:2 625
03 = 4 Fsc 525

1B Sense Video Standard Returns 2 bytes as described in the Select Video Standard Command.

4.7. VIDEO CHARACTER INSERTER COMMANDS

Several of the VCG commands need to specify which VCG window they apply to. The following table defines the VCG window numbers.

WINDOW NUMBER	DESCRIPTION
01	Reader 1 Time
02	Reader 1 User Bits

Table 4-4: VCG Window Numbers

30 Sense Char Gen Size Returns 1 byte as defined below.

20 Select Char Gen Size 1 byte Selects the size of the VCG Character Font
00 = Tiny
01 = Small
02 = Large

31 Sense Char Gen Window Position Window No Returns 3 bytes of window position as follows.

Vertical Position	Horizontal Position	Window Length

21 Preset Char Gen Window Position Window No +1 byte Vertical Position + 1 Byte Horizontal Position

Sets the starting position of a VCG window on the raster.

SIZE	VERT POSITION	HORIZ POSITION
Tiny	0 to 29 are valid for NTSC 0 to 29 are valid for PAL	0 to 32 depending on window length
Small	0 to 14 are valid for NTSC 0 to 16 are valid for PAL	0 to 32 depending on window length
Large	0 to 7 are valid for NTSC 0 to 8 are valid for PAL	0 to 32 depending on window length

Table 4-5: VCG Sizes

32 Sense Char Gen Window On/Off Window No Returns 1 byte as defined below.

22 Select Char Gen Window On/Off Window No + 1 byte

			Turns individual windows on and off. 00 = Off 01 = On
33	**Sense Char Gen Global On/Off**		Returns 1 byte as defined below.
23	**Select Char Gen Global On/Off**	1 byte	Turns all windows on and off. 00 = Off 01 = On
34	**Sense Char Gen Style**		Returns 1 byte as defined below.
24	**Select Char Gen Style**	1 byte	Selects the Style of the VCG windows. 00 = White 01 = White on Black 02 = Black 03 = Black on White 04 = White on Bkgnd 05 = Black on Bkgnd
35	**Sense Char Gen Frames**		Returns 1 byte as defined below.
25	**Select Char Gen Frames**	1 byte	Selects whether the frames digits will be shown on the character inserter. 00 = Blanked 01 = Displayed
36	**Sense Char Gen Fields**		Returns 1 byte as defined below.
26	**Select Char Gen Fields**	1 byte	Selects whether the fields digits (for VITC windows time windows only) will be shown on the character inserter 00 = Blanked 01 = Displayed
37	**Sense Char Gen Symbols**		Returns 1 byte as defined below.
27	**Select Char Gen Symbols**	1 byte	Selects whether the symbols which identify the Character inserter windows will be shown 00 = Blanked 01 = Displayed
38	**Sense Char Gen Raster Position**		Returns 2 bytes of raster position as follows.

Vertical Position	Horizontal Position

28	**Preset Char Gen Raster Position**	2 bytes	1 byte Vertical Position + 1 Byte Horizontal Position

Sets the starting position of a VCG raster with respect to the active picture area. For example to start the raster down 2 lines from the top of active picture set the vertical position to 2. To start the raster 5 pixels to the right of active picture set the horizontal position to 5.

4.8. READER COMMANDS

Several of the Reader commands need to specify which Reader they apply to. This parameter is called the Reader Number.

61	**Sense RDR Mode**	Rdr No	Returns 1 byte as defined below
41	**Select RDR Mode**	Rdr No + 1 byte	Selects the mode of the reader.

Reader modes set according to the following values

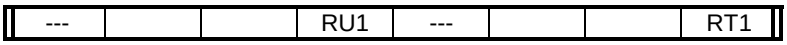
	DESCRIPTION	
MODE	**TIME**	**UB**
1	TIME	DATA
2	TIME	TIME
3	DATA	DATA

Table 4-6: Reader Modes

62	**Sense VITC RDR Lines**	Rdr No	Returns 2 byte as defined below
42	**Preset VITC RDR Lines**	Rdr No + 2 bytes	Selects the VITC lines of the reader.

The VITC reader will read starting at the first line number and ending at the second line numbers. Line numbers are packed BCD format. Valid lines at 6 to 21 for PAL and 10 to 20 for NTSC.

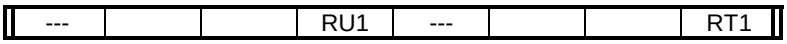
64	**Sense RDR Display**	Rdr No.	Returns 1 byte as defined below
44	**Select RDR Display**	Rdr No. + 1 byte	Selects the whether look ahead processing will be applied to the reader display. 00 = Processed 01 = Direct
65	**Sense Broadcast Mode**		Returns 1 byte as defined below
45	**Define Broadcast Mode**	1 byte	Defines a block of data which will be sent in broadcast mode, and in response to a Sense Broadcast Block command.



Each bit represents a variable length block of data which is requested. Time and User Bits are formatted according to the Select RDR Mode command above. The broadcast data blocks are assembled in the following order:

RT1 RU1

66 Sense Reader 1 byte Returns Reader data as defined by the following byte:



Each bit represents a variable length block of data which is requested. Time and data are formatted according to the Select RDR Mode command above. The bits are polled and return blocks are assembled in the following order:

RT1 RU1

67 Sense Broadcast Block Returns the broadcast block as defined by the Define Broadcast Mode command above.

5. TECHNICAL DESCRIPTION

5.1. OVERVIEW

The model 8950 Digital VITC Reader combines the latest LSI technology with sophisticated microcontroller firmware to provide a powerful, flexible reader system. The 8950 reads Vertical Interval Time Code directly from the digital video bitstream. It displays the data on the front panel and send it out the serial remote control port to a computer.

The front panel alphanumeric display is used to configure various items. The 8950's menu system consists of a main menu with two or more choices on each menu item.

5.2. JUMPERS AND SWITCHES

Component layout drawing 8025-81 shows the location and function of the switches and jumpers inside the model 8950. The jumper positions marked in **bold** face type are the default settings.

5.2.1. DIP Switch Functions

The main circuit board of the model 8950 contains an 8 position DIP switch which is used to invoke various diagnostic and calibration functions. The functions of each switch are described below.

Switch	Name	Normal	Function when Open	Function when Closed
1	Ser In	Closed		Serial Input Hardware Installed
2	Ser Out	Closed		Serial Output Hardware Installed
3	Mon	Open		Monitor Hardware Installed
4	Factory Reset	Open		Resets 8950 to factory defaults on power up
5	Not Used	Open		
6	Quick Boot	Open		Faster Boot up
7	Not used	Open		
8	Not used	Open		

Figure 5-1: DIP Switch Functions

5.2.2. Jumper Functions - Main Board

All jumpers are printed circuit board links and are installed in the default position. To change the position, the board link must be cut and a wire link must be installed in the desired location.

JP1	LCA Size	A	3042
		B	3064/3090
JP3	EPROM Size	**512**	Board link installed connects MCU EPROM U19 Address A15 to microprocessor A15 for use with 512K size EPROM.

		256	Board link installed connects MCU EPROM U19 Address A15 to +5 volts for use with 256K size EPROM.
JP4	EPROM CE	**Pin 2,3**	Board link installed connects Char EPROM CE to ground.
		Pins 1,2	Board link installed connects Char EPROM CE to +5 Volts after LCA loads.
JP5			Not installed for 8950
JP8	RS422	Pins 1,2	
	RS232	Pins 2,3	Default
JP10,11,12,13			Not installed for 8950

5.3. CIRCUIT DESCRIPTION

The model 8950 is a microcontroller based device functionally divided into the following hardware subsystems:

1 Microcontroller & I/O
2 Display and Pushbuttons
3 Serial Digital Video Input
4 Serial Digital Video Output
5 VITC Reader/Character Generator Logic
6 VITC Reader/Character Generator Keyer
7 LTC Translator
8 Analog Composite Monitor

The microcontroller, serial video inputs and outputs, and keyer LCA circuits are all contained on the main circuit card (8025). The display and keypad circuitry is contained on a separate circuit board (5220) which plugs into the main board via a twenty conductor ribbon cable. The analog composite monitor circuitry is contained on a separate circuit board (8026 or 8029) which plugs into the main board via two forty-four pin headers. The VITC Reader/Character generator logic circuitry is contained on a separate circuit board (8037) which plugs into the main board via a forty-pin header. The relevant schematic drawings are shown in brackets for each section of the circuit. The heart of the model 8950 circuitry is a programmable logic array (LCA) device (U17) which contains the keyer circuitry and the support circuitry for addressing various devices on the board.

5.3.1. Microcontroller (8025-36)

At the heart of the model 8950 reader is an 8032 microcontroller, (MCU) U19. Its three 8 bit bi-directional ports and 8 bit bus provide peripheral interfacing to the rest of the circuits. Program memory is contained on EPROM U21. Scratch pad and data RAM are provided internally by the MCU. An onboard oscillator, also part of the MCU, is crystal controlled. Its' 14.7456 MHz frequency is internally divided by 12, resulting in a processor operating frequency of 1.2288 MHz. Address decoder U23 provides decoded chip enables to each of the peripheral devices on the

board. Addressable latches U24 and U34 provide mode select control lines used throughout the board.

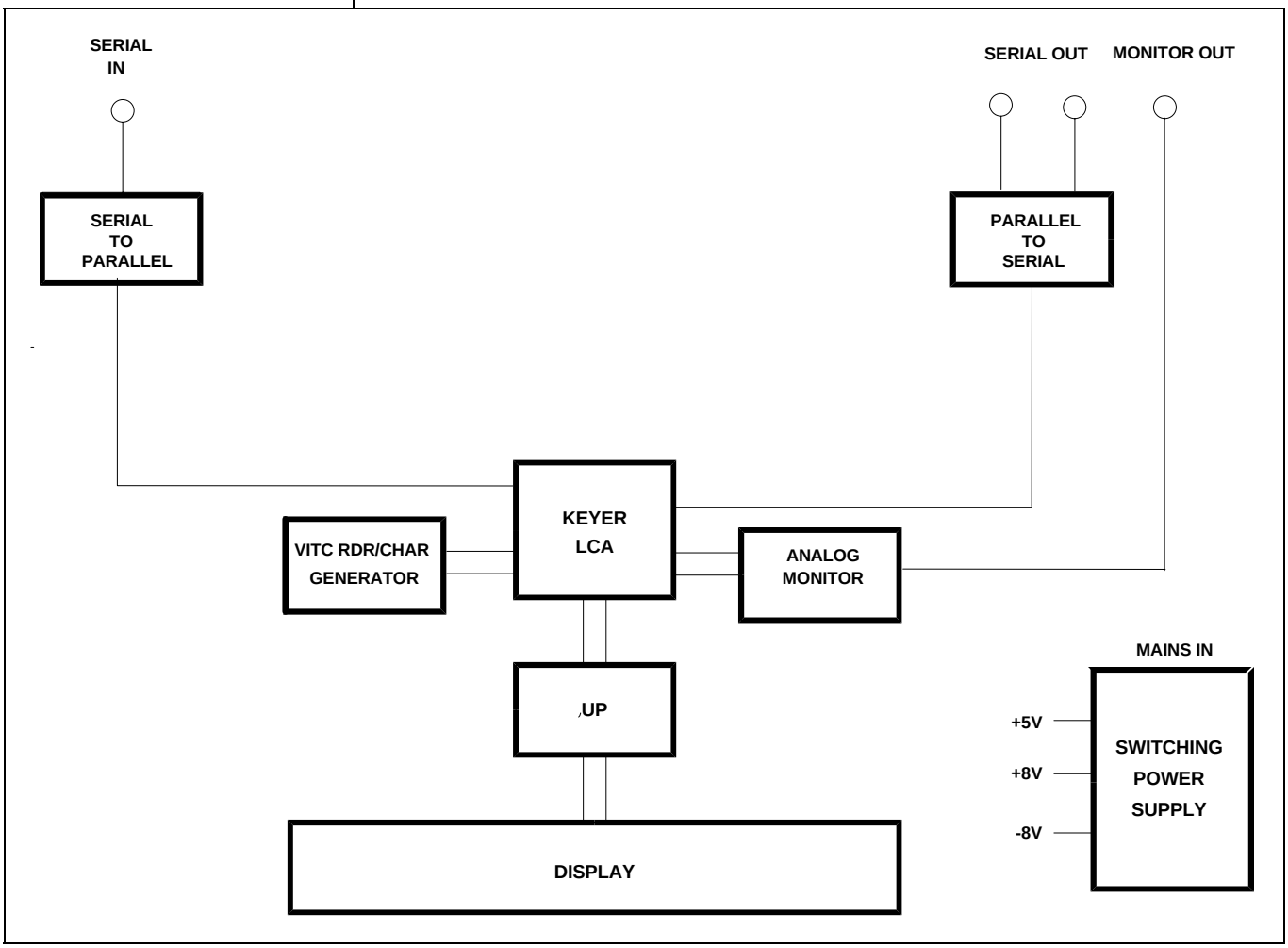


Figure 5-2: Block Diagram

5.3.2. Front Panel Display and Pushbuttons (5220-31)

A 12 digit alphanumeric display, and a 8 button keypad are contained on a separate circuit card (5220) which is connected to the main circuit board via a 20 conductor ribbon cable.

The 12 digit display is self scanning and contains its own character display memory. Data is written to the displays once per frame. Address Latch U1 generates chip enable and address information to the display devices to allow the MCU to write data to the display and control registers.
The status LED's are controlled by interface driver U3. This driver is accessed with a serial clock and data stream once per frame. When all the LED information has been shifted into the driver, it is latched there by the LEDSTB signal from the MCU (display header pin 10).

The 10 pushbuttons are arranged in a 8 x 2 matrix. Data from 8 keys at a time is latched into U2 by signal SH/LD on U2 pin 1. Address decoder U1

selects which set of 8 switches is latched into U2 using enable lines A0 and A1. Each time a key is pressed, the MCU firmware generates a key scan code corresponding to the position of the key in the key matrix.

To perform a Keyboard test and lamp test of the front panel LED's hold down the SETUP key on power up. The front panel display will show:

```
00    KEY
```

As you press various key combinations various of the LEDs will illuminate. The front panel display will show the Keyboard scan codes for each key combination pressed. Table 5-1 below shows the SCAN code for each key. To exit LED test mode, remove and re-apply power to the unit.

DISPLAY	01	SHIFT	41
VCG ON/OFF	02	VCG WINDOW	42
←	05	SELECT	45
↓	06	↑	46
→	07	SETUP	47

Table 5-1: Keyboard Scan Codes

5.3.3. Serial Digital Video Input (8025-33)

The serial digital input circuitry is based on the Gennum Genlinx Serial Digital Video chip set. The 9005 receiver/equalizer provides automatic cable equalization and clock extraction from the serial digital signal. It provides a balanced ECL level recovered clock and data signals to the 9000 decoder. The 9000 decoder de-serializes the signal and provides a parallel clock and 10 bits of parallel data input B of the input multiplexer U7, U8, and U9.

The 9005 receiver is capable of working with 143 MHz 4 Fsc composite NTSC, or 270 MHz 4:2:2 component video data rates. The capture frequency of the 9005 is set by trim pots VR2 for 270 MHz, and VR4 for 143 Mhz. The capture range can be adjusted with the following procedure.

1. Connect a digital volt meter set on a 10 volt range to the Loop filter test point LF (located at the rear left corner of the 8025 board).

2. Connect a serial digital video signal to the serial input of the 8950. Connect the serial output of the 8950 to a digital monitor, or connect the analog monitor output of the 8950 to an analog monitor.

4. Rotate trimpot VR2 for component video (VR4 for composite) fully clockwise. Slowly rotate the trimpot counter clockwise monitoring the loop filter voltage on the digital volt meter. Continue turning the trimpot until the picture appears. Note the voltage on the LF test point.

5. Continue rotating the trimpot until the loop filter voltage is 200 mVolts above the voltage measures in step 4.

5.3.4. Serial Digital Video Output (8025-34)

The serial digital output circuitry is based on the Gennum Genlinx chip set, and consists of the 9002 encoder and 9008 cable driver. The 9002 receives TTL level parallel data and clock signals from the keyer LCA and encodes the data into the SMPTE 259 specified bitstream. Cable driver 9008 receives the serial data from the 9002. The output of the 9008 is adjustable using trim pot VR7, and is nominally set to 800 mVolt p-p. Two identical serial outputs are provided.

5.3.5. VITC Reader/Character Generator Logic (8034-31, 8034-32, 8034-33) or (8037-31, 8037-32, 8037-33)

The 8950 may be fitted with either a 8034 or 8037 submodule which contains the VITC reader and character generator logic circuitry. Both submodules contain similar circuitry for the VITC reader and Character generator. The following description shows component designators for the 8037 board. Component designations in square brackets refer to the older 8034 board. Where only one component designator is shown the circuit number is the same on both boards.

The actual extraction of the VITC and insertion of the character data into the digital bitstream is done by the Keyer LCA circuitry on the main board. (See section 5.3.6) The Keyer LCA extracts video sync and pixel clock data from the digital video and passes it to the 8037 [8034] on the 40 pin header. Vertical sync (V) is on pin 15, Horizontal sync (H) is on pin 16, Field information (F) is on pin 1 and the digital sample clock (KCK) is on pin 2 of the header. The MCU address and data bus are also fed up the header from the main board. The majority of the logic for the VITC Reader/Character generator functions is contained in a programmable logic device (LCA) U18 [U9]. Its program is loaded from FLASH EPROM U2 on power up. Configuration latch U3 controls what part of the FLASH EPROM is used during loading of the LCA on power up.

The VITC data is clocked out of the keyer LCA on the main board and passed up the header on pin KC0 to the LCA on the submodule. The VITC bit rate is derived from the sample clock KCK in the LCA. For digital composite NTSC signals, each VITC bit is 8 sample clocks long. For digital component signals the VITC bit rate is 15 sample clocks per 2 VITC bits.

The decoded VITC bit rate clock is used to decode 0 and 1 bits inside the LCA. The LCA validates the cyclic redundancy check (CRC) word and sync bit patterns for the received data and writes the decoded data to RAM U1 [U7] one byte (8 bits) at a time. Once per field, the MCU unloads the recovered VITC data from the RAM on lines where VITC reading is enabled.

The majority of the logic for the character generator functions is also contained in a programmable logic device (LCA) U18 [U9]. The character

display is formatted to display 28 rows of 32 characters each in the tiny size, 14 rows the small size, and 7 rows in the large size. Each of the character positions corresponds to one location in static RAM U1 [U7]. The MCU writes characters into specified locations in the RAM corresponding to the position of the characters on the screen. RAM locations are scanned during each television field. Valid characters address corresponding sections of the character FLASH EPROM U2 and are loaded into the LCA one byte (8 bits) at a time. Each byte corresponds to either the left or right half of a character pixel line. The internal logic in the LCA controls how many lines per character and how many character lines there are on the raster according to registers set by the firmware.

The character pixel clock is derived from and is the same rate as the digital sample clock KCK. A 4 bit value representing the white level of each pixel is clocked out of the LCA on the KC0, KC1, KC2, and KC3 lines and fed down the header to the keyer LCA. The special value with all bits set to 1 disables the keyer where no characters are displayed. The character white level is encoded by the other 15 values to provide anti-aliasing of the character data. Maximum white level is set at 80 IRE, while character black level is fixed at setup level.

5.3.6. Keyer LCA (8025-32, 8025-35, 8025-37)

The heart of the 8950 is the Keyer LCA U17 on the main board. Input video from the serial input circuitry is fed to the inputs of the keyer LCA by U7, U8, and U9.

The keyer control signals from the VITC Reader / Character generator submodule and are fed down the 40 pin header from the 8037/8034 on the KC0, KC1, KC2, and KC3 lines and are used to control what data is being inserted into the bitstream and when it will be inserted. During the vertical interval, when VITC is being read, the VITC data is passed up the header on KC0. During the remainder of the field when characters are being generated, character data is passed down from the submodule on all four lines.
The keyer LCA provides parallel data out which is fed to the serial output circuitry. The LCA also generates the necessary signals required to control the analog output circuitry which is contained on the 8026/8029 submodule.

5.3.7. LTC Translator (8025-35) and (8037-33, or 8036-30)

The bit-rate generator, located in the main board LCA U17, divides the 14.456 Mhz crystal frequency down to twice the LTC bit frequency (4798 Hz for NTSC, and 4000 Hz for PAL). An interrupt to the MCU is generated on the MCU T0 interrupt in (main board U25 pin 7) every 4 bits. The MCU writes the next 4 bits to a register in the LCA and the data is clocked out from the LTCOUT (main board U17 pin 3) to the LTC shaping circuitry which is located on the 8037 or 8036 submodule.

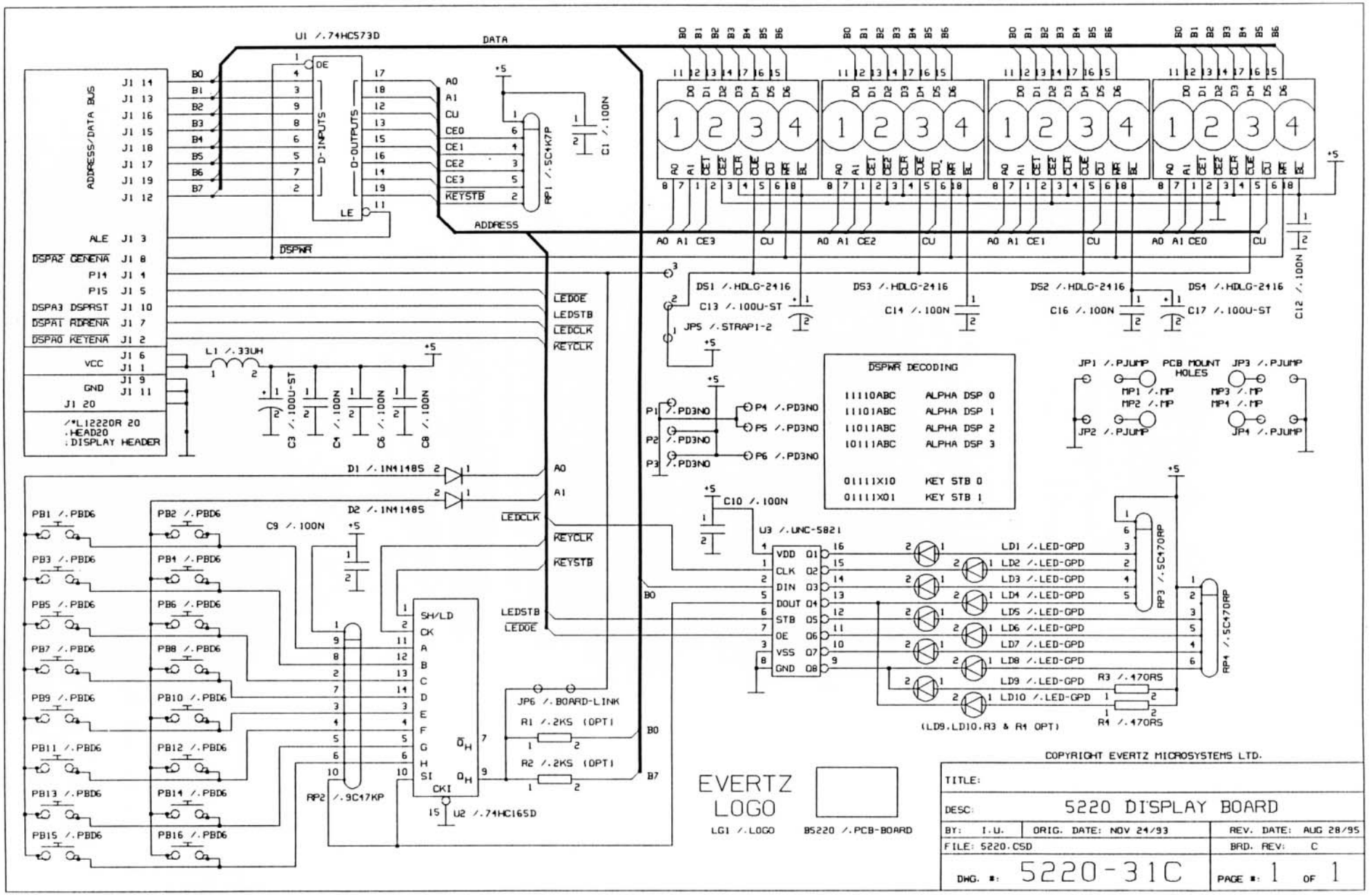
For 8950 units fitted with the 8037 VITC Reader submodule the LTC output driver circuitry is contained on the 8037 submodule. The LTC is shaped to

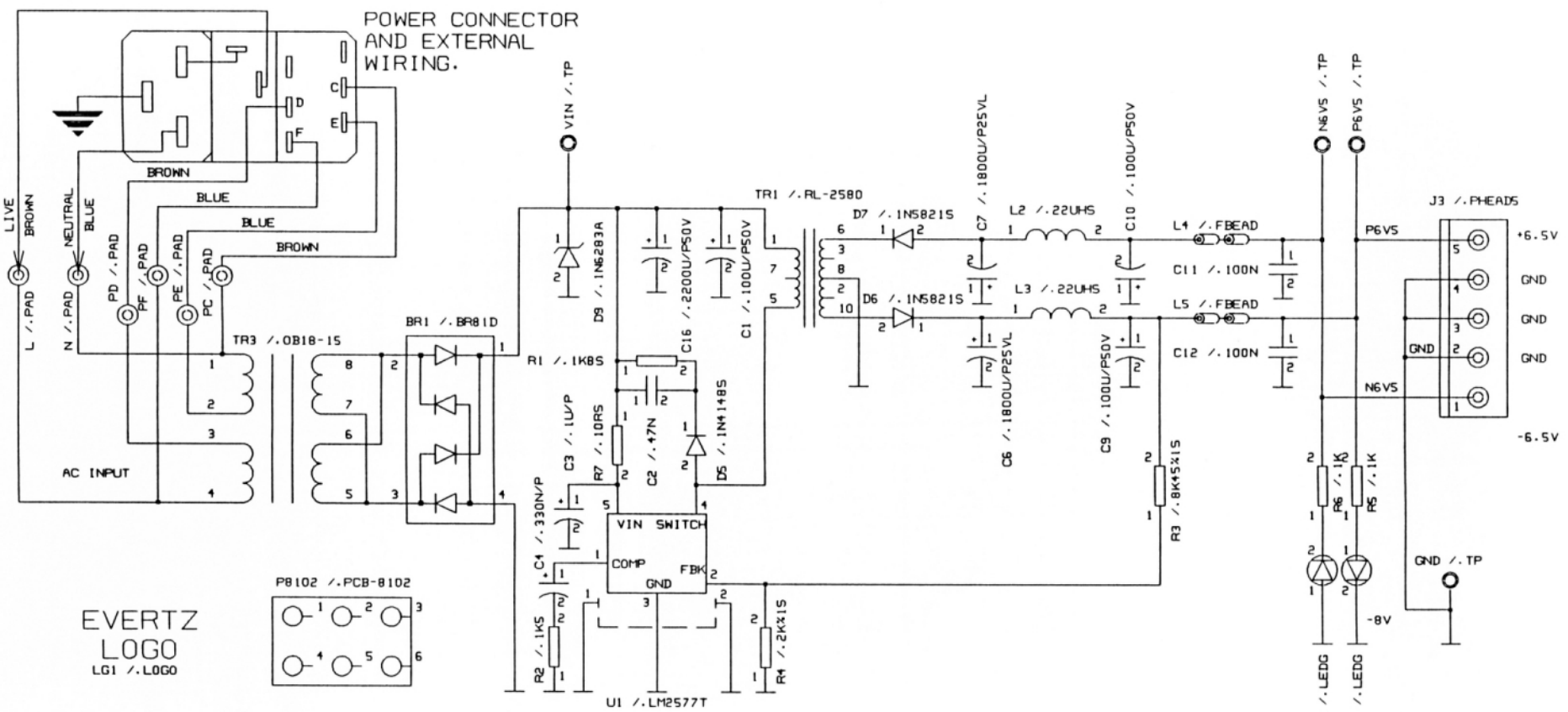
the correct rise and fall times by U15 and associated components and fed to the output driver U17. NOVPOT U16 is a digitally controlled potentiometer, set from the MCU and is used to control the output level of the LTC.

For 8950 units fitted with the 8034 VITC Reader submodule the LTC output driver circuitry is contained on a small circuit board (8036) mounted to the LTC Out connector. The LTC is shaped to the correct rise and fall times by U1 and associated components and fed to the output driver U2. Trimpot VR1 is used to control the output level of the LTC.

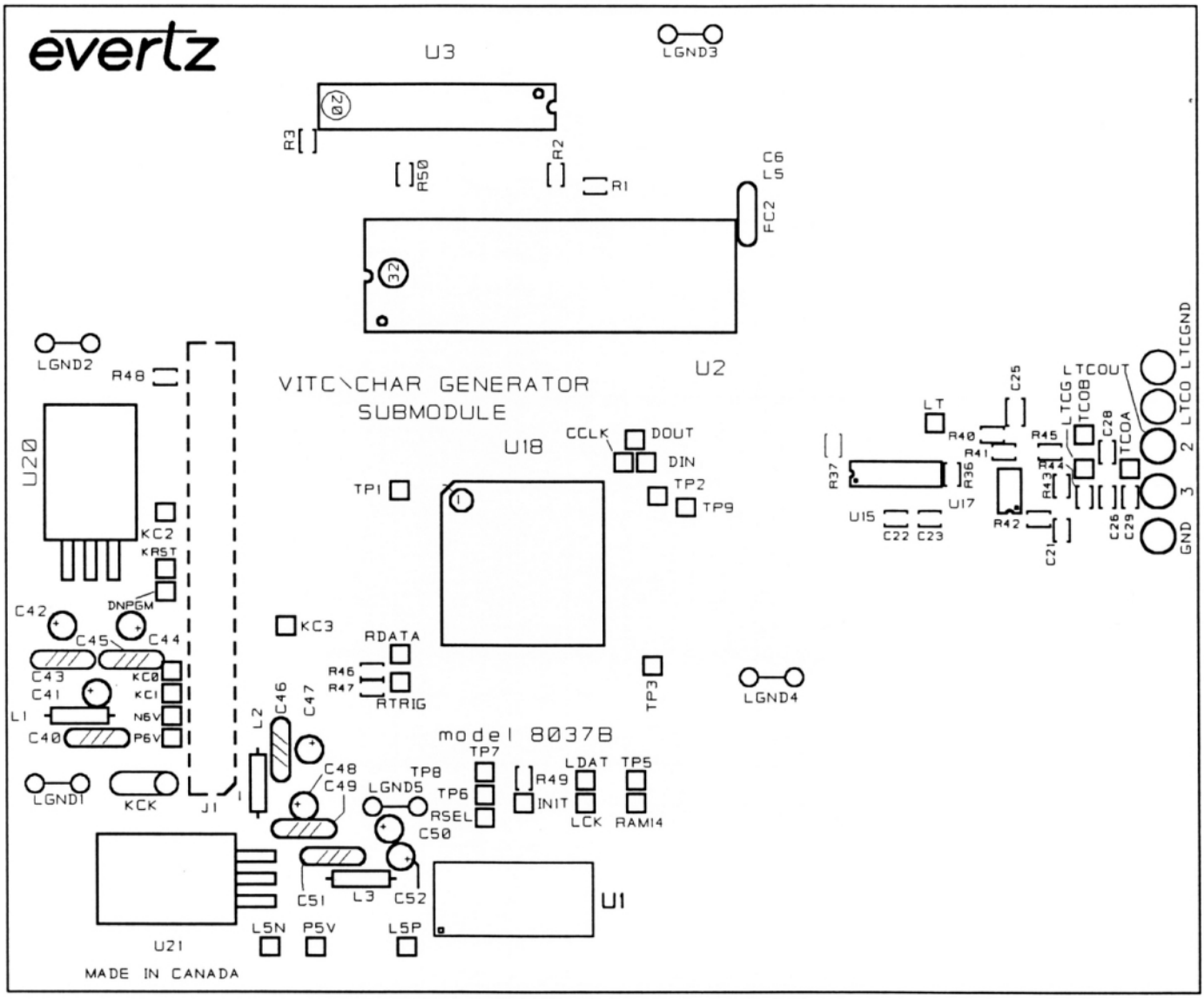
5.3.8. Analog Monitor Output - optional (8026-31, 8026-32) or (8029-31, 8029-32)

The 8950 may be fitted with either a 8026 or 8029 submodule submodule which contains the analog monitor output circuitry. Circuit designators on each of these two boards is similar, so the following description applies to both. The heart of the analog monitor is the 22191 Digital Video Encoder chip. When used in component (4:2:2) applications, Y/C data is demultiplexed by latches U4 and U5 and fed to the parallel data port of the 22191. The chrominance signals are modulated onto a digitally synthesized subcarrier by the 22191. Luminance and chrominance signals are separately interpolated at twice the pixel rate and digitally combined. The resulting composite signal is converted to analog levels by a 10 bit D/A converter and output to the analog filter circuitry. The encoder operates from a single clock which is running at 27 MHz (PXCK).

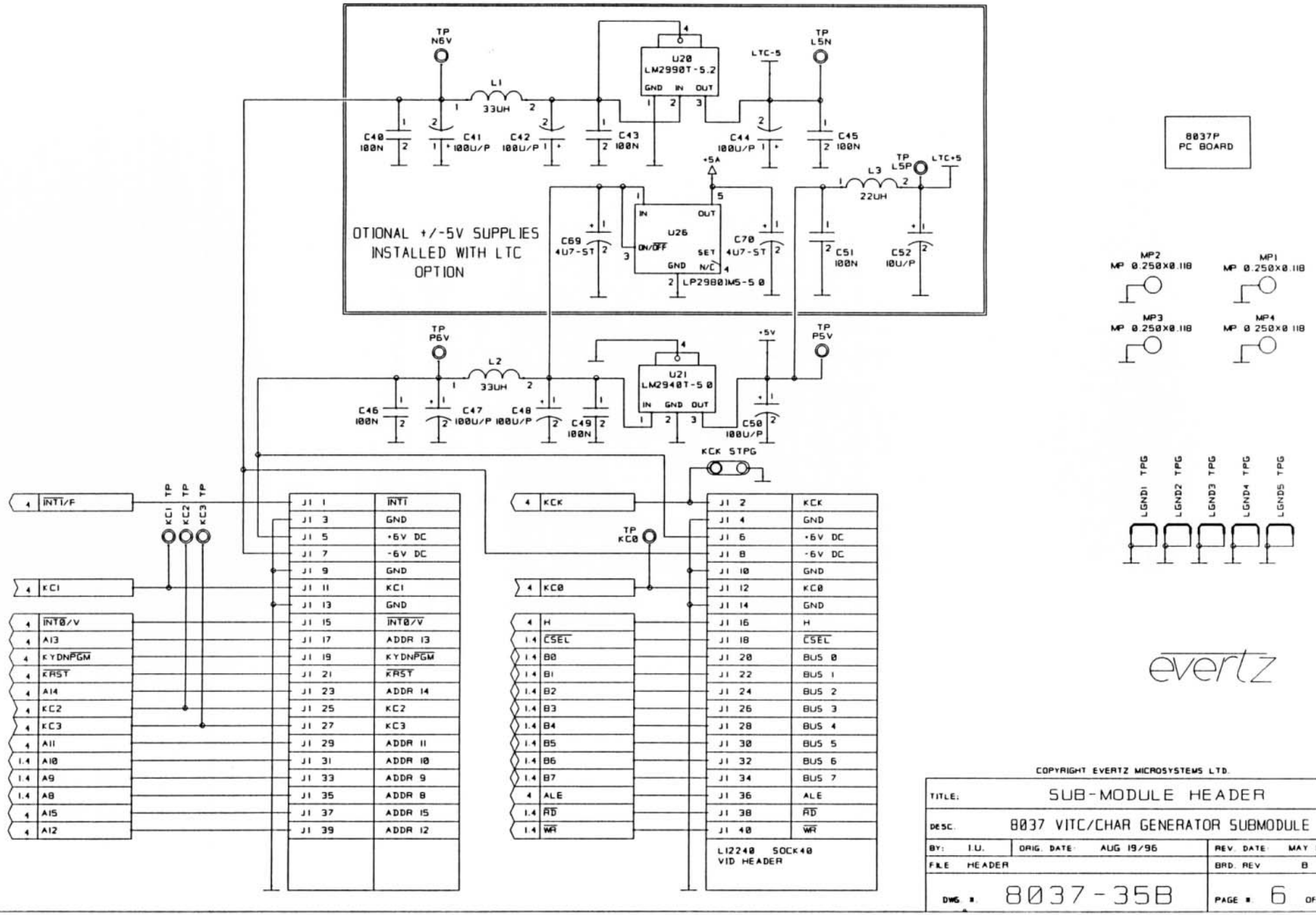

U1 /.74HC573D
DATA
ADDRESS/DATA BUS
ALE
DSPA2 GENENA
P14
P15
DSPA3 DSPRST
DSPA1 ADRENA
DSPA0 KEYENA
VCC
GND
/*L12220R 20
.HEAD20
;DISPLAY HEADER
L1 /.33UH
C3 /.100U-ST
C4 /.100N
C6 /.100N
C8 /.100N
DSPWR
ADDRESS
RP1 /.SC47K7P
C1 /.100N
LEDOE
LEDSTB
LEDCLK
KEYCLK
DS1 /.HDLG-2416
DS3 /.HDLG-2416
DS2 /.HDLG-2416
DS4 /.HDLG-2416
C13 /.100U-ST
C14 /.100N
C16 /.100N
C17 /.100U-ST
C12 /.100N
JPS /.STRAP1-2
DSPWR DECODING
11110ABC ALPHA DSP 0
11101ABC ALPHA DSP 1
11011ABC ALPHA DSP 2
10111ABC ALPHA DSP 3
01111X10 KEY STB 0
01111X01 KEY STB 1
P1 /.PD3NO
P2 /.PD3NO
P3 /.PD3NO
P4 /.PD3NO
P5 /.PD3NO
P6 /.PD3NO
JP1 /.PJUMP
JP2 /.PJUMP
JP3 /.PJUMP
JP4 /.PJUMP
PCB MOUNT HOLES
MP1 /.MP
MP2 /.MP
MP3 /.MP
MP4 /.MP
D1 /.1N4148S
D2 /.1N4148S
C9 /.100N
C10 /.100N
U3 /.UNC-5821
LD1 /.LED-GPD
LD2 /.LED-GPD
LD3 /.LED-GPD
LD4 /.LED-GPD
LD5 /.LED-GPD
LD6 /.LED-GPD
LD7 /.LED-GPD
LD8 /.LED-GPD
LD9 /.LED-GPD
LD10 /.LED-GPD
RP3 /.SC470RP
RP4 /.SC470RP
R3 /.470RS
R4 /.470RS
(LD9,LD10,R3 & R4 OPT)
PB1 /.PBD6
PB2 /.PBD6
PB3 /.PBD6
PB4 /.PBD6
PB5 /.PBD6
PB6 /.PBD6
PB7 /.PBD6
PB8 /.PBD6
PB9 /.PBD6
PB10 /.PBD6
PB11 /.PBD6
PB12 /.PBD6
PB13 /.PBD6
PB14 /.PBD6
PB15 /.PBD6
PB16 /.PBD6
RP2 /.9C47KP
U2 /.74HC165D
JP6 /.BOARD-LINK
R1 /.2KS (OPT)
R2 /.2KS (OPT)
EVERTZ LOGO
LG1 /.LOGO
B5220 /.PCB-BOARD
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE:
DESC: 5220 DISPLAY BOARD
BY: I.U.
ORIG. DATE: NOV 24/93
REV. DATE: AUG 28/95
FILE: 5220.CSD
BRD. REV: C
DWG. #: 5220-31C
PAGE # 1 OF 1



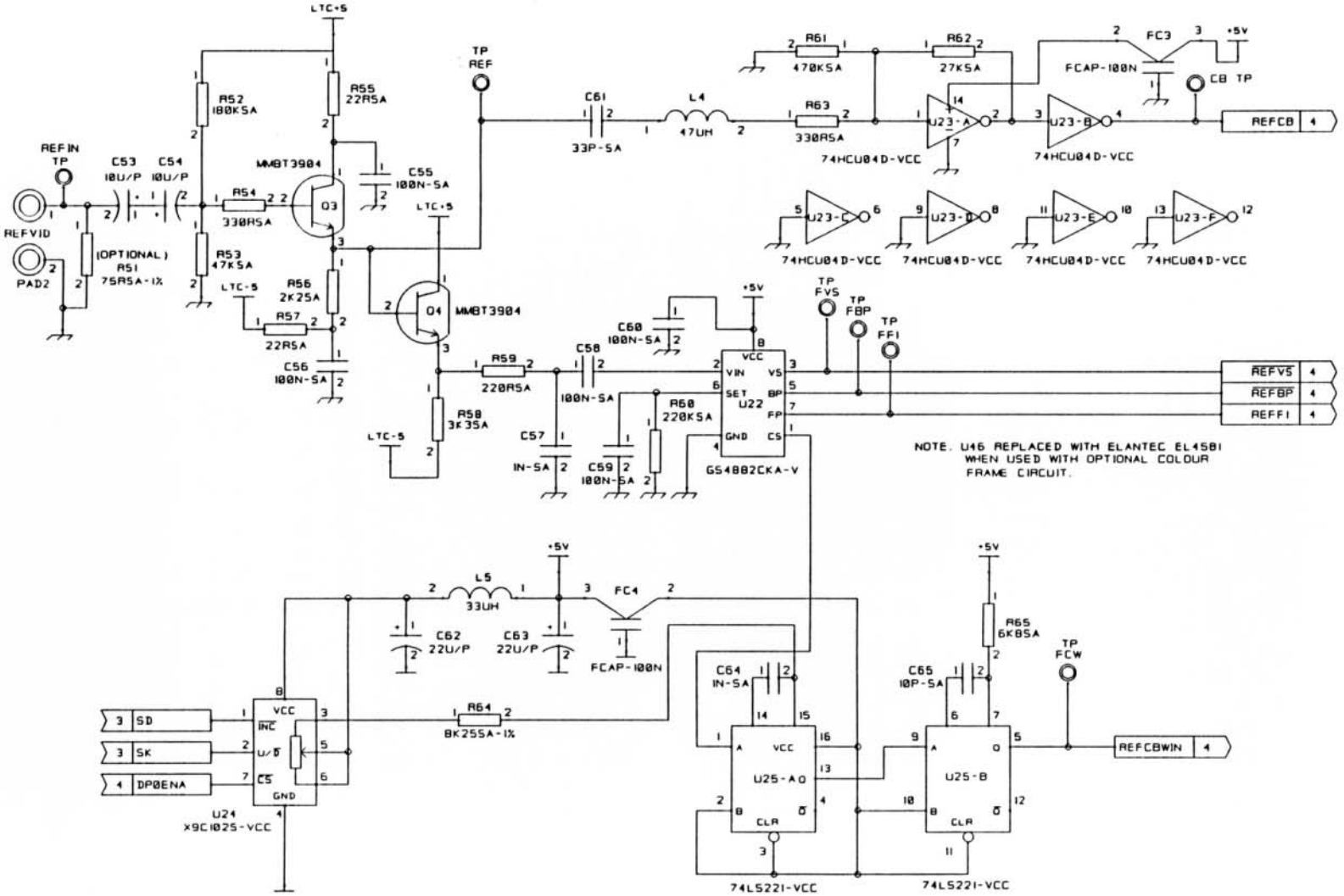
TITLE:		
DESC:	POWER SUPPLY CIRCUIT	
BY: I.U.	ORIG. DATE: FEB 26/93	REV. DATE: MAY 6/94
FILE: PWR.CSD		BRD. REV: A
DWG. #: 8102-31A		PAGE #: 1 OF 1



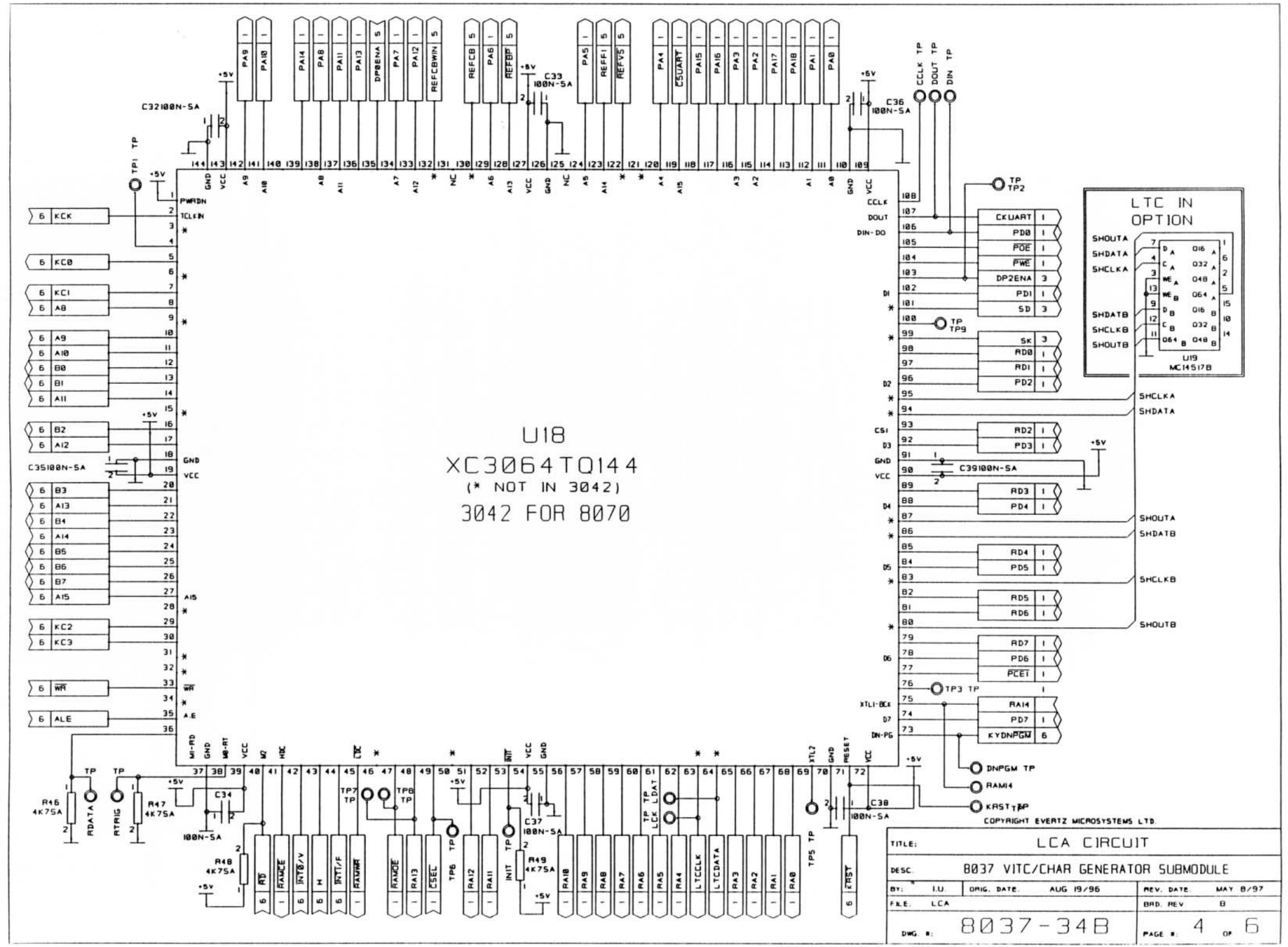
EVERTZ	BOARD NO. : MODEL 8037 VITC/CHAR GEN SUBMODULE	TITLE: MODEL 8037 COMPONENT LAYOUT FOR INSTALLATION IN 8950	REV: B	DWN I.U.
		DATE: MAY 21/97	DWG NO. : 8037B-82	

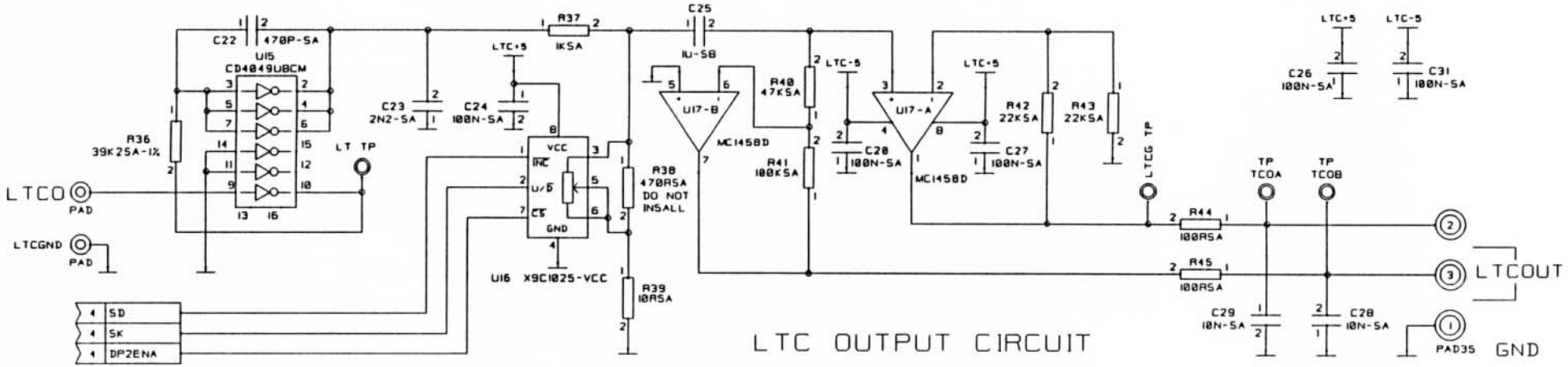


TITLE:	SUB-MODULE HEADER		
DESC.	8037 VITC/CHAR GENERATOR SUBMODULE		
BY: I.U.	ORIG. DATE: AUG 19/96		REV. DATE: MAY 8/97
FILE HEADER			BRD. REV B
DWG. # 8037-35B			PAGE # 6 OF 6



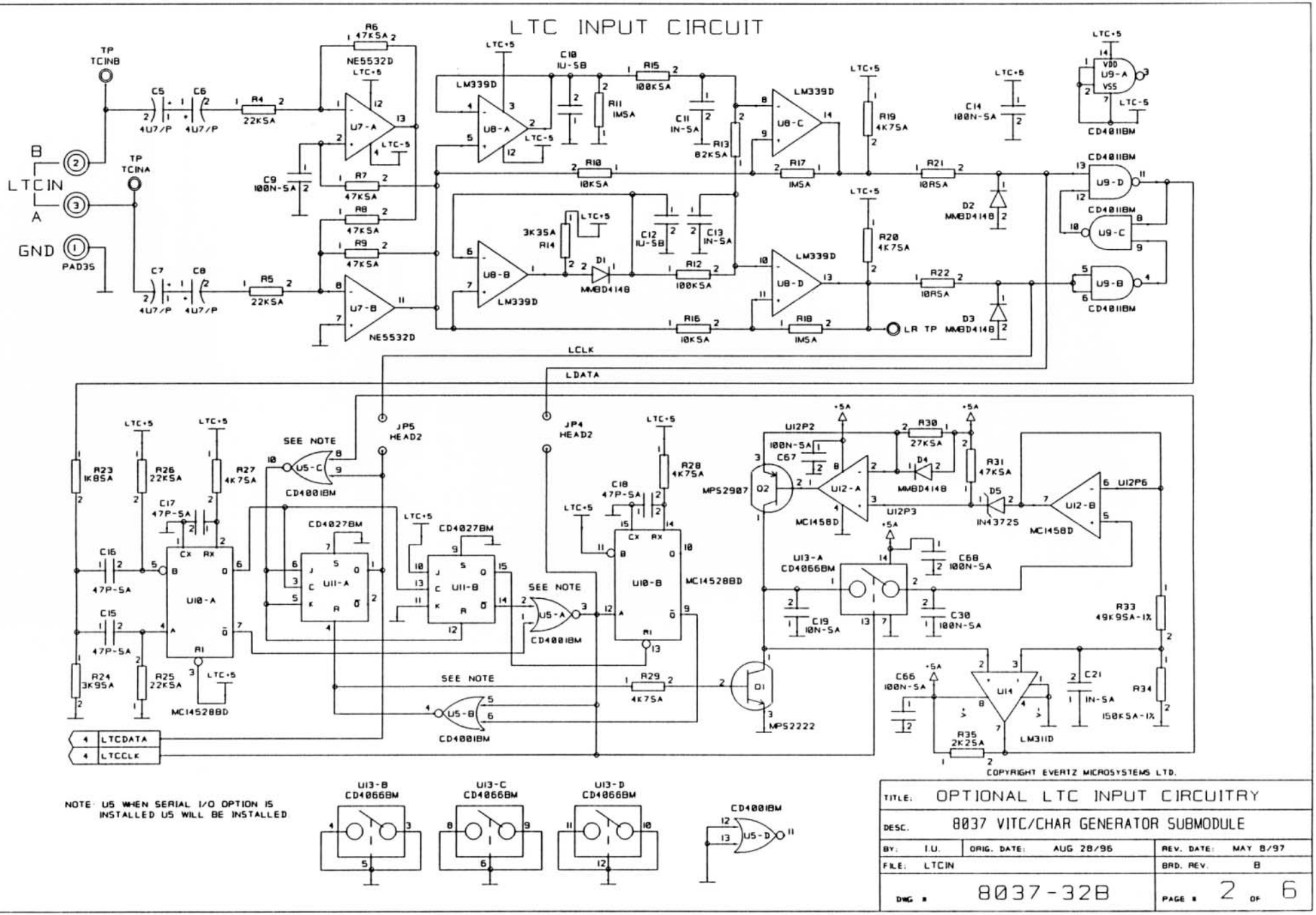
TITLE:	OPTIONAL COLOUR FRAME & REF VIDEO CIRCUIT		
DESC.	8037 VITC/CHAR GENERATOR SUBMODULE		
BY: I.U.	ORIG. DATE: AUG 19/96	REV. DATE:	MAY 8/97
FILE REF		BRD REV	B
DWG. #.	8037-35B	PAGE #.	5 OF 6


U18
XC3064TQ144
(* NOT IN 3042)
3042 FOR 8070
LTC IN OPTION
U19
MC145178
C32 100N-SA
C33 100N-SA
C34 100N-SA
C35 100N-SA
C36 100N-SA
C37 100N-SA
C38 100N-SA
C39 100N-SA
R46 4K7SA
R47 4K7SA
R48 4K7SA
R49 4K7SA
TP1 TP
TP2
TP3 TP
TP6 TP
TP7 TP
TP8 TP
TP9
TP5 TP
CCLK TP
DOUT TP
DIN TP
DNPGM TP
RAM4
KRST TP
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE: LCA CIRCUIT
DESC. 8037 VITC/CHAR GENERATOR SUBMODULE
BY: I.U. ORIG. DATE. AUG 19/96 REV. DATE. MAY 8/97
FILE. LCA BRD. REV B
DWG. #: 8037-34B PAGE # 4 OF 6

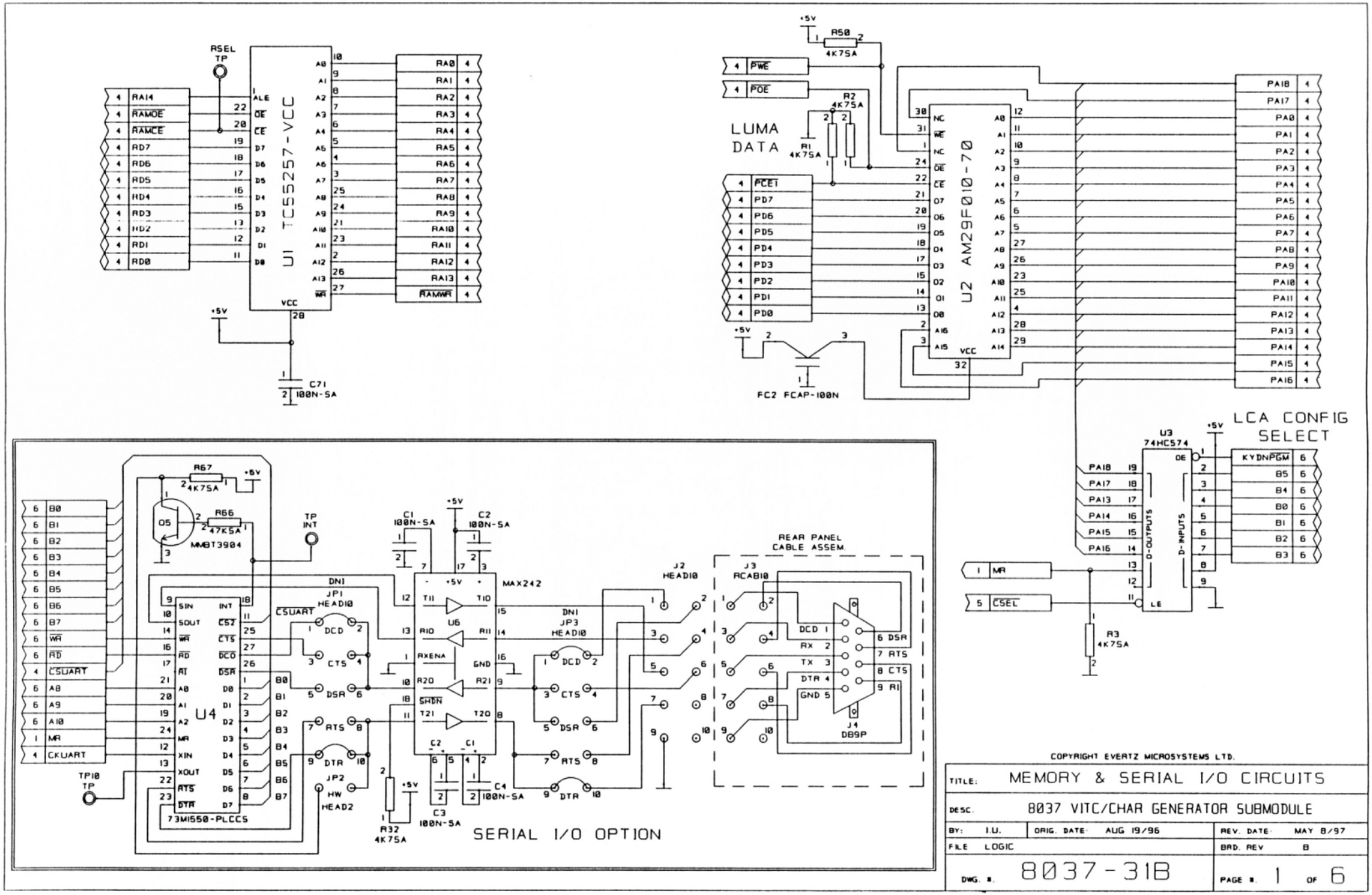


LTC OUTPUT CIRCUIT

TITLE:	OPTIONAL LTC OUTPUT CIRCUITRY		
DESC.	8037 VITC/CHAR GENERATOR SUBMODULE		
BY: I.U.	ORIG DATE: AUG 19/96	REV. DATE:	MAY 8/97
FILE LTCOUT		BRD. REV	B
DWG. #	8037-33B	PAGE #	3 OF 6

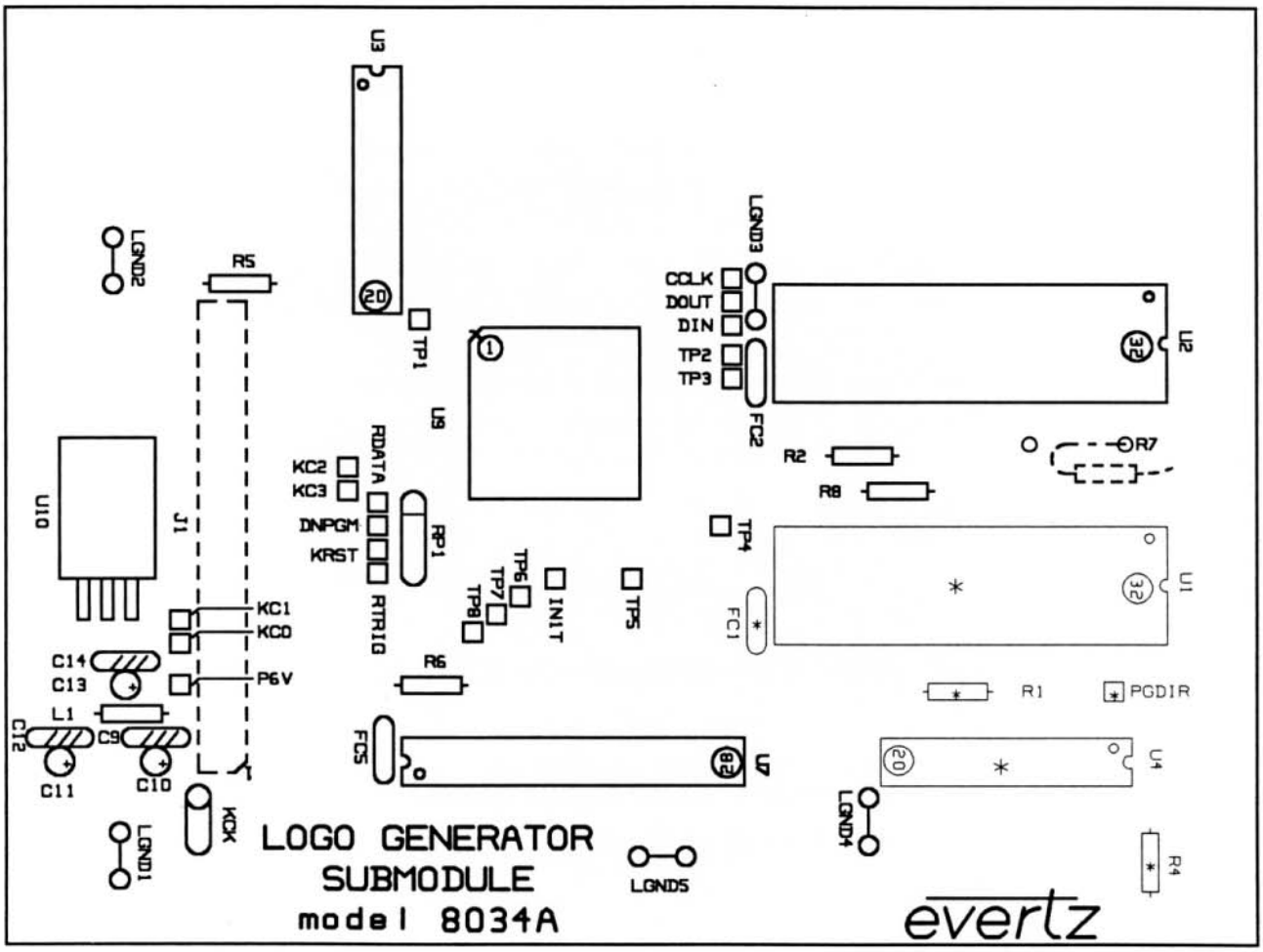


TITLE:	OPTIONAL LTC INPUT CIRCUITRY		
DESC.	8037 VITC/CHAR GENERATOR SUBMODULE		
BY: I.U.	ORIG. DATE: AUG 28/96	REV. DATE: MAY 8/97	
FILE: LTCIN		BRD. REV. B	
DWG # 8037-32B		PAGE # 2 OF 6	



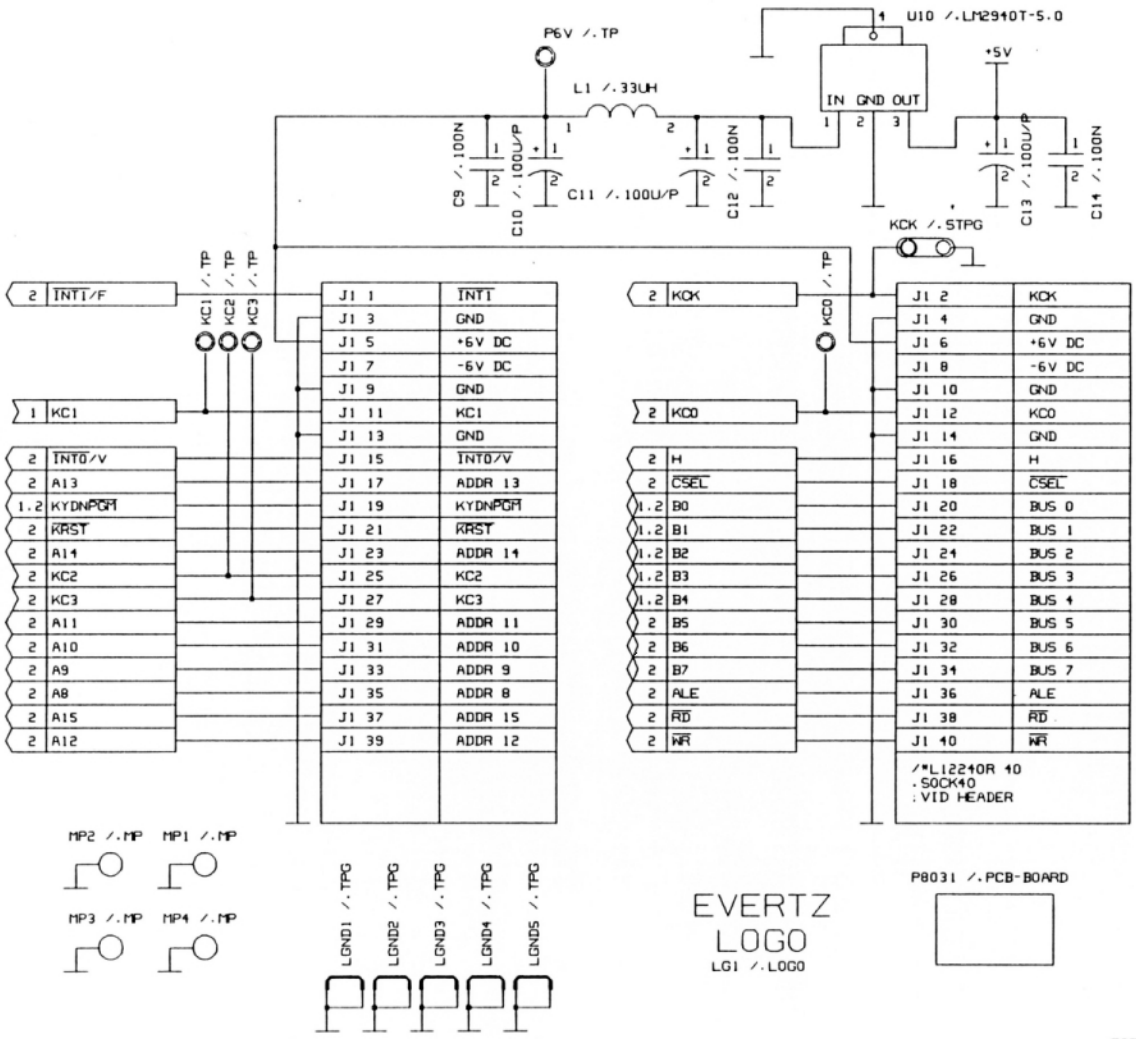
COPYRIGHT EVERTZ MICROSYSTEMS LTD.

TITLE:	MEMORY & SERIAL I/O CIRCUITS		
DESC.	8037 VITC/CHAR GENERATOR SUBMODULE		
BY: I.U.	ORIG. DATE: AUG 19/96		REV. DATE: MAY 8/97
FILE LOGIC			BRD. REV B
DWG. #.	8037-31B		PAGE #. 1 OF 6

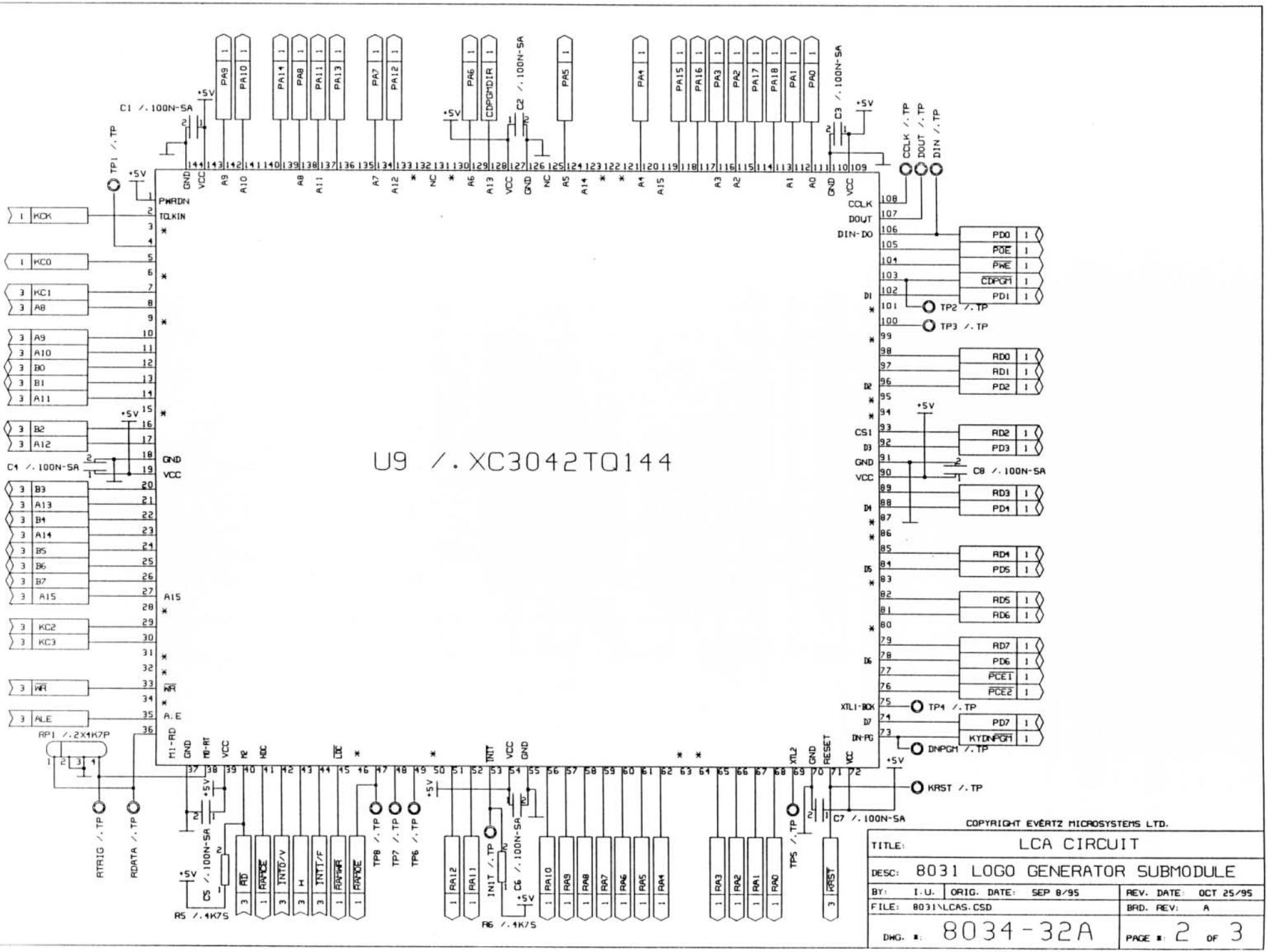


* = NOT INSTALLED

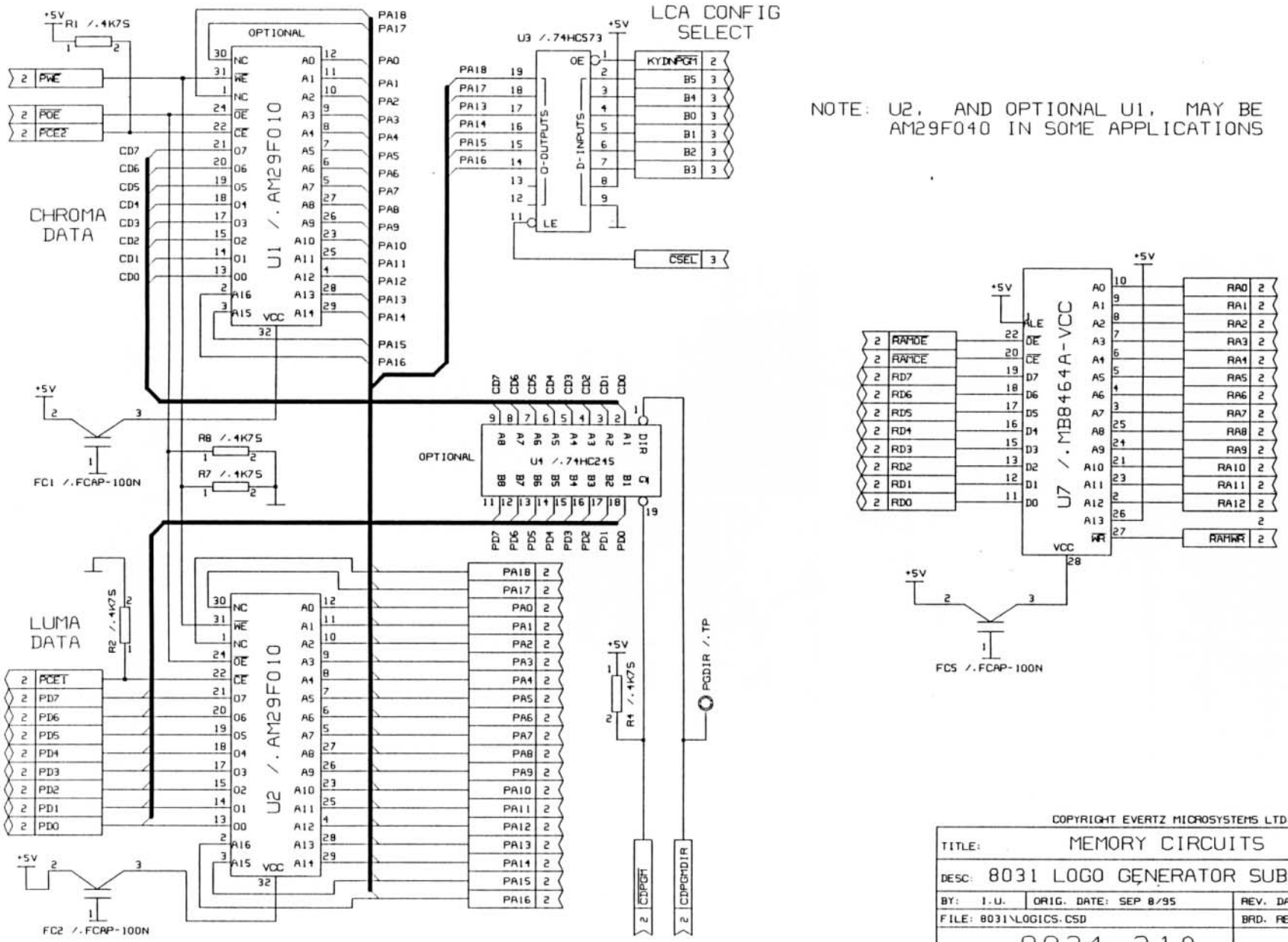
EVERTZ	BOARD NO. : 8034 LOGO GENERATOR SUB-MODULE	TITLE: MODEL 8034 COMPONENT LAYOUT	REV: A	DWN I.U.
		DATE: MAR 1/96	DWG NO. : 8034-80A	

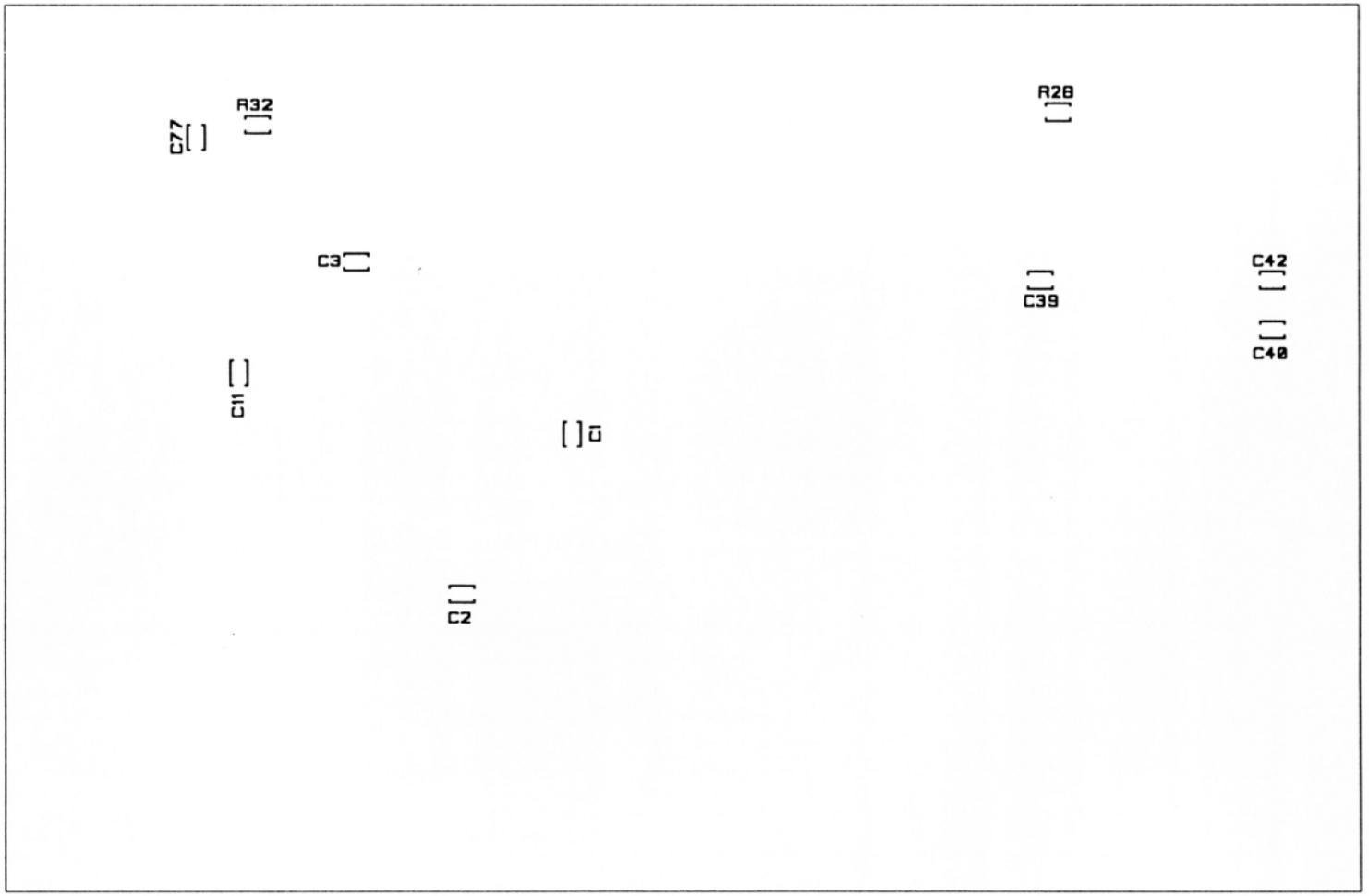


TITLE:	SUB-MODULE HEADER		
DESC:	8031 LOGO GENERATOR SUBMODULE		
BY: I.U.	ORIG. DATE: SEP 8/95		REV. DATE: OCT 25/95
FILE: 8031\HEADERS.CSD			BRD. REV: A
DWG. #: 8034-33A			PAGE #: 3 OF 3

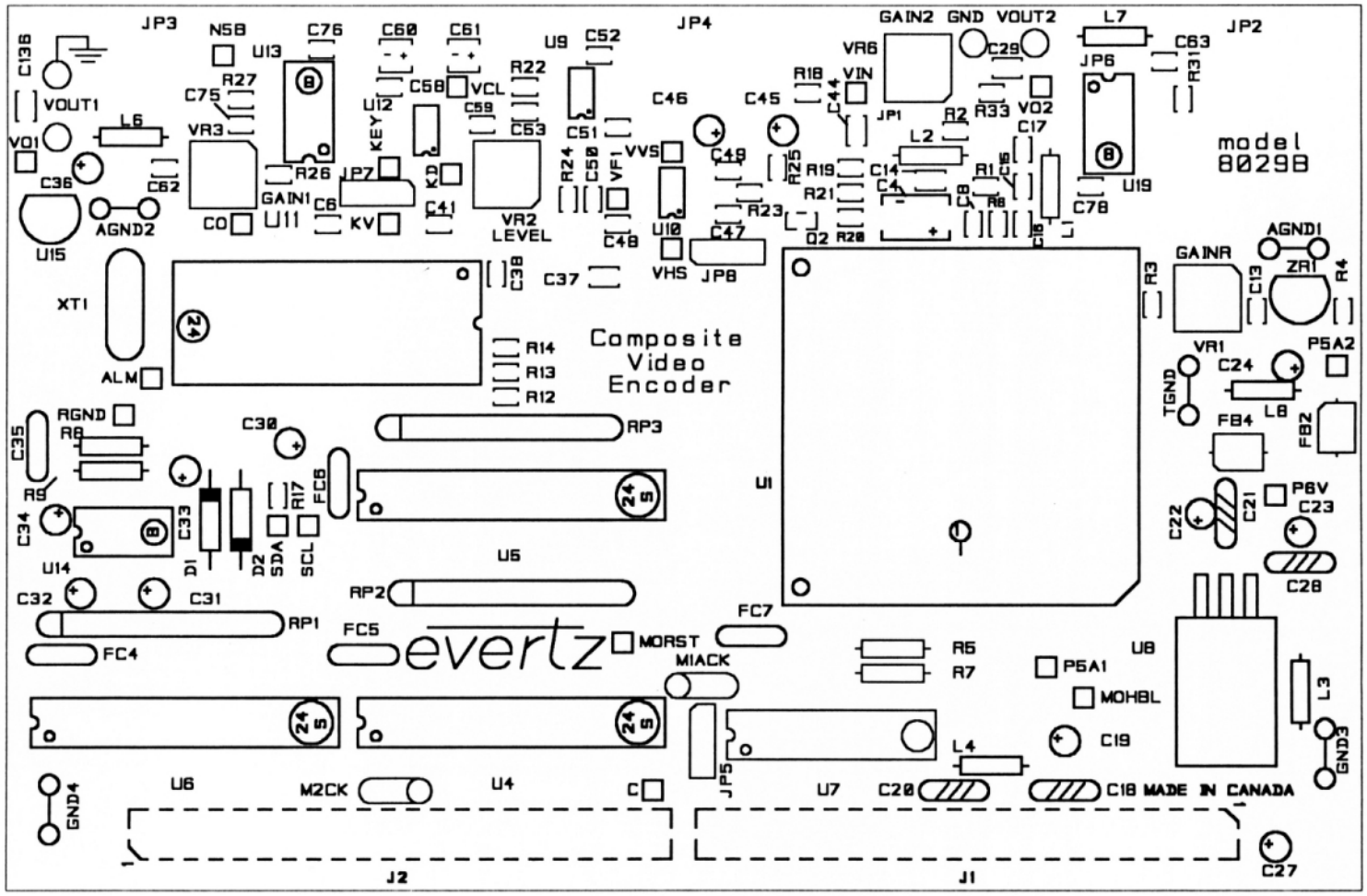


TITLE:	LCA CIRCUIT		
DESC:	8031 LOGO GENERATOR SUBMODULE		
BY: I.U.	ORIG. DATE: SEP 8/95		REV. DATE: OCT 25/95
FILE: 8031\LCAS.CSD			BRD. REV: A
DWG. #: 8034-32A			PAGE #: 2 OF 3


LCA CONFIG SELECT
NOTE: U2, AND OPTIONAL U1, MAY BE AM29F040 IN SOME APPLICATIONS
CHROMA DATA
LUMA DATA
OPTIONAL
U1 /.AM29F010
U2 /.AM29F010
U3 /.74HCS73
U4 /.74HC245
U7 /.MB8464A-VCC
R1 /.4K7S
R2 /.4K7S
R4 /.4K7S
R7 /.4K7S
R8 /.4K7S
FC1 /.FCAP-100N
FC2 /.FCAP-100N
FC5 /.FCAP-100N
PGDIR /.TP
KYDNPGM
CSEL
PWE
POE
PCE2
PCET
RAMDE
RAMCE
RAMWR
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE: MEMORY CIRCUITS
DESC: 8031 LOGO GENERATOR SUBMODULE
BY: I.U.
ORIG. DATE: SEP 8/95
REV. DATE: OCT 25/95
FILE: 8031\LOGICS.CSD
BRD. REV: A
DWG. #: 8034-31A
PAGE #: 1 OF 3

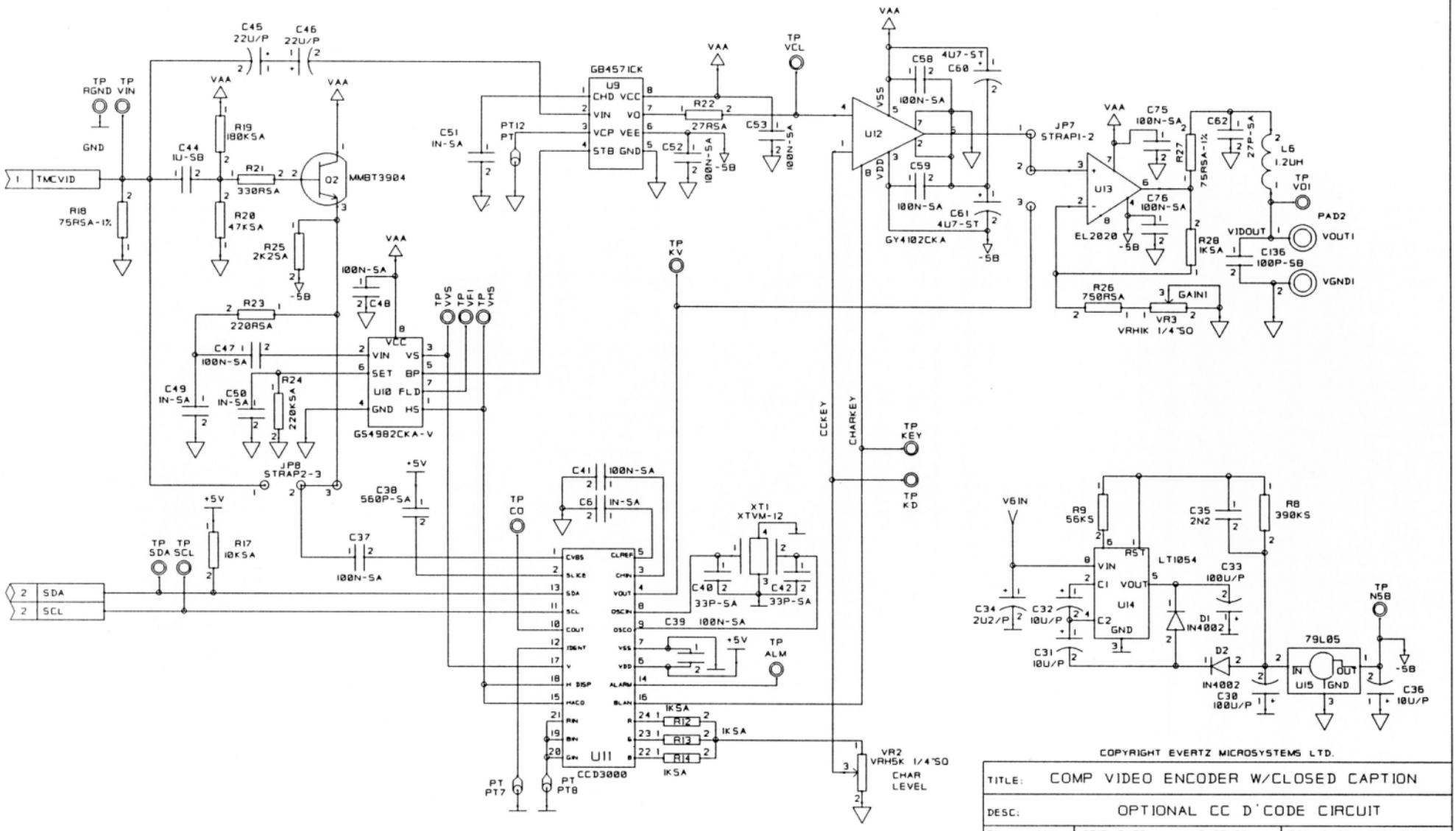


EVERTZ	TITLE: MODEL 8029 COMPOSITE VIDEO ENCODER	
TITLE : BOTTOM COMPONENT LAYOUT	DWN BY: I.U.	REV. B
DATE: JUN 28/96	REV DATE: FEB 19/97	DWG No.: 8029-81B

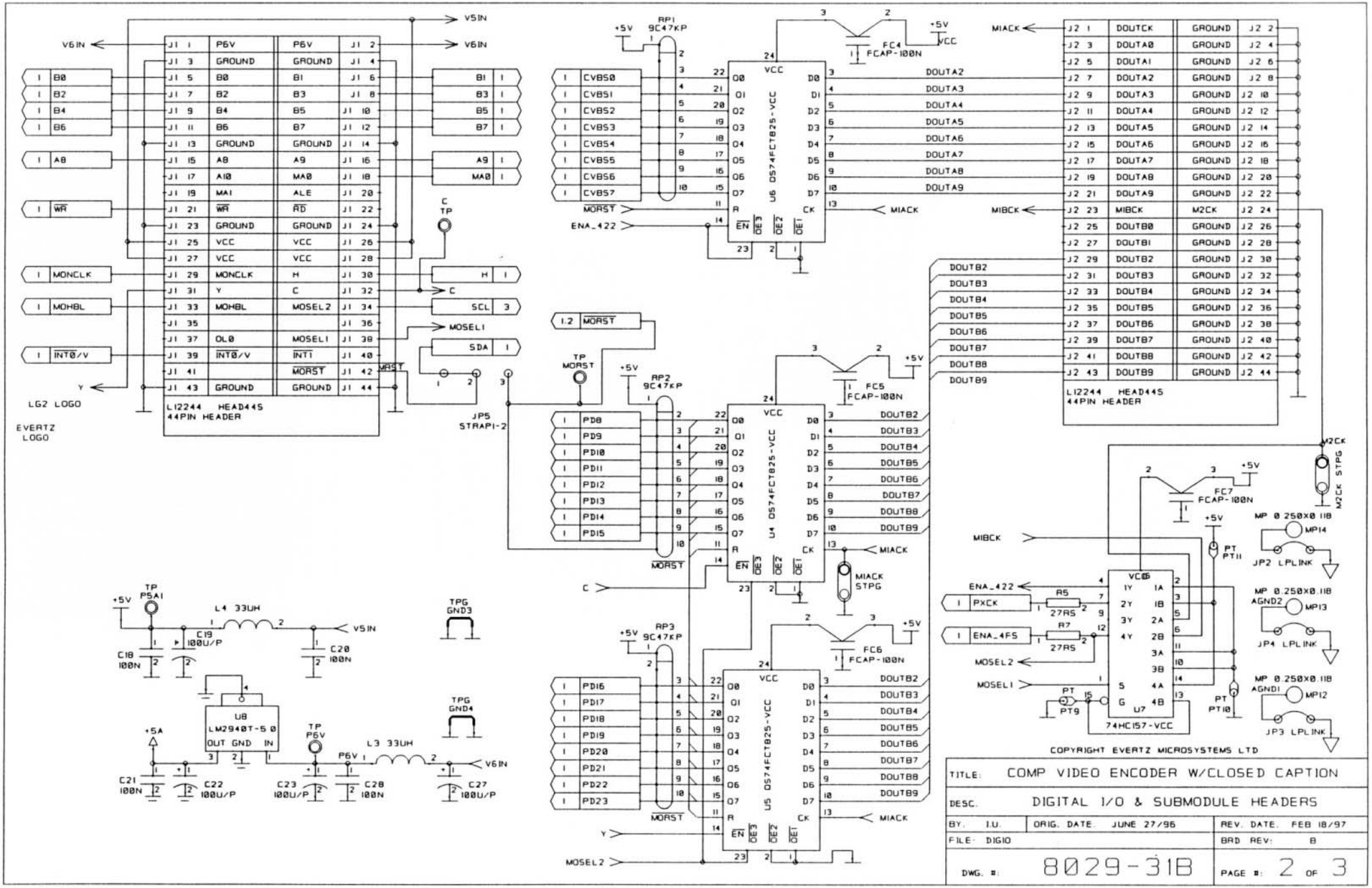


C1, C2, C3 , C11, C39, C40,C42,C77
R28 & R32 ARE MOUNTED ON BACK
OF BOARD.

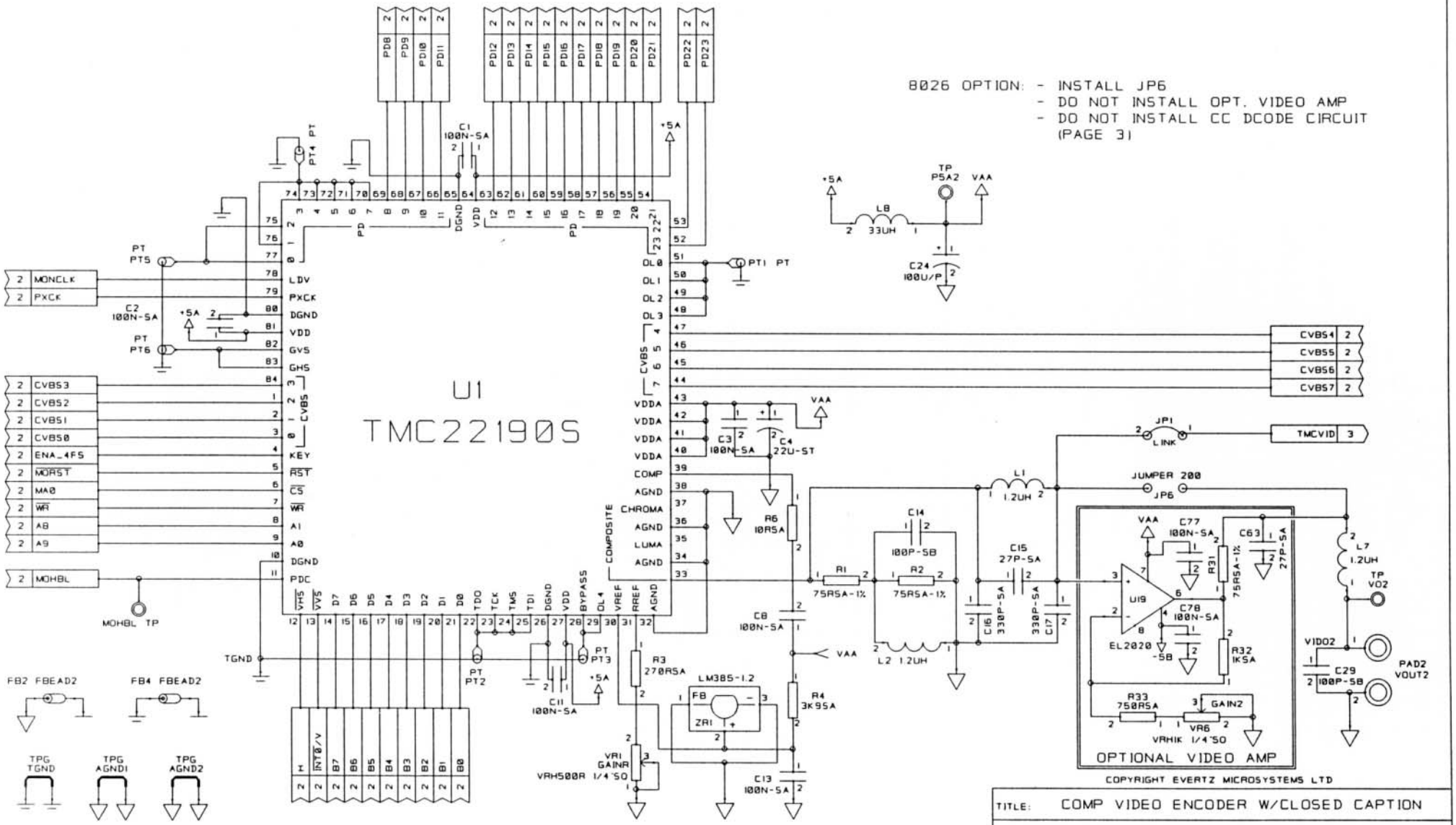
EVERTZ		TITLE: MODEL 8029 COMPOSITE VIDEO ENCODER
TITLE : TOP COMPONENT LAYOUT		DWN BY: I.U. | REV: B
DATE: JUN 28/96	REV DATE: FEB 19/97	DWG No.: 8029-80B

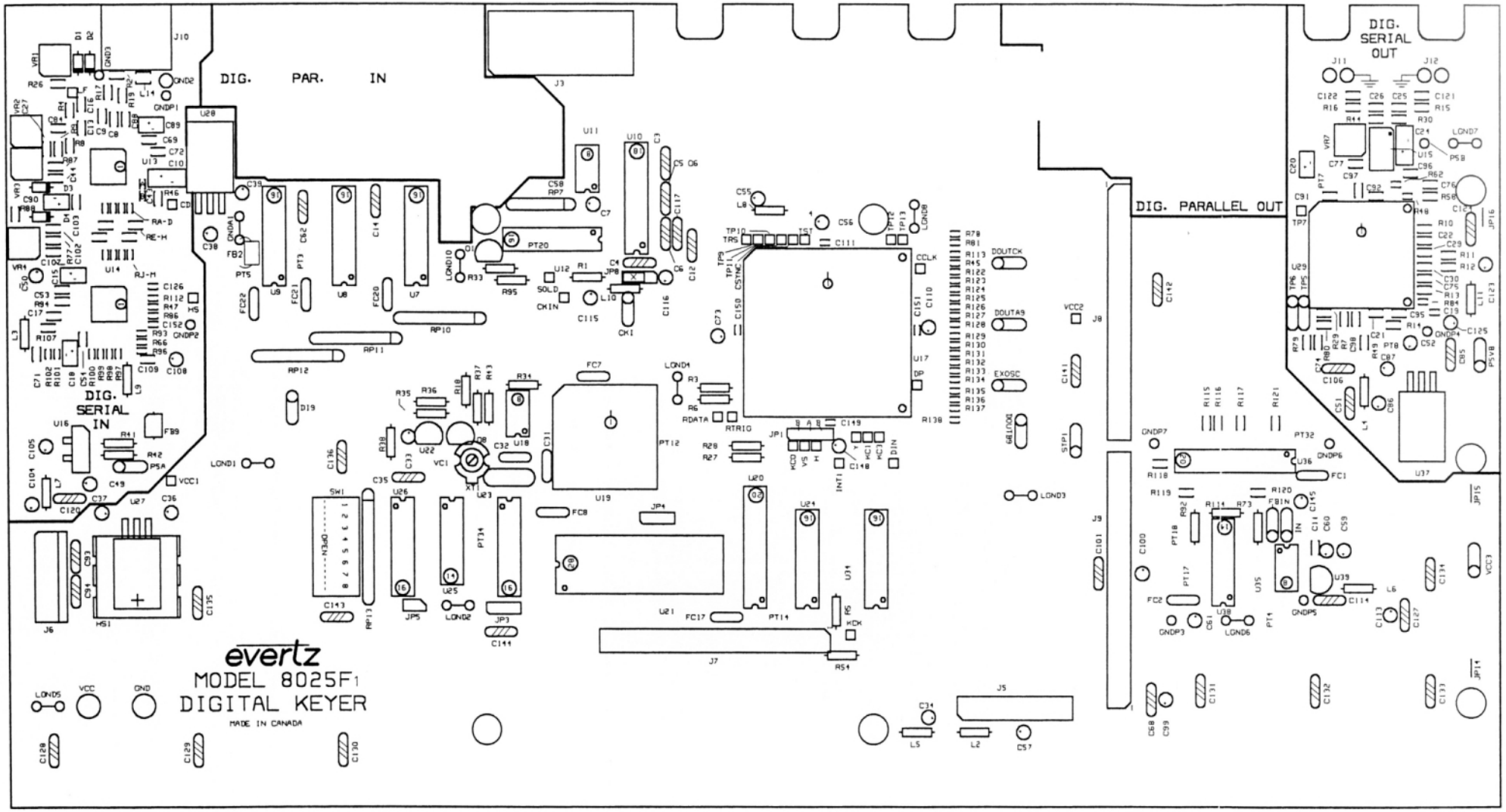


TITLE:	COMP VIDEO ENCODER W/CLOSED CAPTION		
DESC:	OPTIONAL CC D'CODE CIRCUIT		
BY: I.U.	ORIG. DATE: JUNE 27/96		REV. DATE: FEB 18/97
FILE: VIDEO_10			BRD. REV: B
DWG. #: 8029-32B			PAGE #: 3 OF 3

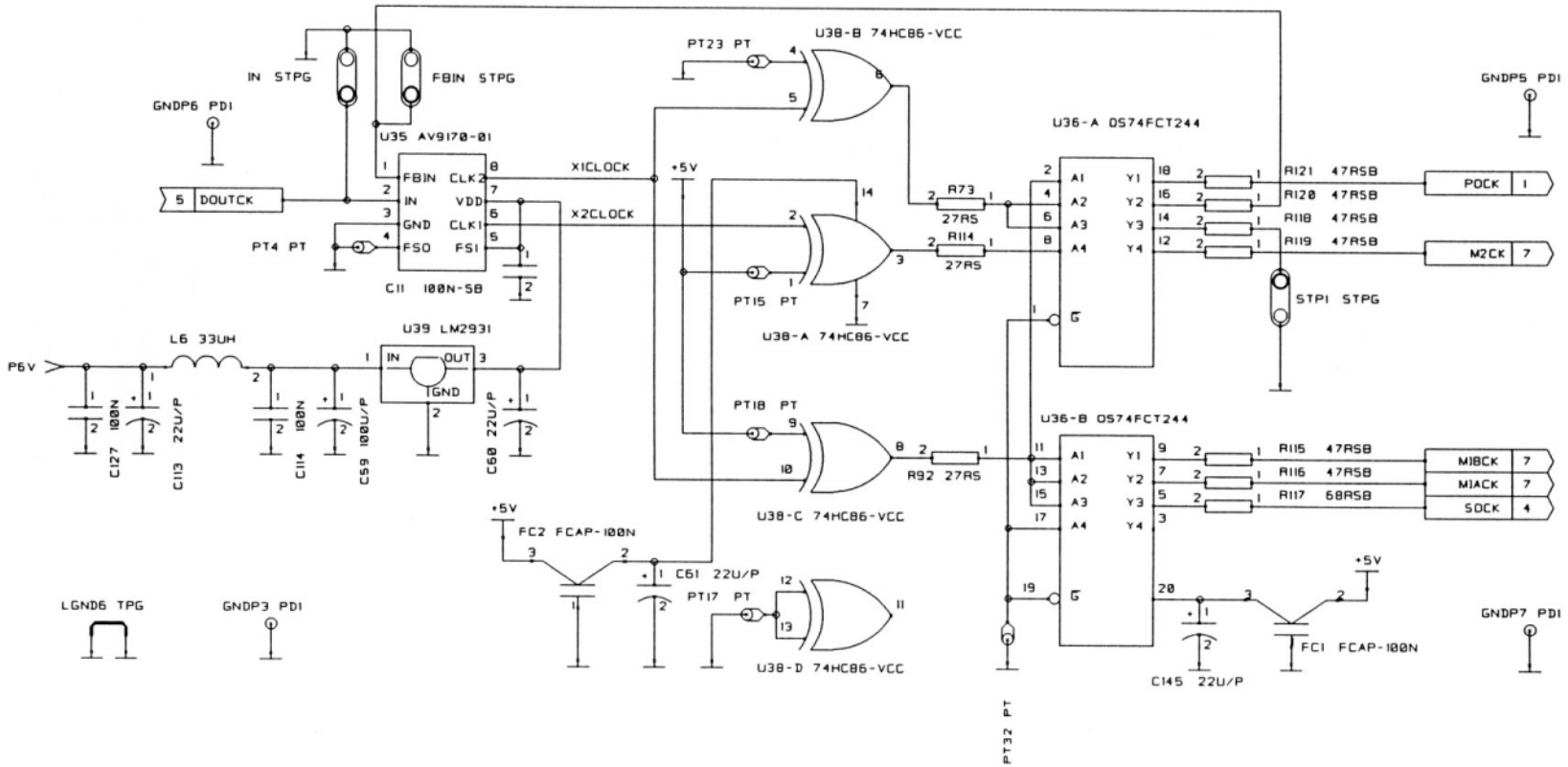


TITLE:	COMP VIDEO ENCODER W/CLOSED CAPTION		
DESC.	DIGITAL I/O & SUBMODULE HEADERS		
BY. I.U.	ORIG. DATE. JUNE 27/96	REV. DATE. FEB 18/97	
FILE: DIGIO		BRD REV: B	
DWG. #: 8029-31B		PAGE #: 2 OF 3	

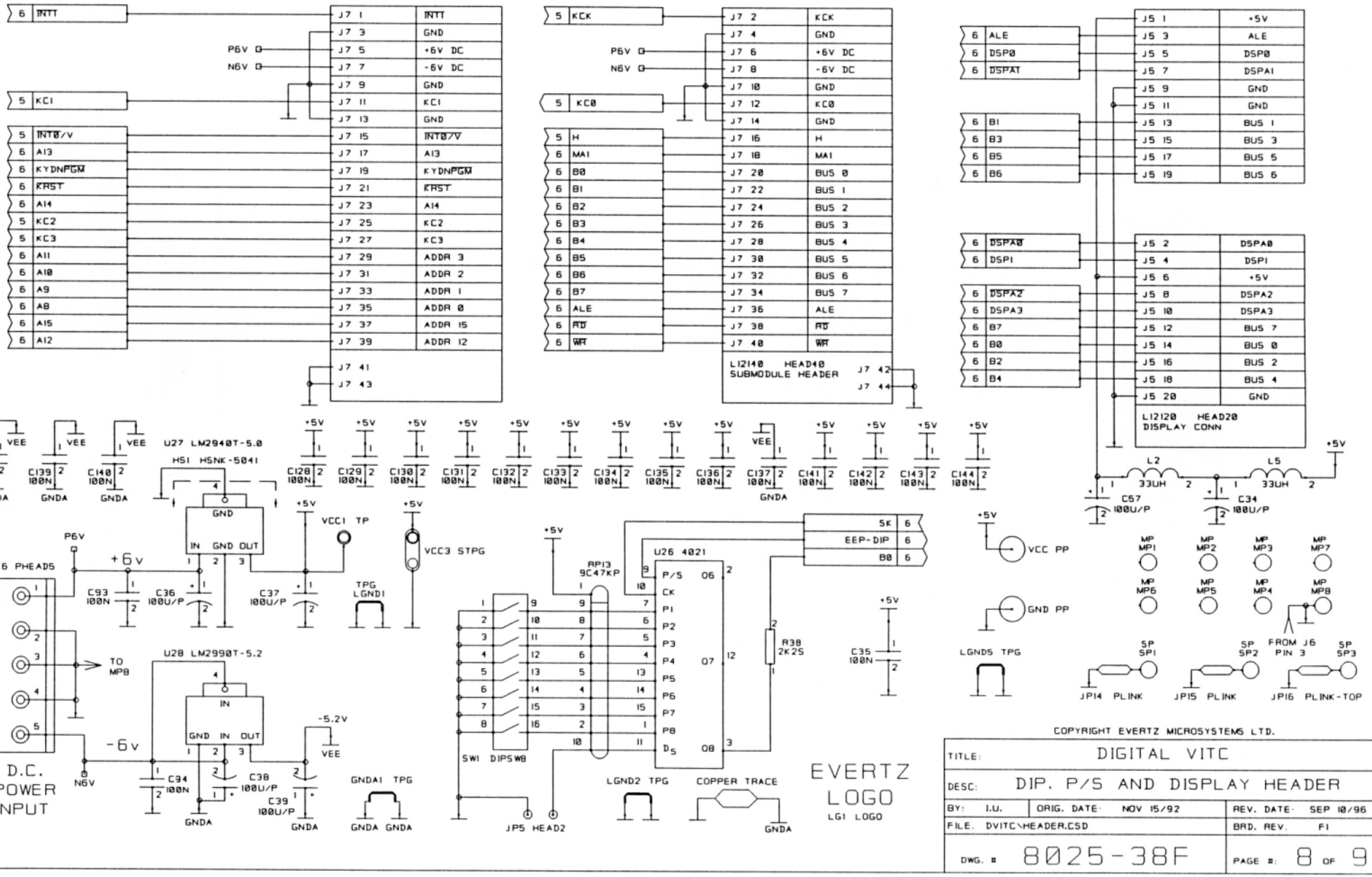

8026 OPTION: - INSTALL JP6
- DO NOT INSTALL OPT. VIDEO AMP
- DO NOT INSTALL CC DCODE CIRCUIT (PAGE 3)
U1
TMC22190S
OPTIONAL VIDEO AMP
COPYRIGHT EVERTZ MICROSYSTEMS LTD
TITLE: COMP VIDEO ENCODER W/CLOSED CAPTION
DESC. VIDEO ENCODER
BY. I.U. ORIG. DATE. JUNE 27/96 REV. DATE. FEB 18/97
FILE: VIDENC BRD REV: B
DWG. #: 8029-30B PAGE #: 1 OF 3



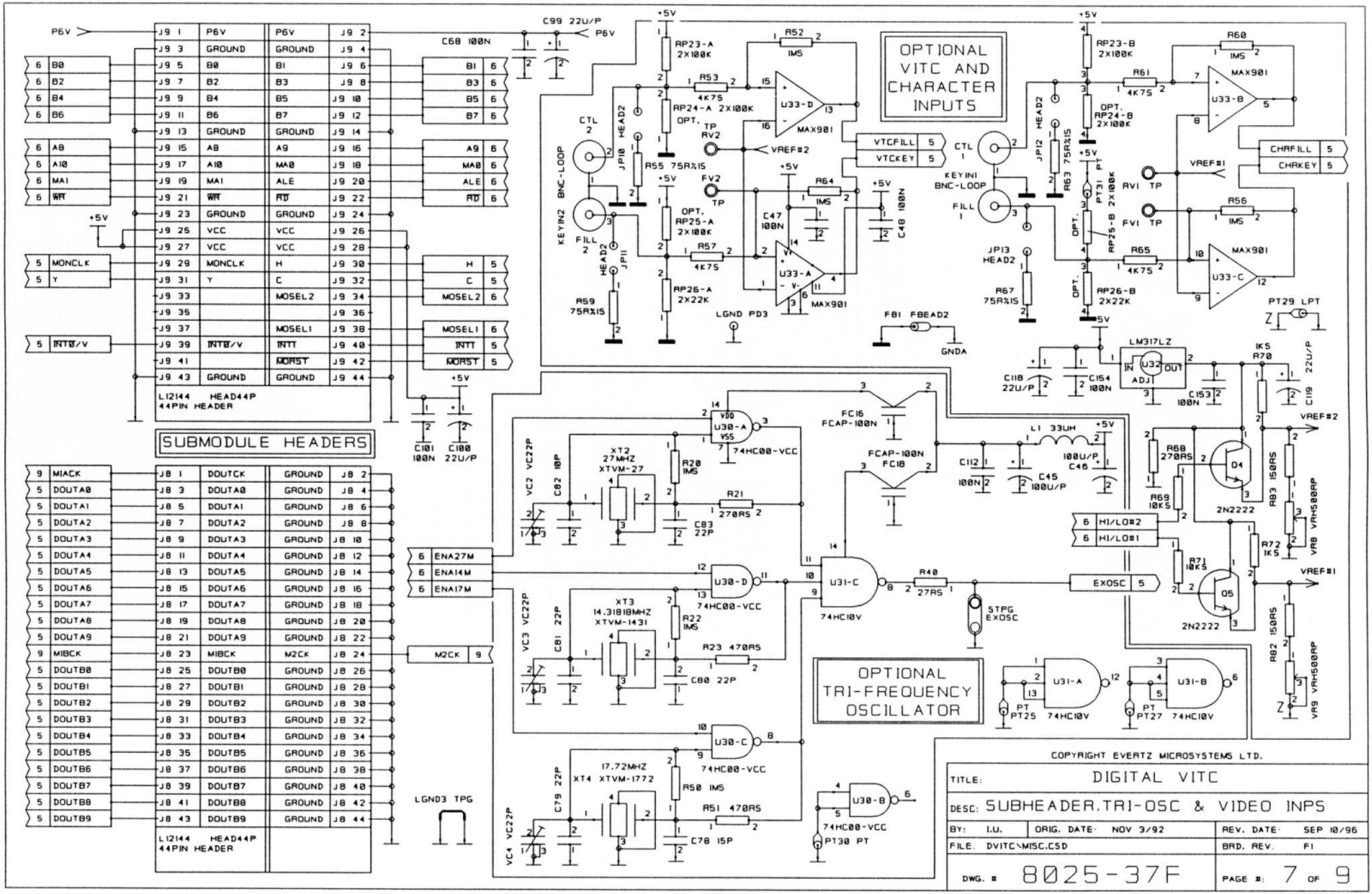
EVERTZ	BOARD: MODEL 8025 DIGITAL KEYER	TITLE: 8010 AND 8950 COMPONENT LAYOUT	DWN BY: I.U.	REV: F1
		DATE: OCT 16/96	DWG NO.: 8025-83F1	

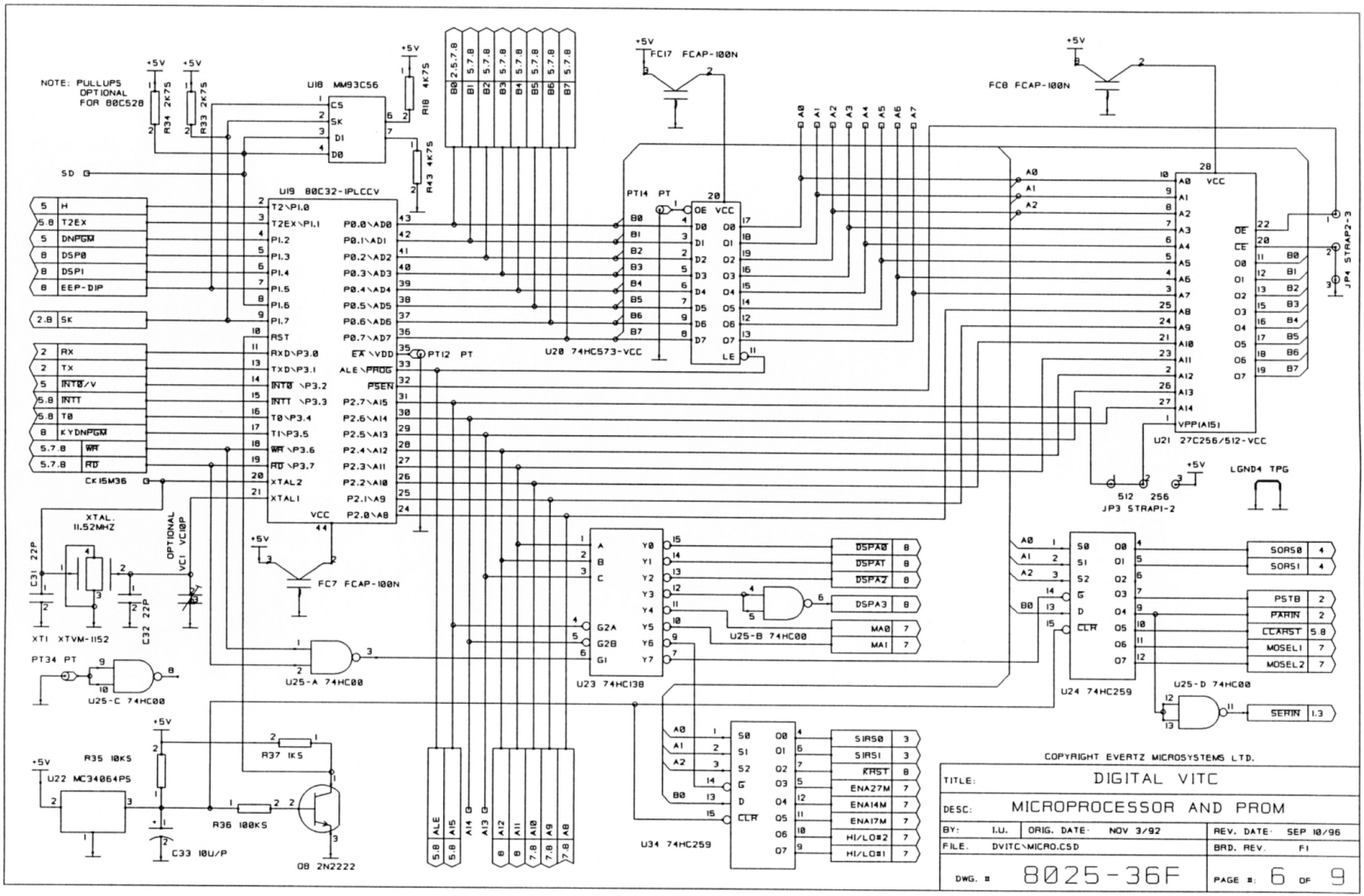


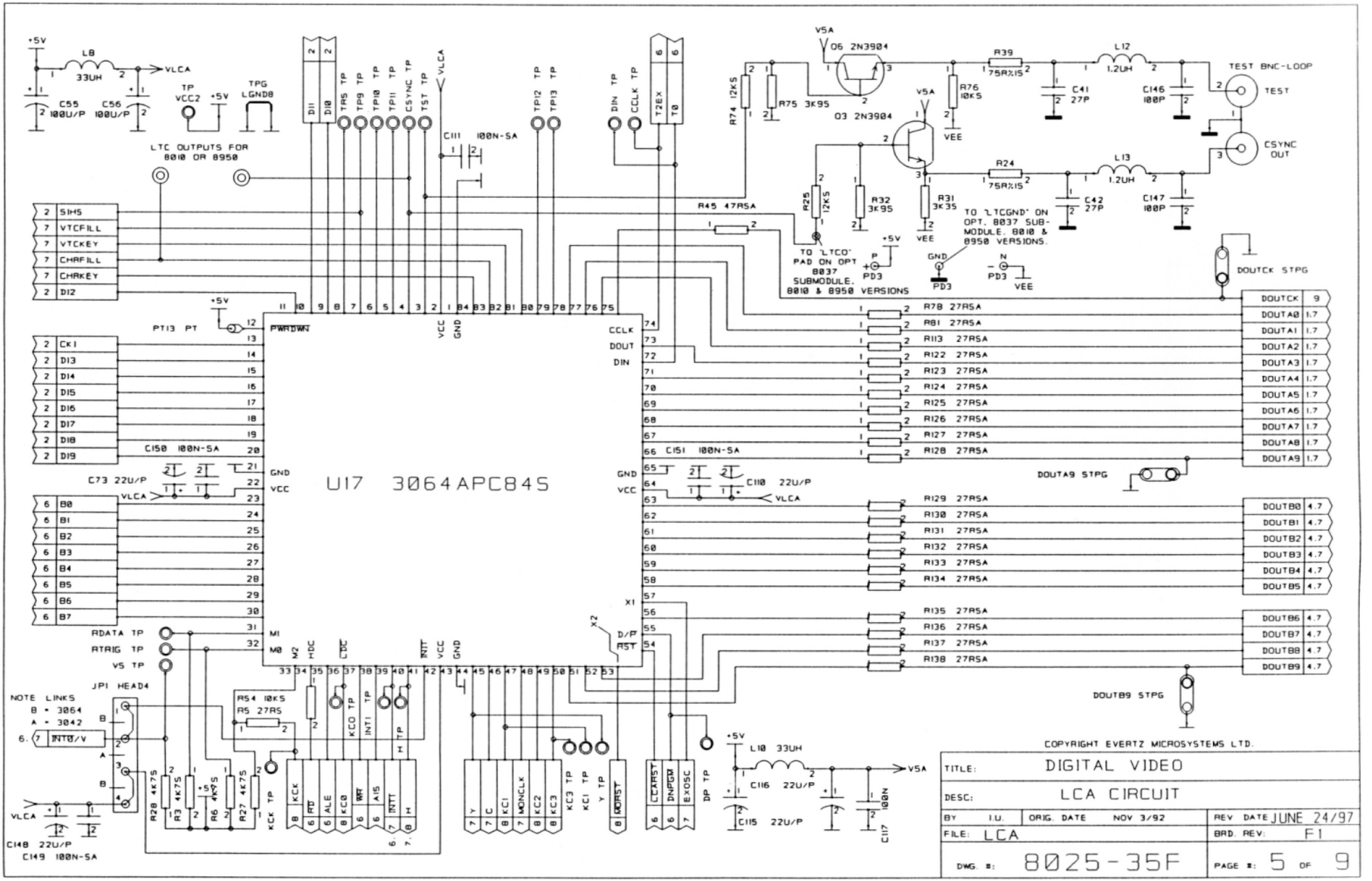
TITLE: DIGITAL VITC			
DESC: CLOCK BUFFER/MULIPLIER CIRCUIT			
BY: I.U.	ORIG. DATE: NOV 15/92		REV. DATE: SEP 10/96
FILE: DVITC\CLOCK.CSD			BRD. REV. F1
DWG. #: 8025-39F			PAGE #: 9 OF 9

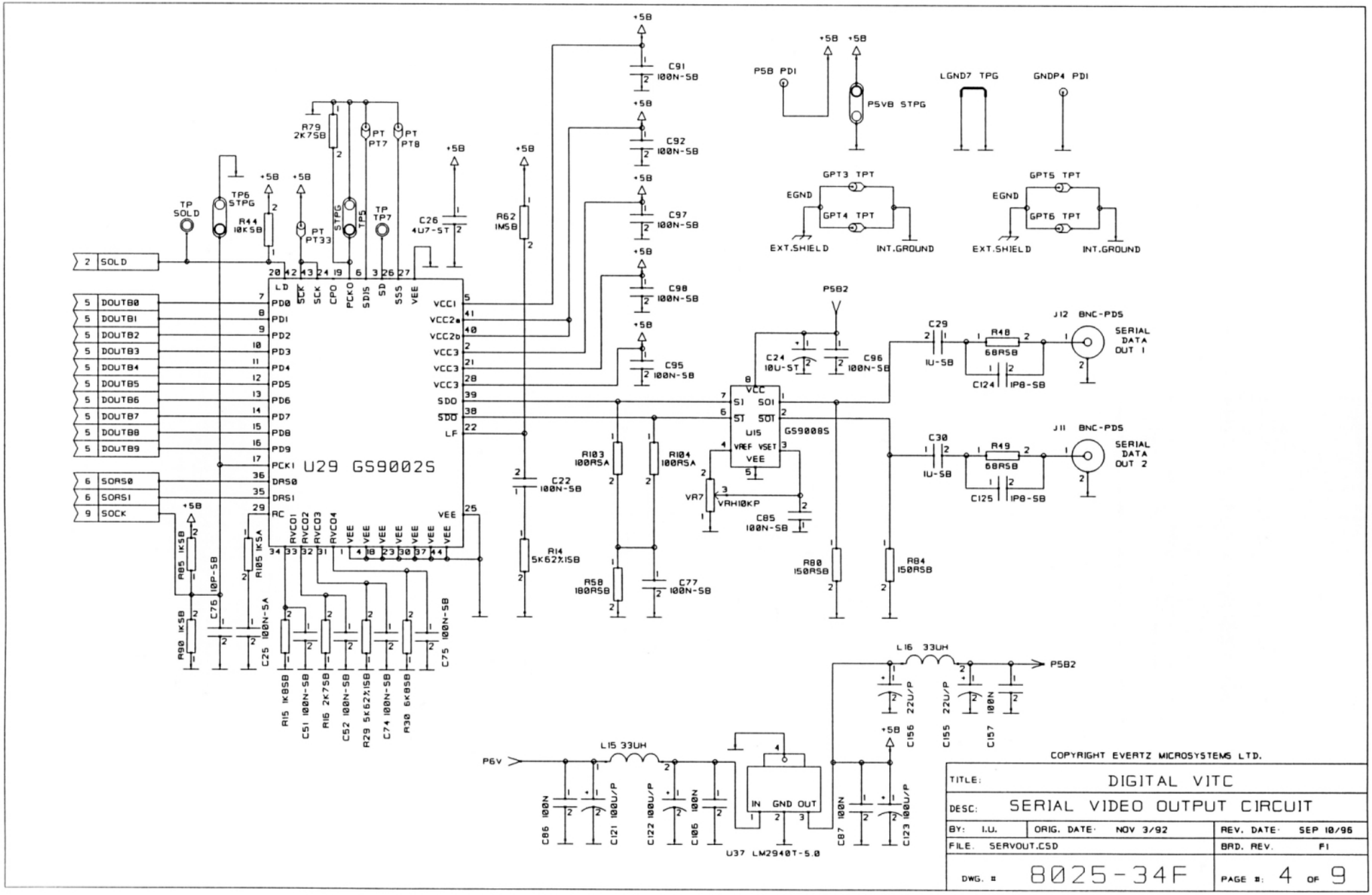


TITLE:	DIGITAL VITC		
DESC:	DIP. P/S AND DISPLAY HEADER		
BY: I.U.	ORIG. DATE: NOV 15/92		REV. DATE: SEP 10/96
FILE: DVITC\HEADER.CSD			BRD. REV. F1
DWG. #: 8025-38F			PAGE #: 8 OF 9


OPTIONAL VITC AND CHARACTER INPUTS
SUBMODULE HEADERS
OPTIONAL TRI-FREQUENCY OSCILLATOR
L12144 HEAD44P 44PIN HEADER
LGND3 TPG
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE: DIGITAL VITC
DESC: SUBHEADER,TRI-OSC & VIDEO INPS
BY: I.U.
ORIG. DATE: NOV 3/92
REV. DATE: SEP 10/96
FILE: DVITC\MISC.CSD
BRD. REV. F1
DWG. # 8025-37F
PAGE #: 7 OF 9


NOTE: PULLUPS OPTIONAL FOR 80C528
U18 MM93C56
U19 80C32-1PLCC
U20 74HC573-VCC
U21 27C256/512-VCC
U23 74HC138
U24 74HC259
U34 74HC259
U25-A 74HC00
U25-B 74HC00
U25-C 74HC00
U25-D 74HC00
FC7 FCAP-100N
FC8 FCAP-100N
FC17 FCAP-100N
XTAL. 11.52MHZ
XT1 XTVM-1152
Q8 2N2222
U22 MC34064P5
JP3 STRAP1-2
JP4 STRAP2-3
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE: DIGITAL VITC
DESC: MICROPROCESSOR AND PROM
BY: I.U. ORIG. DATE: NOV 3/92 REV. DATE: SEP 10/96
FILE: DVITC\MICRO.CSD BRD. REV. F1
DWG. # 8025-36F PAGE #: 6 OF 9


U17 3064APC84S
LTC OUTPUTS FOR 8010 OR 8950
TO 'LTCO' PAD ON OPT 8037 SUBMODULE. 8010 & 8950 VERSIONS
TO 'LTCGND' ON OPT. 8037 SUB-MODULE. 8010 & 8950 VERSIONS.
TEST BNC-LOOP
TEST
CSYNC OUT
DOUTCK STPG
DOUTA9 STPG
DOUTB9 STPG
NOTE LINKS
B = 3064
A = 3042
JP1 HEAD4
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE: DIGITAL VIDEO
DESC: LCA CIRCUIT
BY I.U. ORIG. DATE NOV 3/92
REV DATE JUNE 24/97
FILE: LCA
BRD. REV: F1
DWG. #: 8025-35F
PAGE #: 5 OF 9



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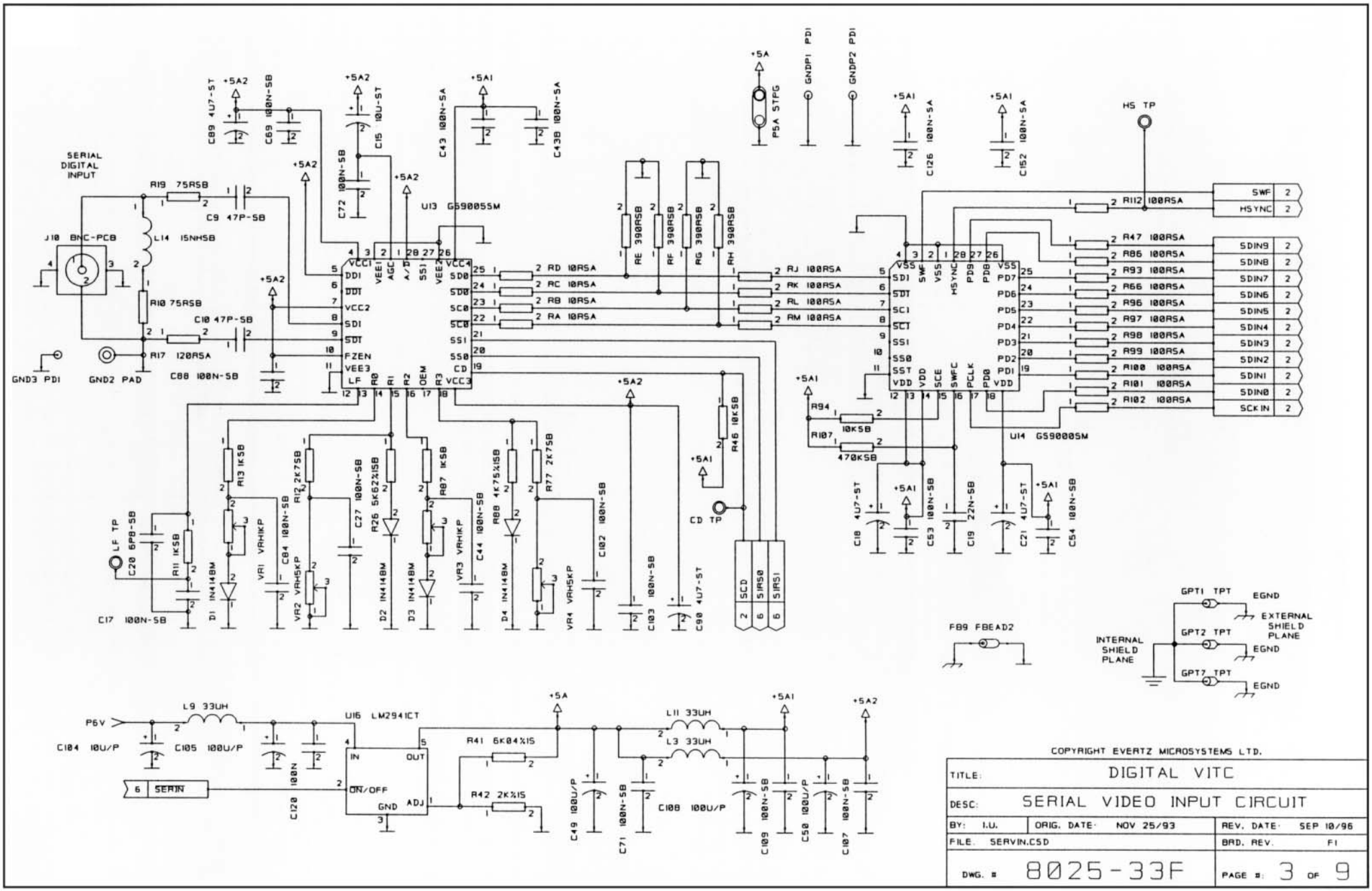
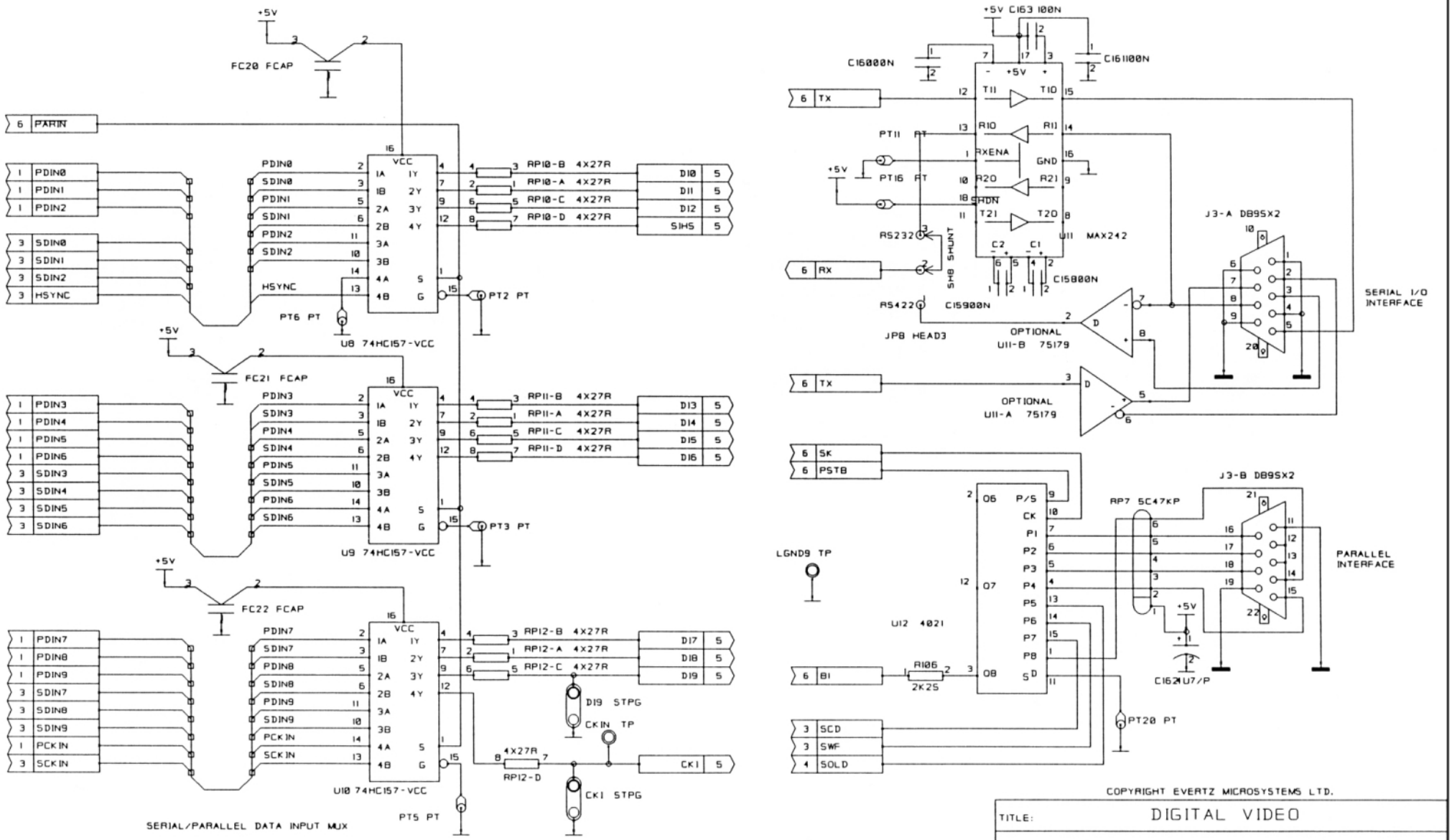
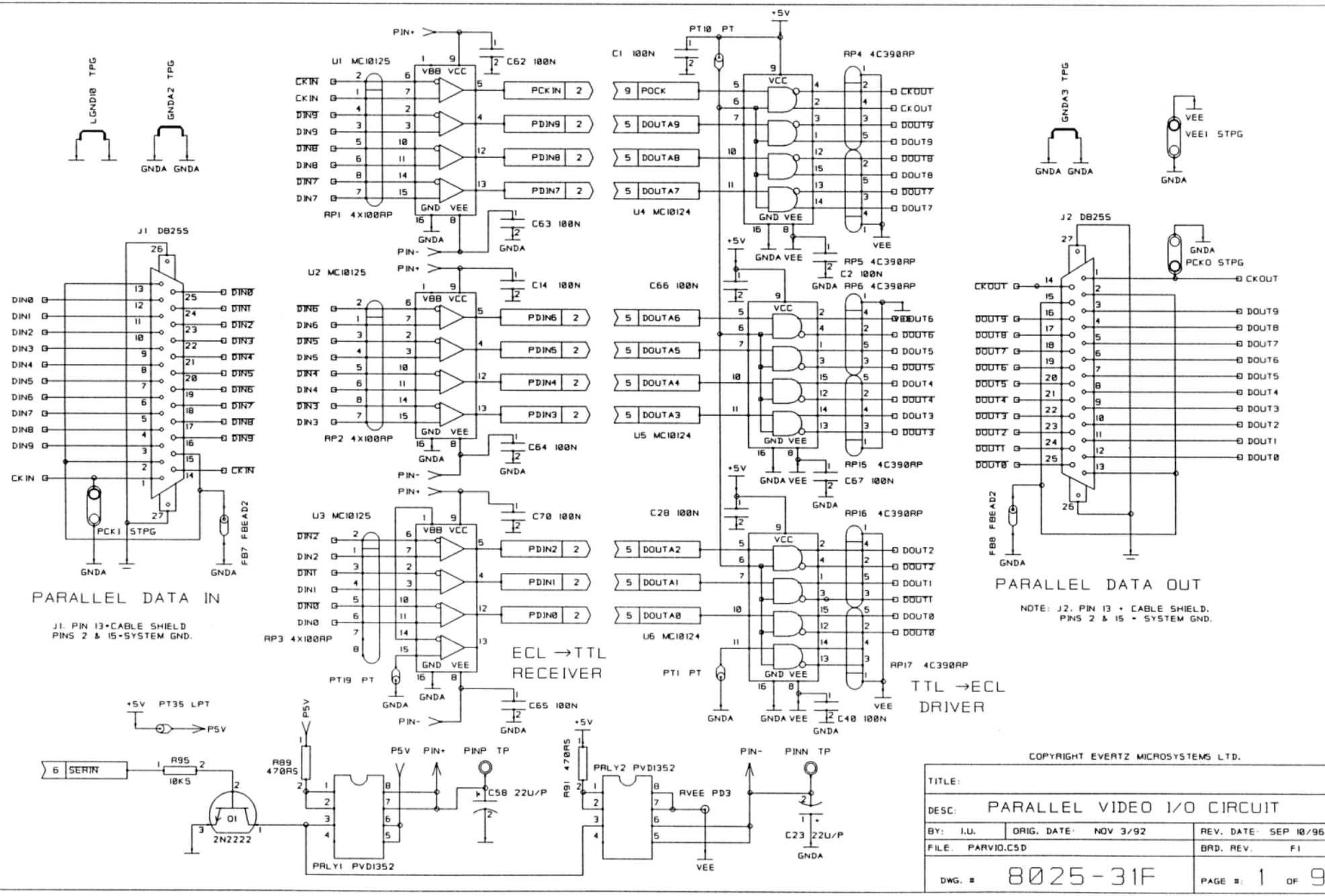
TITLE:	DIGITAL VITC		
DESC:	SERIAL VIDEO OUTPUT CIRCUIT		
BY: I.U.	ORIG. DATE: NOV 3/92		REV. DATE: SEP 10/96
FILE: SERVOUT.CSD			BRD. REV. F1
DWG. #: 8025-34F			PAGE #: 4 OF 9



TITLE:	DIGITAL VITC		
DESC:	SERIAL VIDEO INPUT CIRCUIT		
BY: I.U.	ORIG. DATE: NOV 25/93		REV. DATE: SEP 10/96
FILE: SERVIN.C5D			BRD. REV. F1
DWG. #: 8025-33F			PAGE #: 3 OF 9



TITLE:	DIGITAL VIDEO		
DESC:	SER/PAR MUX & I/O INTERFACE		
BY: I.U.	ORIG. DATE: NOV 3/92		REV. DATE: SEP 10/96
FILE: SPIN1.CSD			BRD. REV. F1
DWG. # 8025-32F			PAGE #: 2 OF 9



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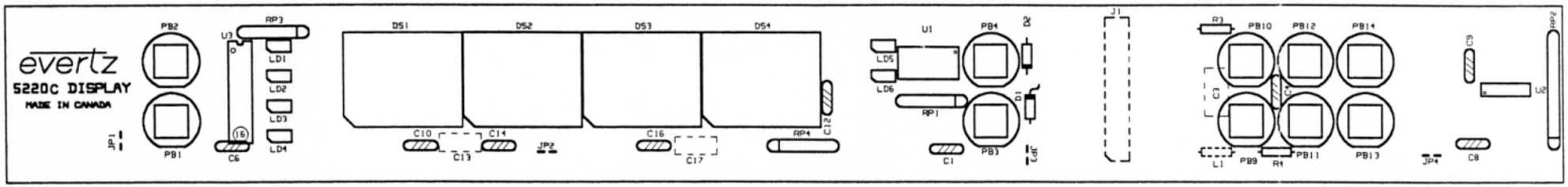
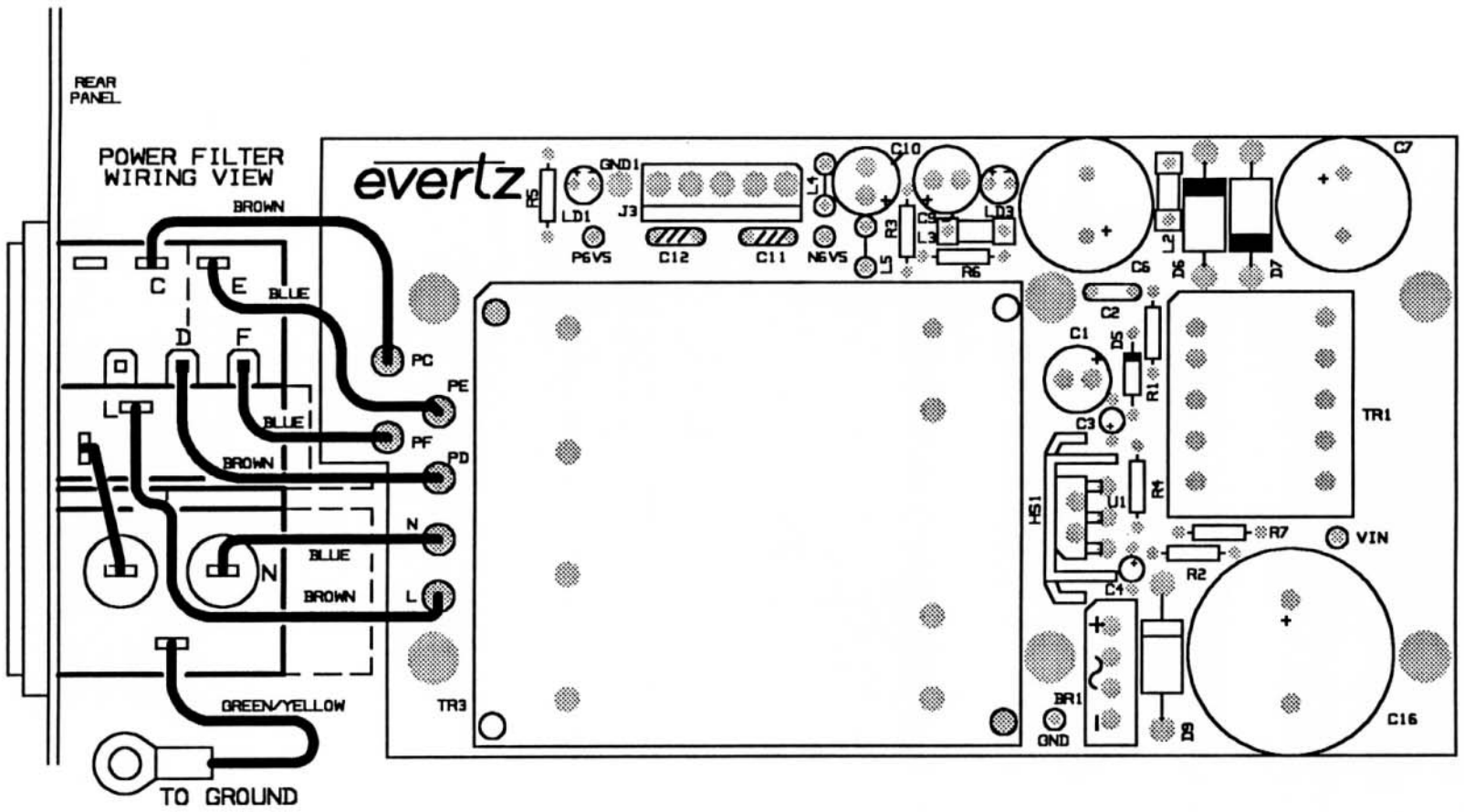
TITLE:		
DESC:	PARALLEL VIDEO I/O CIRCUIT	
BY: I.U.	ORIG. DATE: NOV 3/92	REV. DATE: SEP 10/96
FILE: PARV10.CSD		BRD. REV. F1
DWG. #: 8025-31F		PAGE #: 1 OF 9



EVERTZ MICROSYSTEMS LTD	ORIG DATE : NOV 24/93	REV. DATE : FEB 28/96
TITLE: 8950 DISPLAY COMPONENT LAYOUT	BRD REV. C	DWG NO. : 5220-89C



EVERTZ MOCROSYSTEMS LTD	ORIG DATE : FEB 26/93	REV. DATE :	MAY 6/94
TITLE: 8102 COMPONENT LAYOUT	BRD REV : A	DWG NO. :	8102-80A