MODELS S621, S621-LTR

VITC GENERATOR/TRANSLATOR
WITH SOURCE IDENT

INSTRUCTION MANUAL

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INFORMATION TO USERS IN EUROPE

NOTE

CISPR 22 CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to the European Union EMC directive. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

INFORMATION TO USERS IN THE U.S.A.

NOTE

FCC CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

WARNING

Changes or Modifications not expressly approved by Evertz Microsystems Ltd. could void the user's authority to operate the equipment.

Use of unshielded plugs or cables may cause radiation interference. Properly shielded interface cables with the shield connected to the chassis ground of the device must be used.

REVISION HISTORY

REVISION	DESCRIPTION	DATE
1.0	Original issue	9/89

TABLE OF CONTENTS

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1. MODEL S621 VITC GENERATOR/TRANSLATOR

This microcontroller based module is a full featured vertical interval time code (VITC) generator. Easily accessible DIP switches are used to preset parameters such as VITC line numbers, 2,4, or 8 field locking, drop frame and source ID code. An optional LTC reader sub-module upgrades the S621 to an LTC to VITC translator with sophisicated error bypass functions. Remote control inputs permit generator reset/start, user bit transfer and tally control. (used for ON AIR indication in source ID applications) In addition, 6 uncommitted inputs are available for remote control of downstream equipment via the video path. Figure 1-1 shows a functional block diagram of the S621 module.

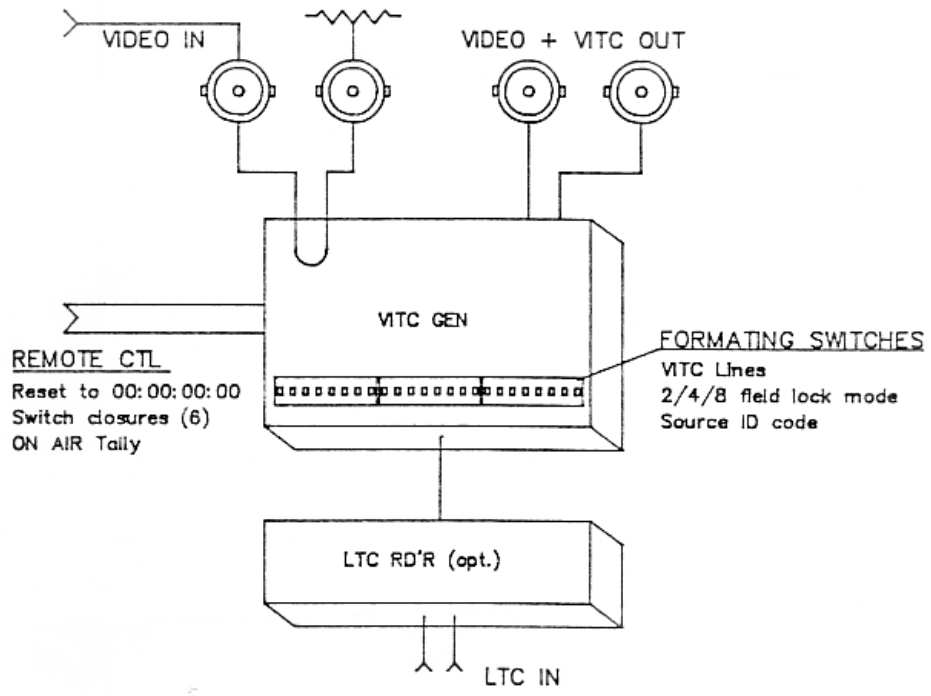


Figure 1-1: S621 Block Diagram

1.1. INSTALLATION

All connections to the S621 are made on the rear panel. During set-up it may be necessary to remove the module from its enclosure to set up DIP Switches. Each module is held in the chassis by two quarter turn screws to allow for easy removal of the module. Care must be taken in aligning the module in the card guides and making sure the board connector is properly seated.

1.1.1. Power Requirements

Power requirements are 12 volts DC

1.1.2. Video Input and Output

The generator must be locked to a stable 1 volt p-p composite video source applied to the video input loop. The S621 inserts VITC on the same video used to provide frame synchronization to the generator. The internal sync separator has a high impedance input tapped off the loop through, therefore, the input must be terminated with 75 ohms at the end of the line. When the S621 senses a stable video input, the µP OK LED will be on. When no video is present, it will be flashing on and off. Program video with VITC inserted on the selected lines is available on two separate outputs.

1.1.3. LTC Input and Output

A loop through consisting of two 1/4" stereo phone jacks is provided as an input to the LTC reader. When using an unbalanced input to the reader, the signal should be applied to the tip of the phone plug. Normally, the unused input (ring) should be connected to ground (sleeve). Code should be applied to the INP connector. The OUTP connector is provided as a convenient way of daisy chaining several modules together.

1.1.4. Parallel Remote Control

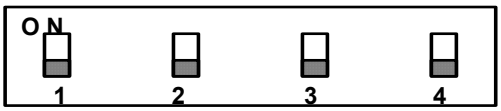
A nine pin subminiature 'D' connector is provided on the rear panel, for remote control of the generator functions. The inputs are activated by a connection to ground. The pin connections are described below:

Pin	Name	Description
5	REM 1	Remote control input #1
9	REM 2	Remote control input #2
4	REM 3	Remote control input #3
8	REM 4	Remote control input #4
3	REM 5	Remote control input #5
7	REM 6	Remote control input #6
2	REM 7	ON AIR Tally input
6	GND	Ground
1	REM 8	Generator Start/Reset

1.2. LINE SELECTION

Switch positions 1 to 4, and 5 to 8 of the rightmost DIP switch (SW 3) select the video line numbers for placement of the first and second lines of VITC respectively. It is recommended that two non-adjacent lines be used, however, adjacent lines and a single line (selected when both line numbers

are the same) are permitted. Figure 1-2 shows the switch settings and the corresponding video line numbers.



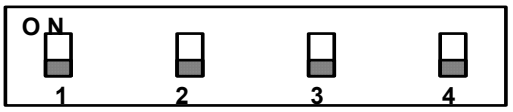
(5)	(6)	(7)	(8)	VITC LINES
Off	Off	Off	Off	6
Off	Off	Off	On	7
Off	Off	On	Off	8
Off	Off	On	On	9
Off	On	Off	Off	10
Off	On	Off	On	11
Off	On	On	Off	12
Off	On	On	On	13
On	Off	Off	Off	14
On	Off	Off	On	15
On	Off	On	Off	16
On	Off	On	On	17
On	On	Off	Off	18
On	On	Off	On	19
On	On	On	Off	20
On	On	On	On	21

Figure 1-2: Line Selection

On NTSC units, If the switches are set for lines 6-10, then line 10 will be selected. If the switches are set for line 21, then line 20 will be selected.

1.3. SOURCE IDENTIFICATION ENCODING

The two leftmost 8 position DIP switches provide an easy method of presetting unique source identification codes into the user bits. Each 8 position switch is configured as a pair of 4 position switches, each one encoding a bcd value as shown below.



(5)	(6)	(7)	(8)	BCD VALUE
Off	Off	Off	Off	0
Off	Off	Off	On	1
Off	Off	On	Off	2
Off	Off	On	On	3
Off	On	Off	Off	4
Off	On	Off	On	5
Off	On	On	Off	6
Off	On	On	On	7
On	Off	Off	Off	8
On	Off	Off	On	9

Figure 1-3: BCD Encoding of DIP Switch

1.3.1. Message Number Switch

Positions 2 to 4 and 5 to 8 of the leftmost DIP switch (SW 1) provide BCD encoding for the 10x and 1 x digit of the message number respectively. Of the 79 possible messages, only number 0 through 63 are valid. Any invalid switch settings will be set to the maximum message number (63). Figure 1.4 below shows the standard messages, as they are decoded by the VITC reader and their respective codes. Custom messages may be installed in the readers at the factory by a PROM change.

Position 1 of the message number switch selects whether the user bits from the optional LTC reader or source ID user bits will be inserted into the VITC. Remote control input #8 overrides the setting of the position 1 switch. When it is grounded it reverses the setting of the position 1 switch. When the LTC reader option is not fitted, source ID user bits are always inserted. In this case, position 1 switch is used for the generator mode (see section 1.5).

MESSAGE	CODE	MESSAGE	CODE
SPARE	00	NET	32
JAN	01	OB	33
FEB	02	PRES	34
MAR	03	REM	35
APR	04	SAT	36
MAY	05	SLID	37
JUN	06	STL	38
JUL	07	STUD	39
AUG	08	TC	40
SEP	09	TEST	41
OCT	10	TV	42
NOV	11	VCR	43
DEC	12	VITC	44
AIR	13	VT	45
AUX	14	VTR	46
BARS	15	SPARE	47
BAY	16	SPARE	48
BLK	17	SPARE	49
BVU	18	SPARE	50
CAM	19	SPARE	51
CAP	20	SPARE	52
CGEN	21	SPARE	53
CLK	22	SPARE	54
CRT	23	SPARE	55
DUB	24	SPARE	56
ECM	25	SPARE	57
EDIT	26	SPARE	58
ENG	27	SPARE	59
FILM	28	SPARE	60
LINE	29	SPARE	61
MCR	30	SPARE	62
MON	31	SPARE	63

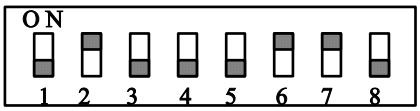
Figure 1-4: Message Select Codes

1.3.2. Source Number Switch

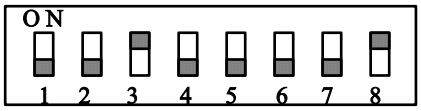
Positions 1 to 4 and 5 to 8 of the centre DIP switch (SW 2) provide BCD encoding for the 10x and 1 x digits of the source number from 00 to 99 respectively. An example of proper switch settings follows.

For source identification "VTR 21" set up the switches as shown:

MESSAGE #: 46



SOURCE #: 21



1.4. GENERATOR RUN FUNCTIONS

When the LTC reader option is not fitted, the S621 module may be used as a stand alone VITC generator with source ID. On power up, VITC from the S621 contains only source identification user bits, (i.e. the time bits are all set to zero). A special code is inserted into the user bits that turns off the time display on any decoder module, so that only the source ID is displayed.

Remote control input #8 starts the generator running from 00:00:00:00 each time it is grounded. When the time is running, a different source ID lead in code is used, enabling simultaneous time and user bit/source ID display on the decoder. The generator is properly colour framed to the input video when the mode select shorting jumper is installed on the CF side of header J1. (located at the extreme front of the module) Non colour frame mode is used when the jumper is placed on the NCF side of header J1. On NTSC units, position 1 of switch SW1 selects drop frame when set to the ON position.

When the LTC reader option is fitted, the internal generator always runs slaved to the incoming code. Position 1 of switch SW1 in conjunction with remote control input #8 configures whether the user bits will be transferred from the LTC reader or whether Source ID user bits will be used. The table below shows the four combinations possible:

SW1	**REMOTE**	
Position 1	**INPUT**	**USER BITS**
On	Open	From LTC
On	Grounded	Source ID
Off	Open	Source ID
Off	Grounded	From LTC

1.5. REMOTE CONTROL INPUTS

Remote control inputs 1 to 7 are encoded directly into the 'hours' byte of source ID user bits. When an input is closed to ground, a '1' is encoded, otherwise a '0' is encoded. When the user bits from the LTC reader are being transferred to the generator, remote control inputs 1 to 7 have no effect.

Remote input #7 has a special significance to the source ID decoder. It may be connected to the tally output of your routing switcher and will be decoded as an 'ON AIR' tally on the monitor output.

Remote input #8 is used to start/reset the generator to 00:00:00:00 when the LTC reader option is not fitted. When the LTC reader is fitted, it is used in conjunction with position 1 of switch SW1 to configure whether the user bits will be transferred from the LTC reader or whether Source ID user bits will be used.

1.6. TECHNICAL DESCRIPTION

The S621 generator is a microcontroller based module functionally divided into the following hardware subsystems:

1. Microcontroller & I/O
2. Sync Separator/Video processing
3. VITC generator logic
4. High speed LTC Reader

The microcontroller and video processing circuits are contained on the main circuit card (6210). The LTC reader circuitry is optional and is contained on a separate sub-module (6211) which plugs into the main module. Video input buffers and all input/output connectors are contained on a separate I/O module, (6031) which the main module plugs into. The relevant schematic drawings are shown in brackets for each section of the circuit.

1.6.1. Microcontroller (6210-32)

At the heart of the S621 reader module is a 8749 microcontroller, (MCU) U4. Its two 8 bit bi-directional ports and 8 bit bus provide peripheral interfacing to the rest of the circuits. Program memory and scratch pad and data RAM are provided internally by the MCU. An onboard oscillator, also part of the MCU, is crystal controlled. Its' 10.08 MHz is internally divided by 15 resulting in a processor operating frequency of 672 KHz.

The remote control inputs are latched by U6 and read directly by the MCU. Switches SW1 to SW3 are scanned by the MCU, and their data is fed directly onto the bus via isolating diodes U1 to U3 respectively.

1.6.2. Video Processing (6210-30)

Composite video, buffered on the separate I/O module, and on the main PCB by U10d and U10c, is AC coupled into U8b. Immediately following each horizontal sync pulse, a sample pulse is generated at U8c which allows U8a to compare the actual DC level of the video to ground potential. If they are not equal, U8a generates an error signal which adjusts the bias point of U10d thus ensuring proper operation of the video keyer with varying video and sync levels. Comparator U11 switches when the negative sync tip goes below its half amplitude point, producing composite SYNC. Composite SYNC is integrated by U7d to derive vertical sync (VSYNC) which interrupts the MCU at U4 pin 6.

The VITC keyer is controlled by a pair of opposite polarity controls, (KY1) generated by the VITC generator logic. KY1 switches U13d on and U13c off for program video, and vice versa for VITC. When U13c is on, VITC data is added to the black level of the video.

To calibrate the VITC keyer, connect colour bars from your sync generator to the Video input loop, of the S621, and to channel A of your oscilloscope, and terminate it. Connect the VITC output to channel B of your scope and terminate it. Adjust the **GAIN** trimpot (VR 2) so that the output amplitude matches the input. Adjust the **VITC LEVEL** trimpot (VR 4) so that the inserted VITC is approximately 550 millivolts above video black level. The frequency response is adjusted using trimmer VC 1 so that the chrominance amplitude of the inputs and outputs is the same.

1.6.3. Colour Frame Detector (6210-32)

The MCU samples VSYNC and 3/4 H derived by U5a to generate an internal frame sync. When the colour frame mode is enabled, the MCU enables the colour burst detector at line 10 for NTSC and line 6 for PAL. U16 generates a burst sample window which clocks U15a on for positive going burst phase on the sampled line. The MCU reads the state of U15a and resets the colour frame detector until the next frame.

Re-calibration of the colour frame detector is accomplished by adjusting **CFP ADJ** (VR 3) The generator input must be connected to an RS-170-A (8 field PAL) video source and properly terminated. The unit must also be set up to operate in the colour frame mode. This is accomplished by placing the shorting jumper on header J1 in the 'CF' position.

You will need a sync pulse generator with a colour field #1 identification pulse output, and a dual channel oscilloscope to perform the calibration.

1. Display the colour field #1 ID pulse from your sync generator on channel A of your oscilloscope. Set up the time base to show two pulses.

2. Connect channel B of your scope to U4 pin 1.

3. Position VR 3 near the centre of its range so that a pulse appears on channel B two frames before the second pulse of channel A. (See figure 1-5 below) Continue adjusting VR 3 clockwise until the pulse disappears. Mark the position of VR 3 with a pencil. Adjust VR 3 counter clockwise until the pulse reappears and disappears again. Mark the position of VR3 with a pencil.

4. Position VR 3 halfway between the pencil marks. The µP OK LED should be ON.

1.6.4. VITC Generator Logic

The VITC bit rate is generated by a crystal controlled oscillator consisting of U21e and associated components. The oscillator output is **FREQ** test point. The frequency of 14.31818 MHz for NTSC, or 14.5 MHz for PAL is 8 times the VITC bit rate. Divider U20 is used to derive the VITC bit rate from the oscillator and to count the number of VITC bits generated per line.

Once per field, the MCU loads the VITC bit pattern into shift register U18. On the lines selected for VITC insertion, the reset to U5b is released, and a start of line signal is generated. The starting position of the VITC on the line is adjusted by the **VITC POS** trimpot (VR1). It is set at the factory such that the first bit of code is 10.5 µsec (11.5 µsec for PAL) after the leading edge of horizontal sync.

When adjusting the VITC POS trimpot, take care that the keyer enable signal KY1 does not start during the colour burst,and that it ends before the leading edge of horizontal sync for the next line.

When U5b times out, flip flop U19b is reset, turning on the VITC keyer, and enabling the clocking out of 96 bits of data from U18. The data is registered with the VITC clock at U19a, so that the bit width is not dependent on propogation delays in the shift register. The first three and last three bits are always zero, so that a 3 bit window is keyed around the VITC data. This ensures that any old VITC will be totally removed.

1.6.5. High Speed LTC Reader (6211-31)

The high speed LTC reader is optional and is contained on a separate circuit card 6211. (Refer to drawing 6211-31).

Incoming code is decoupled and amplified by U16, U15, and U14, and associated components, to provide a regenerated reader data signal at U14 pin 10. A series of timing pulses, generated by U10 and U9, are used to properly decode 0 and 1 bits from the incoming code. A constant

amplitude ramp is generated by U11 and associated components. Three quarters of the peak ramp level is used as a reference on comparator U12 to decode the data from the clock transitions. If the next code bit is a 0, then the ramp will exceed the reference before a transition occurs. If the next bit is a 1, an extra transition will occur before the ramp exceeds the reference, clocking flip flop U9b on. The LTC data is available at U9 pin 15, and is shifted through sync detector U4 and U6 into one half of shift register U3.

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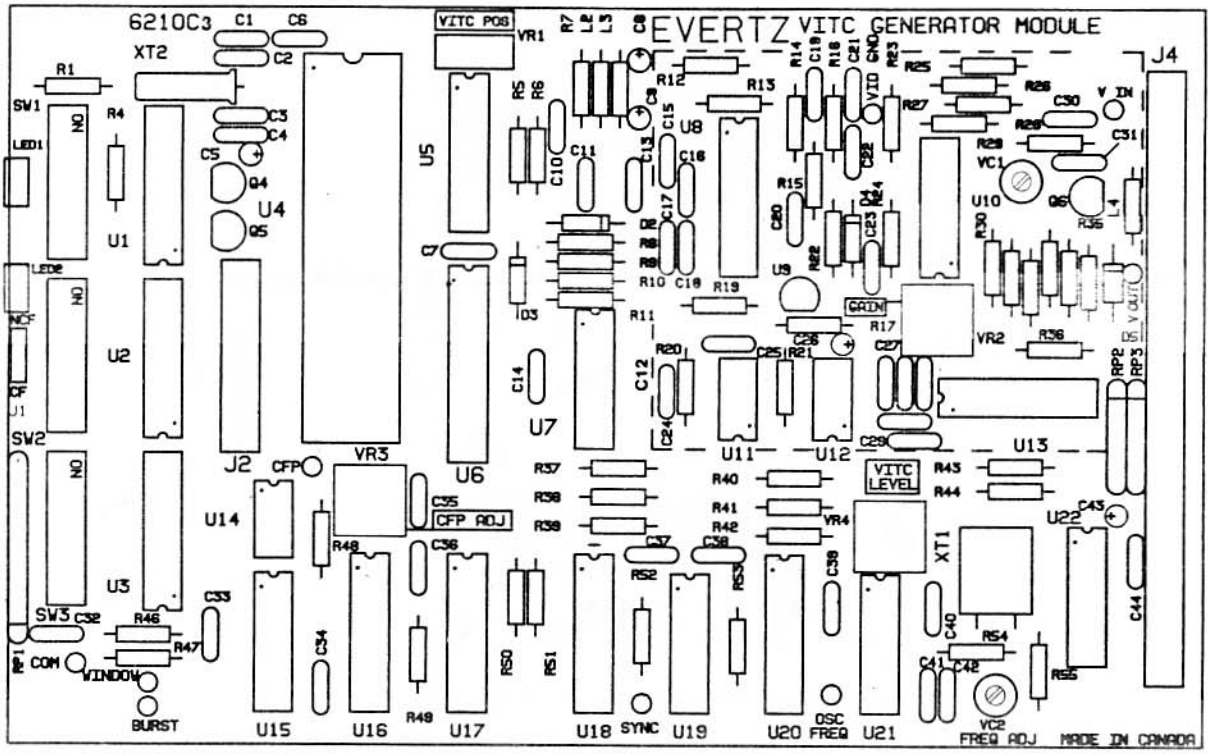
		DATE: DEC 2/85	DWN: I.U.



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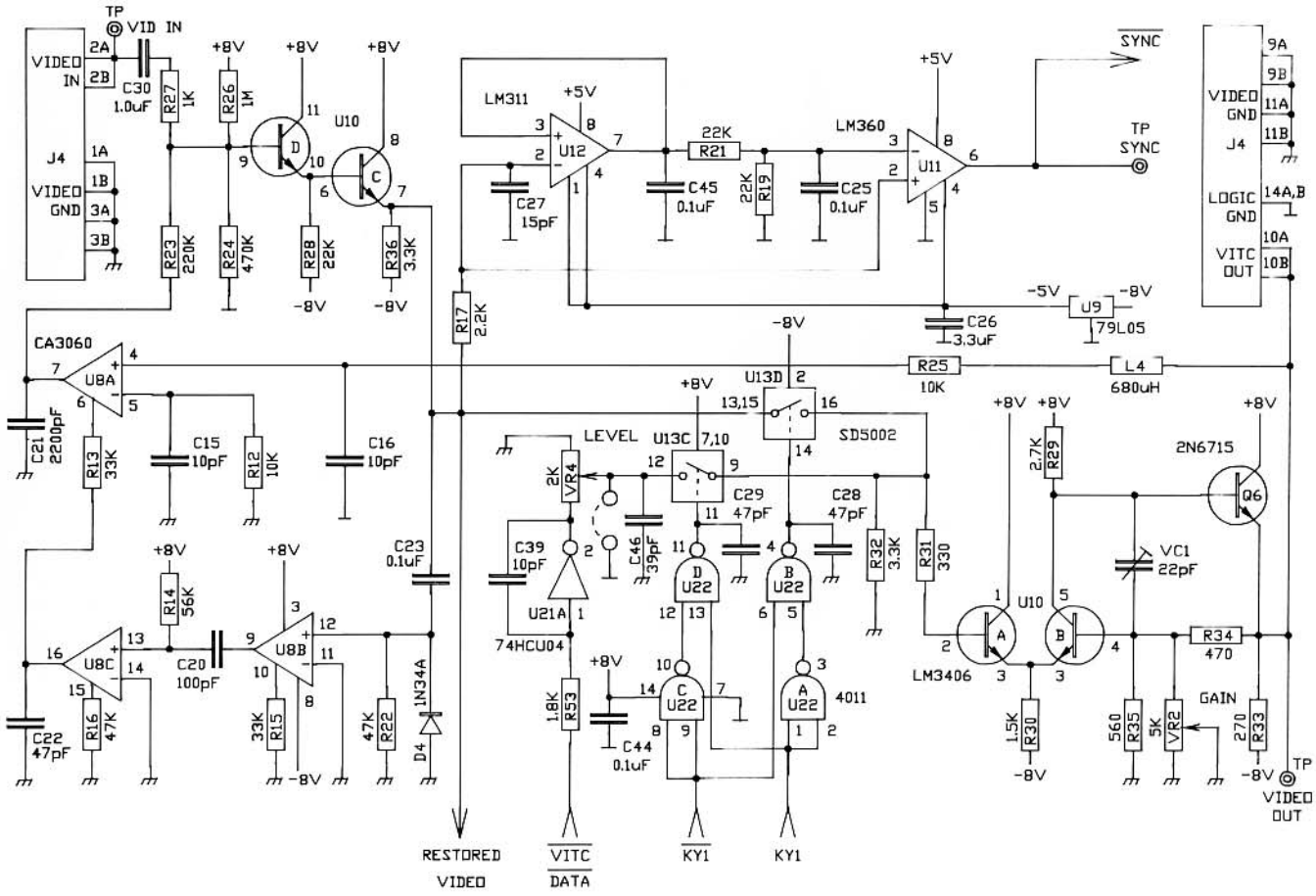

NOTE:

FOR MODEL 620, OMIT COMPONENTS VR4, R53, C39, C46, U21

INSTALL JUMPER BETWEEN PIN 12 OF U13 AND GROUND

SEE DWG # 6210-31
OR DWG # 6210-32

EVERTZ MICROSYSTEMS LTD			
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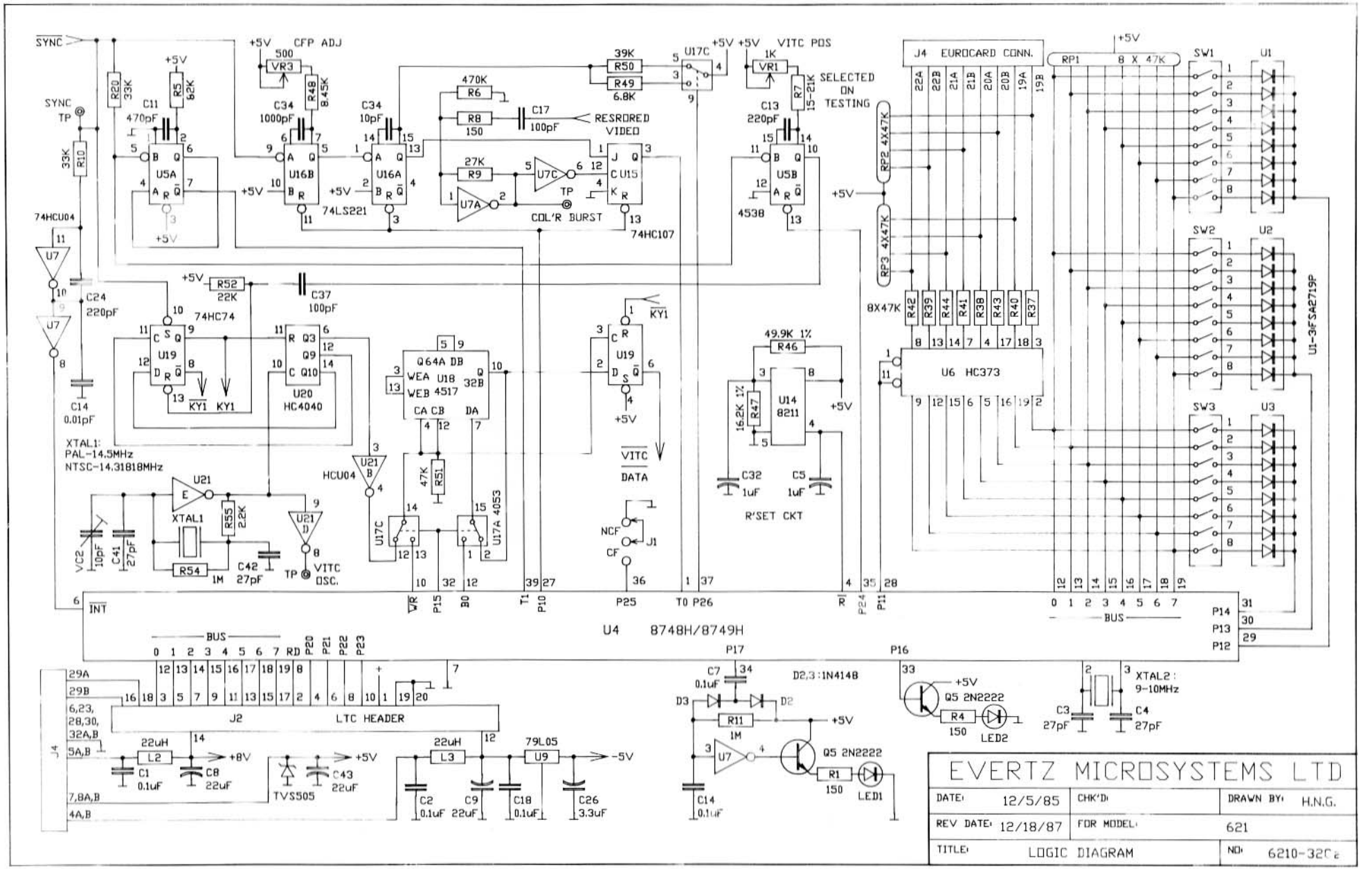

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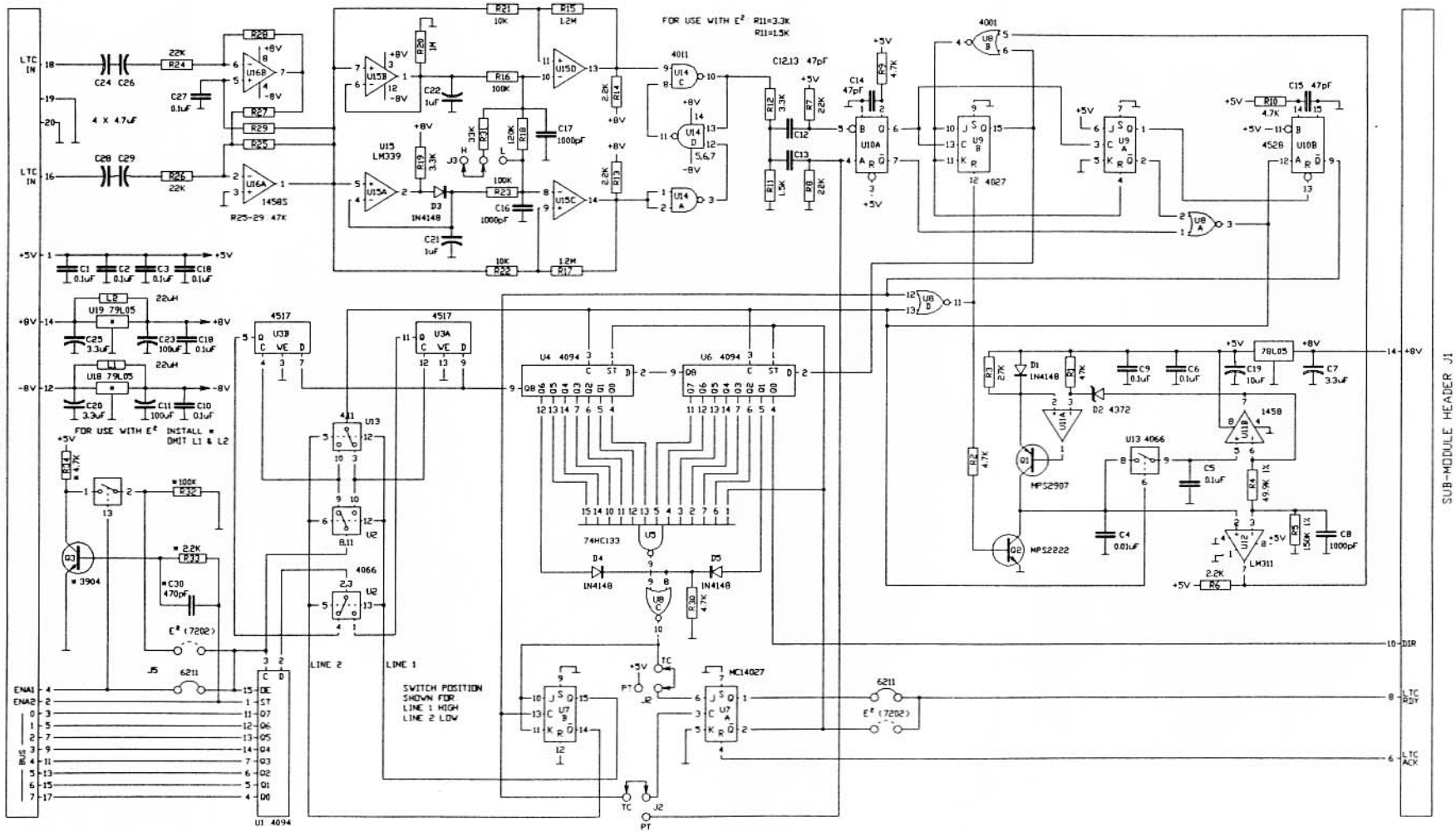

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REV DATE:	FOR MODEL: 6140, 6210, E²		
TITLE: LTC READER SUB-MODULE		NO: 6211-30E	

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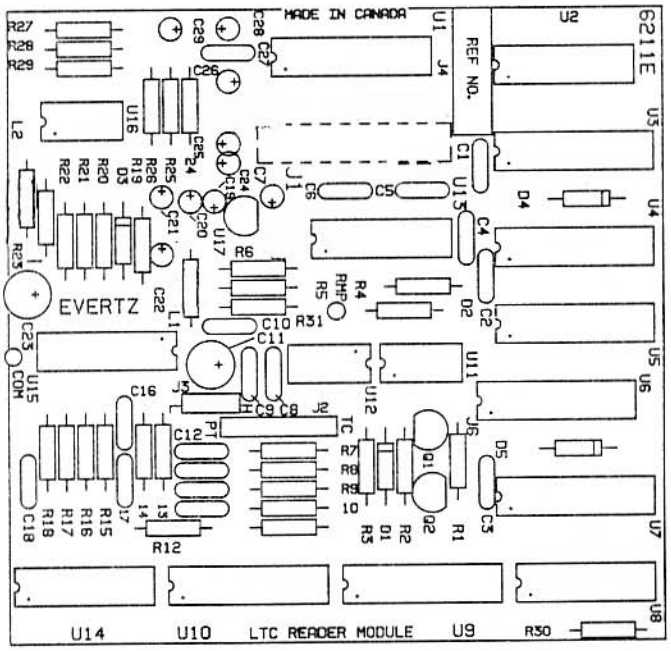
		DATE: MAY 25/88	DWN: I.U.



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