Model S622, S622-VCG

VITC Reader

INSTRUCTION MANUAL

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INFORMATION TO USERS IN EUROPE

NOTE

CISPR 22 CLASS A DIGITAL DEVICE OR PERIPHERAL

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to the European Union EMC directive. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

INFORMATION TO USERS IN THE U.S.A.

NOTE

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

WARNING

Changes or Modifications not expressly approved by Evertz Microsystems Ltd. could void the user's authority to operate the equipment.

Use of unshielded plugs or cables may cause radiation interference. Properly shielded interface cables with the shield connected to the chassis ground of the device must be used.

REVISION HISTORY

REVISION	DESCRIPTION	DATE
2.1	Original issue	01/86

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1. MODEL 622 VITC READER/TRANSLATOR

The 622 module is a vertical interval time code reader and longitudinal time code generator in one slim euro-card package containing features not found anywhere else. When used as a translator from VITC to LTC, a unique soft locking scheme assures error free play speed code regardless of speed variations of the code being read. If the VTR is bumped in and out of sync by an editor or synchronizer, the translated LTC framing follows gradually without missing a beat. The 622 reader contains all the necessary video processing circuits and therefore requires no external signals other than the video signal containing the VITC.

The 622 module has several reading modes. The first valid line of code encountered in each field will be processed in the 'AUTO' mode. This mode, invoked automatically when the optional VCG is not installed, ensures smooth reader operation from still frame to about 20 times play speed. The use of a time base corrector will extend the recovery range. Two further modes, available when the VCG option is installed, permit selective reading of one VITC line pair, when several sets of VITC data are present.

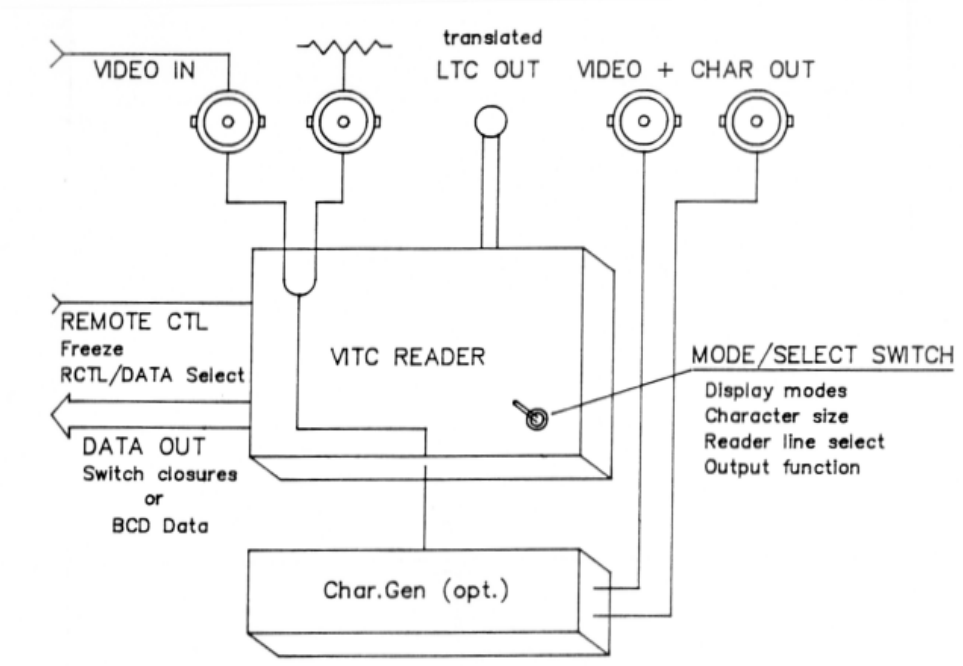

Figure 1-1: Model 622 Block Diagram

An optional video character inserter allows this unit to be used as a direct display reader. A broadcast quality keyer inserts white high resolution characters with a black background into the program video. Character size and raster position are switch selectable.

Another application is source identification. A look-up table is used to decode a special code (placed in the user bits of the VITC by a 621 encoder or other VITC generator) and display source ID messages using the optional VCG. The ID code may be “source only" for a camera (ie. CAM 1), on air status (ON AIR blinking), or source ID plus timecode for a time coded source (ie. VTR 3).

Six Buffered outputs are provided for either multiplexed parallel BCD data outputs, or grounding solid state switches used for remote machine control applications. A two position front panel switch aids in selection of the various operational modes such as VCG display characteristics, function of parallel outputs, VITC line select, etc. Formatted modes are retained in non-volatile memory even when power is removed.

1.1. INSTALLATION

All connections to the 622 VITC Reader are made using the Model 603-RD Parallel I/O module. Refer to section 2.2 for instructions on fitting the 622 and I/O modules into the rack frame.

1.1.1. Video Input and Output

The reader video with VITC recorded on it is connected to the VIDEO IN loop. The internal sync separator has a high impedance input tapped off the loop through, therefore, the input must be terminated with 75 ohms at the end of the line. The input video is also used as a reference for phasing of the LTC translator output and as an input to the optional character inserter. When video is present at the reader input the µP OK LED will be on. When no video is present, it will be flashing on and off. When VITC is being read from the input video, the VITC LED will also be on.

Program video with characters inserted is available on two separate outputs.

1.1.2. LTC Translator Output

A 1/4" stereo phone jack is provided as an output from the LTC translator. This output is play speed regenerated code from the VITC being read. When the incoming code is at normal play speed, the output code is properly synchronized to the input video. When there is no incoming VITC, the LTC output disappears.

1.1.3. CTL/DATA Pin Assignments

A nine pin subminiature 'D' connector is provided on the Model 603 Parallel I/O module, for remote control of the reader functions and BCD data/remote control outputs from the reader. The inputs are activated by a connection to ground. The pin connections are described below:

Pin	Name	Description
5	FRZ	Freeze time display input
9	RCT/DAT	remote ctl/data select input
4	OP5/STB	Address/data strobe/bit 5
8	OP6/CTS	Clear to send / output bit 6
3	OP3	Data output bit 3
7	OP4	Data output bit 4
2	OP1	Data output bit 1
6	GND	Ground
1	OP2	Data output bit 2

1.2. FORMAT FUNCTIONS

A two position toggle switch mounted on the front panel is used in conjunction with the optional video character inserter to configure the following operational modes. Each time the switch is pressed to the **MODE** position, the next mode to be formatted is selected, and an appropriate message is displayed in the top left corner of the VCG display. If you want to change that mode, press the switch to the **SELECT** position to cycle through the possible configurations. When the desired selection is displayed, release the switch to the centre position. The next mode may be selected by pressing the switch to the **MODE** position, etc. After 5 seconds with no switch action, the format display is turned off, and the selections are stored in a non-volatile memory, for recall after a power failure. The format modes are listed below in the order they occur.

When the optional VCG is not installed, the Model 622 uses AUTO reading mode. The RCTL/DATA remote control input selects the DATA/RCTL mode.

DSPLY Pressing SELECT changes the display format of the VCG display to show time, user bits (source ID or numeric), time and user bits, or no VCG display. In the absence of incoming VITC, the VCG display may be blanked (see VCG MODE below). Display mode selection should be done with a valid VITC input. When Source ID user bits are being read without running time code numbers, the time digits will not be displayed.

SIZE Pressing SELECT alternates between one of two VCG sizes.

VCG MODE Pressing SELECT alternates between one of two modes for the VCG display.

When BLANK is displayed, the character display is blanked when there is no incoming VITC on the lines it is programmed to read.

When SHOW is displayed, the character display shows the last value read after VITC is removed from the programmed lines.

When code is present, the VITC data is displayed according to the formatted DSPLY mode.

READ MODE One of three reading modes will be selected. When AUTO is displayed, the first valid line of VITC encountered in each field will be read.

When two line numbers are displayed, (ie. 12 14), only VITC recorded on the displayed lines will be read.

When two line numbers separated by an arrow are displayed, (ie. 12>14), then the first valid line of VITC encountered in the range of lines selected will be read.

Selection of individual lines or a range of lines can only be used when the incoming video with VITC is at play speed, or is time base corrected. If no VITC exists on the selected lines, the 622 reader will turn the VITC IN indicator off and blank the character display if the BLANK VCG mode is selected. If the SHOW VCG mode is selected, the last valid time read will be displayed.

LINE1 Two line numbers will be displayed, with the leftmost one blinking. Pressing SELECT will advance the blinking number. When the last permitted line is reached, the number will return to the lowest permitted number. Valid numbers are 10 to 20 for NTSC, and 6 to 21 for PAL.

LINE2 Two line numbers will be displayed, with the rightmost one blinking. Line selection is accomplished as for LINE1 above.

OUTPUT One of two modes for the parallel outputs will be selected. When DATA is displayed, the reader data is output as described in section 1.4.1. When RCTL is displayed, the outputs operate as remote control switches as described in section 1.4.2.

1.3. CHARACTER GENERATOR FUNCTIONS

When fitted with the optional VCG sub module, the Model 622 VITC reader provides a display of time or user bit information as characters keyed into the program video.

1.3.1. Character Position

The position of the reader display is selected by a 16 position rotary switch located on the side of the module. A small screwdriver can be used to position the characters to one of 15 positions on the screen. Selecting position 0 turns the characters off.

1.3.2. Background Selection

The position of the shorting jumper on header J3, (located on the VCG sub module near the position switch), determines whether characters will be keyed into a black background or not. With the jumper in the 'B' position, (closest the rear of the module), a black background will be used. When in the 'NB' position, white characters will be keyed into the video without a background.

1.3.3. Drop Frame Indication (NTSC units only)

When displaying reader time information, the colon between the seconds and frames will be replaced by a period if the data being read was recorded in the EIA drop frame mode.

1.3.4. Field Indication

When displaying the VITC time numbers, the field number sequence will be displayed to the right of the frames display. When the data being read was recorded in the non colour frame mode, the field number sequence will be 1,2,1, etc (1,2,3,4,1,etc for PAL). When the data being read was recorded in the colour frame mode, the field number sequence will be 1,2,3,4,1, etc (1,2,3,4,5,6,7,8,1,etc for PAL).

1.3.5. Time/User Bits Display

Either the time or user bits or both may be displayed. The format toggle switch is used to control the display mode. (See section 1.2 above) The colons are blanked when the user bits are being displayed. When the incoming code contains source ID user bits from a non time coded source, (i.e. the 'frames' user bits are 94), the time numbers will be automatically blanked regardless of the formatted display mode.

1.3.6. Source Identification

When reading code that has been recorded with source ID user bits, generated by one of our VITC generators, these user bits will be displayed as alpha-numeric character groups, and not their hexadecimal equivalents, when the user bit display is turned on. (See section 1.3.5 above)

1.3.7. Freeze Remote Control Input

Momentarily grounding the Freeze input (on the 9 pin CTL/DATA connector) freezes the character display. Grounding the input again restores normal display of the reader data.

1.4. PARALLEL OUTPUTS

Six transistor switches brought out to the 9 pin CTL/DATA connector are configured to operate in one of two modes. When the optional VCG is installed, the use of these outputs is configured using the mode select switch. (see section 1.2) When the VCG is not installed, the CTL/DATA remote control input on the 9 pin connector selects DATA when grounded and RCTL when left open.

The table below shows the addresses for the respective time code digits.

ADDRESS	DIGIT	ADDRESS	DIGIT
0000	1X Frm	1000	Bin Grp 1
0001	10X Frm	1001	Bin Grp 2
0010	1X Sec	1010	Bin Grp 3
0011	10X Sec	1011	Bin Grp 4
0100	1X Min	1100	Bin Grp 5
0101	10X Min	1101	Bin Grp 6
0110	1X Hrs	1110	Bin Grp 7
0111	10X Hrs	1111	Bin Grp 8

1.4.1. BCD Time/User Bit Output

When the DATA mode is formatted, parallel BCD time and user bit information is available on 6 output lines on the 9 pin connector. The data is presented in a multiplexed format as follows:

> The CTS line is brought low at the beginning of the sequence. Then a 4 bit address is presented with a positive going strobe (STB). Four bits of BCD data are then presented along with a negative going STB. This cycle is repeated for each of the 8 digits of time, followed by the 8 user bit digits. When the output sequence is complete, the CTS line returns high. The sequence of data is presented once per frame, during the last half of field 2.

Flag bits are output along with the time bits as follows:

BIT POSITION	NTSC	PAL
10 x Frm Bit 2	Drop Frame	Unassigned
10 x Frm Bit 3	Col'r Flag	Col'r Flag
10 x Sec Bit 3	Field Flag	Bin Grp Flg #1
10 x Min Bit 3	Bin Grp Flg #1	Bin Grp Flg #2
10 x Hrs Bit 2	Bin Grp Flg #2	Unassigned
10 x Hrs Bit 3	Unassigned	Field Flag

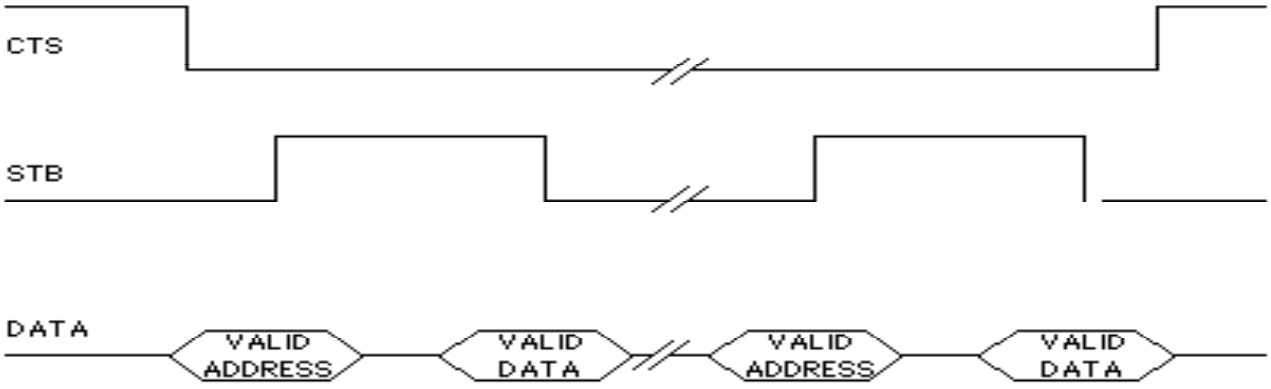

Figure 1-2: BCD Output Waveforms

1.4.2. Remote Control Switch Outputs

When the RCTL mode is formatted, the six parallel outputs are configured as open collector transistor switch outputs. When source ID user bits are being received, the 'hours' user bits, (binary groups 7 & 8), will be used to control the remote control switch outputs. When a '1' is encoded in the corresponding user bit position, the switch will be turned on, otherwise it will be off. These switches can be used to remotely control devices using the user bits in the VITC encoded in the video path, thus producing a low cost remote control system.

1.5. TECHNICAL DESCRIPTION

The 622 reader is a microcontroller based module functionally divided into the following hardware subsystems:

1. Microcontroller & I/O
2. Sync Separator
3. VITC reader logic
4. Video Character Generator

The microcontroller and VITC reader circuits are contained on the main circuit card (6220). The video character inserter circuitry is optional and is contained on a separate sub-module (6221) which plugs into the main module. Video input buffers and all input/output connectors are contained on a separate I/O module, (603) which plugs into the rear of the backplane. The relevant schematic drawings are shown in brackets for each section of the circuit.

1.5.1. Microcontroller (6220-30)

At the heart of the 622 reader module is an 8749 microcontroller, (MCU) U21. Its two 8 bit bi-directional ports and 8 bit bus provide peripheral interfacing to the rest of the circuits. Program memory and scratch pad and data RAM are provided internally by the MCU.

An onboard oscillator, also part of the MCU, is crystal controlled. Its' 10.0699 MHz (10.08 MHz for PAL) is internally divided by 15 resulting in a processor operating frequency of approximately 672 KHz. The time code output for the LTC translator is generated internally in the MCU, and is brought out on port line P24. The code edges are registered with the MCU clock at U22a, and shaped to the correct rise and fall times by U23.

1.5.2. Sync Separator (6220-31)

Reader composite video with VITC, buffered on the separate I/O module, and on the main PCB by Q5 and Q4, is AC coupled into U20b. Immediately following each horizontal sync pulse, a sample pulse is generated at U20c which allows U20a to compare the actual DC level of the video to ground potential. If they are not equal, U20a generates an error signal which adjusts the bias point of Q5 thus ensuring proper operation of the video keyer with varying video and sync levels. DC restored video is fed to the VCG sub module header J1 & J2.

The output of U20b is buffered by U7b producing composite SYNC. Composite SYNC is integrated by U16a to derive vertical sync (VSYNC) which interrupts the MCU at U21 pin 6. A field 2 pulse is generated by U14a and U15 and is provided to the MCU to correctly frame the LTC code output.

1.5.3. VITC Reader (6220-31)

Composite video is fed to comparator U2, which recovers VITC data from the DC restored video. U1 and associated components provide a reference level to U2, of approximately one half the peak VITC level, to ensure proper extraction of the VITC data regardless of the video level.

At VSYNC, the MCU releases the reset to U6a, enabling the VITC reader circuitry. Switch U4d is closed, clocking the VITC line enable bit pattern from U13, enabling flip flop U6b only for the selected lines. The first VITC data bit turns on U6b which releases the reset to CRC detector U11 and U9.

A crystal controlled oscillator consisting of U7c and associated components operates at a frequency of 14.31818 MHz for NTSC, or 14.5 MHz for PAL. The oscillator output is buffered by U7a, measured at the **OSC FREQ** test point, provides an 8 times bit rate clock to divider U3, which generates a series of timing pulses at the VITC bit rate (1.78977 MHz for NTSC, 1.8125 MHz for PAL). Each positive going transition of the VITC data re-synchronizes the divider so that the VITC recovery clock at U3 pin 13 occurs in the middle of each bit.

Inverted VITC data is shifted into U11 which calculates the cyclic redundancy check (CRC) word for the recovered data. Valid CRC and 90 bits of code, detected by U9, clocks U6a on, disabling the VITC clock and generating a VITC RDY signal to the MCU. The MCU unloads the VITC data through switch U4.

1.5.4. Video Character Generator (6221-30)

The character inserter logic and keyer are contained on a separate circuit sub-module which connects to the main circuit card via header J1 & J2. DC restored video, HSYNC, VSYNC, and the MCU address and data bus are fed up the header from the main board.

The character display is formatted to display 14 (16 for PAL) rows of 32 characters each in the small size, and 7 (8 for PAL) rows in the large size. Each of the character positions corresponds to one of 512 locations in RAM U9. The MCU writes characters into specified locations in the RAM corresponding to the position of the characters on the screen. RAM locations are scanned during each television field. Valid characters address corresponding sections of the character PROM U15 and character data is shifted out from U8 and keyed into the video by U23. Characters with bit 7=1 are written into all positions of the RAM where no characters are to be displayed. These characters disable keyer control flip flop U6a, allowing program video to pass through the keyer. Jumper J3 selects the background signal for the keyer. Installing the jumper in the 'B' position selects the keyer control signal from U6a as the background. Installing the jumper in the 'NB' position selects the character dots themselves. Leaving the jumper off selects the auto mode, where the MCU controls the background, however this mode is not supported when the VCG sub-module is used with the 6220 base module, and hence the jumper should be installed in one of the two positions. Horizontal size of the characters is adjusted by the **HOR SIZE** trimpot (VR1). The starting position of the characters at the left of the screen is preset but may be altered by varying the value of R2.

The VCG keyer control signal from U22a and U22b switch U23a on and U23d off for program video, and vice versa for characters. When U23d is on, character dots are added to the black level of the video.
To calibrate the VCG keyer, connect colour bars from your sync generator to the Video input loop, of the 622, and to channel A of your oscilloscope, and terminate it. Connect the VCG output to channel B of your scope and terminate it. Adjust the **GAIN** trimpot (VR 2) so that the output amplitude matches the input. Adjust the **LEVEL** trimpot (VR 3) so that the inserted characters are slightly above peak white luminance level. The frequency response is adjusted using trimmer VC 1 so that the chrominance amplitude of the inputs and outputs is the same.

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2. 4600T INSTALLATION

2.1. REAR PANEL

The following connectors are provided on the rear panel for connection into your system. Each slot has the same configuration for its respective module.

Timecode Connectors

LTC OUT:A ¼"stereo phone jack for output of SMPTE/EBU longitudinal time code from generator.

LTC IN: A ¼" stereo phone jack for input of SMPTE/EBU longitudinal time code.

Video Connections

VIDEO IN: A BNC loop for input of program video with vertical interval time code. This input is also used to insert characters onto.

OUT: A BNC output of program video with characters inserted.

Serial/Parallel I/O

SER_PAR I/O A 9 pin female "D"connector for either parallel or serial remote control depending on the module inside the 4600T.

Power Connections

LINE: The unit may be set for either 115v/60 Hz or 230v/50 Hz AC operation. The voltage selector switch is accessible on the top panel. The line voltage connector contains an integral slow blow fuse (and a spare one).

2.2. INSIDE THE 4600T:REMOVING THE FRONT PANEL

During the installation procedure it may be necessary to remove the front panel to gain access to the programming switches located inside the unit. This can be accomplished in a few seconds by turning the quick release fasteners, located at the left and right hand sides of the front panel, several turns counter clockwise. The front panel assembly pulls off showing the three circuit modules that comprise the unit.

The module in the center is the LTC/VITC reader/character inserter for time code, and the one on the right is the LTC/VITC reader/character inserter for Keykode.
To replace the front panel assembly, slide it into place, and turn the quick release fasteners clockwise until they are firmly secured.

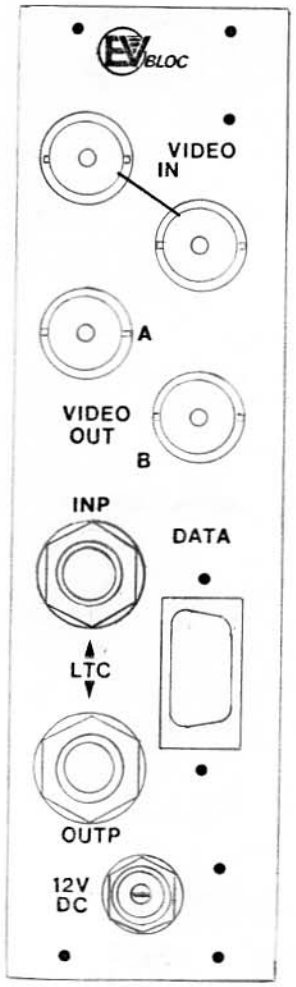
2.3. MOUNTING

The 4600T rackframe is equipped with rack mounting angles and fits into a standard 19 inch by 1 3/4 inch (483mm x 45mm) rack space. The mounting angles may be removed if rack mounting is not desired.

2.3.1. Selecting the Correct Mains Voltage

Power requirements are 115 or 230 volts AC at 50 or 60 Hz, switch selectable on the top cover. Before connecting the line power, be sure to select the proper line voltage. Also, check that the line fuse is rated for the correct value marked on the rear panel.

Never replace with a fuse of greater value.



6031/6051 REAR PANELS

NOTE: THIS DRAWING SHOWS THE EV-BLOC STAND-ALONE SERIES I/O MODULE REAR PANEL WITH ALL CONNECTORS INSTALLED. ON SOME VERSIONS HOWEVER, SOME CONNECTORS ARE NOT REQUIRED AND WILL BE REPLACED WITH PLASTIC-HOLE PLUGS.

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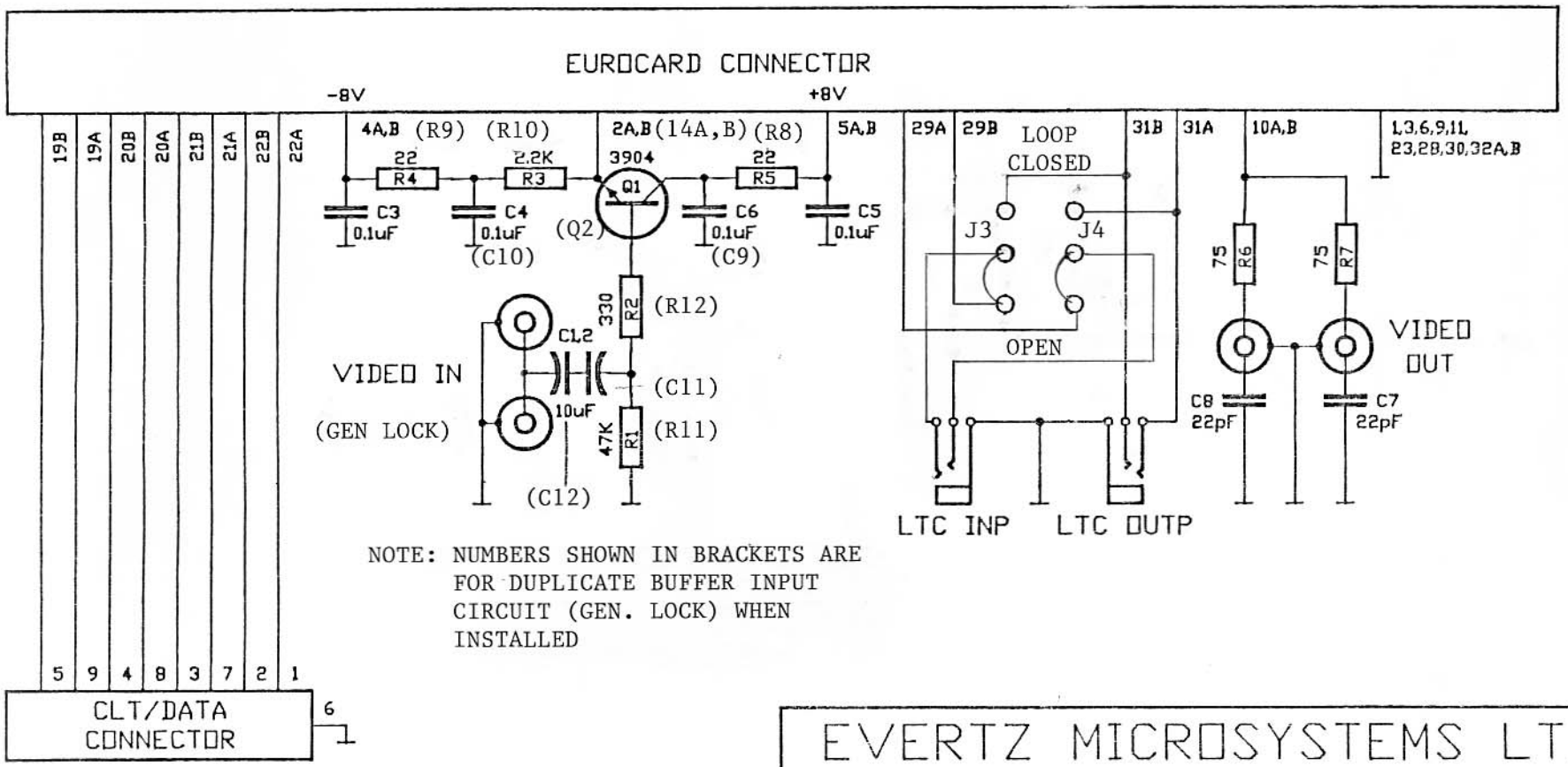

NOTE: NUMBERS SHOWN IN BRACKETS ARE FOR DUPLICATE BUFFER INPUT CIRCUIT (GEN. LOCK) WHEN INSTALLED

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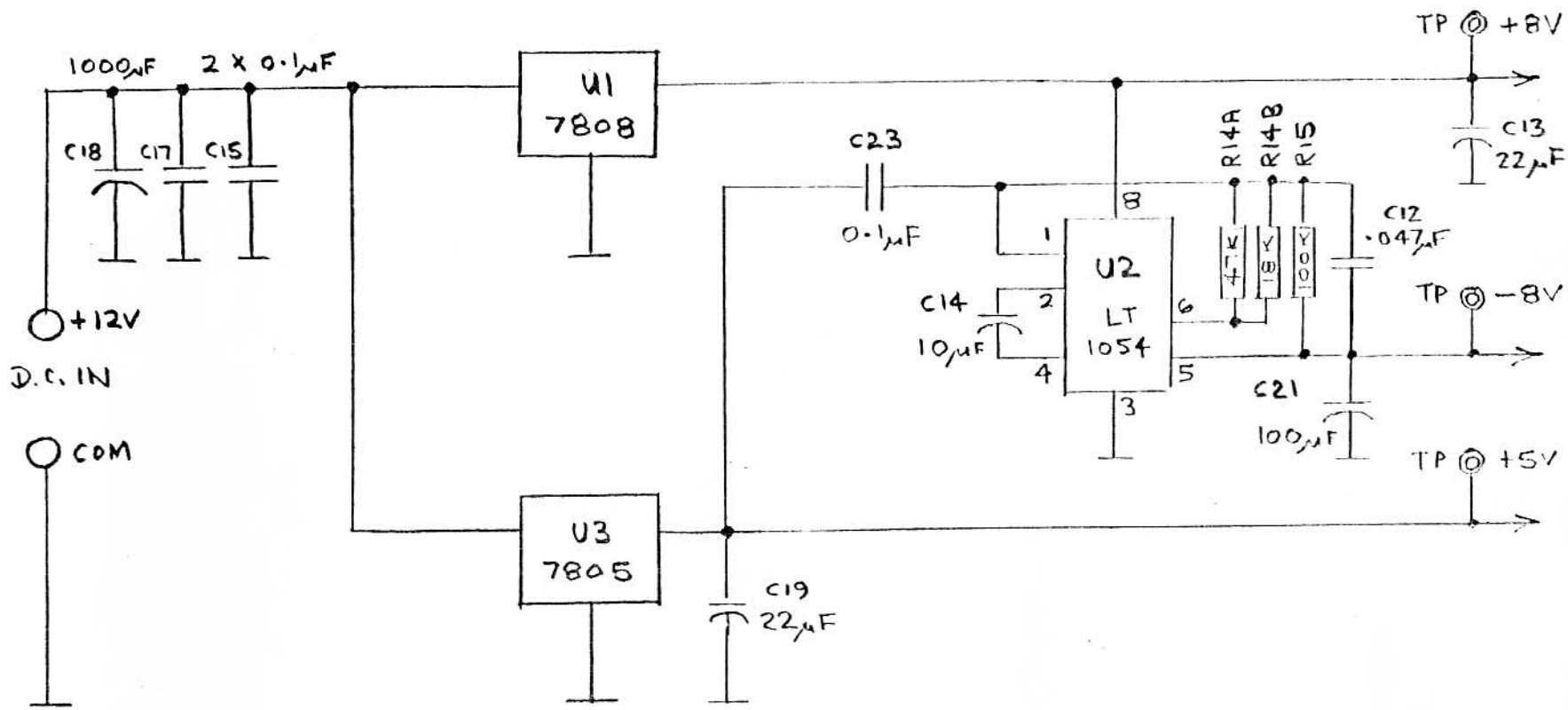

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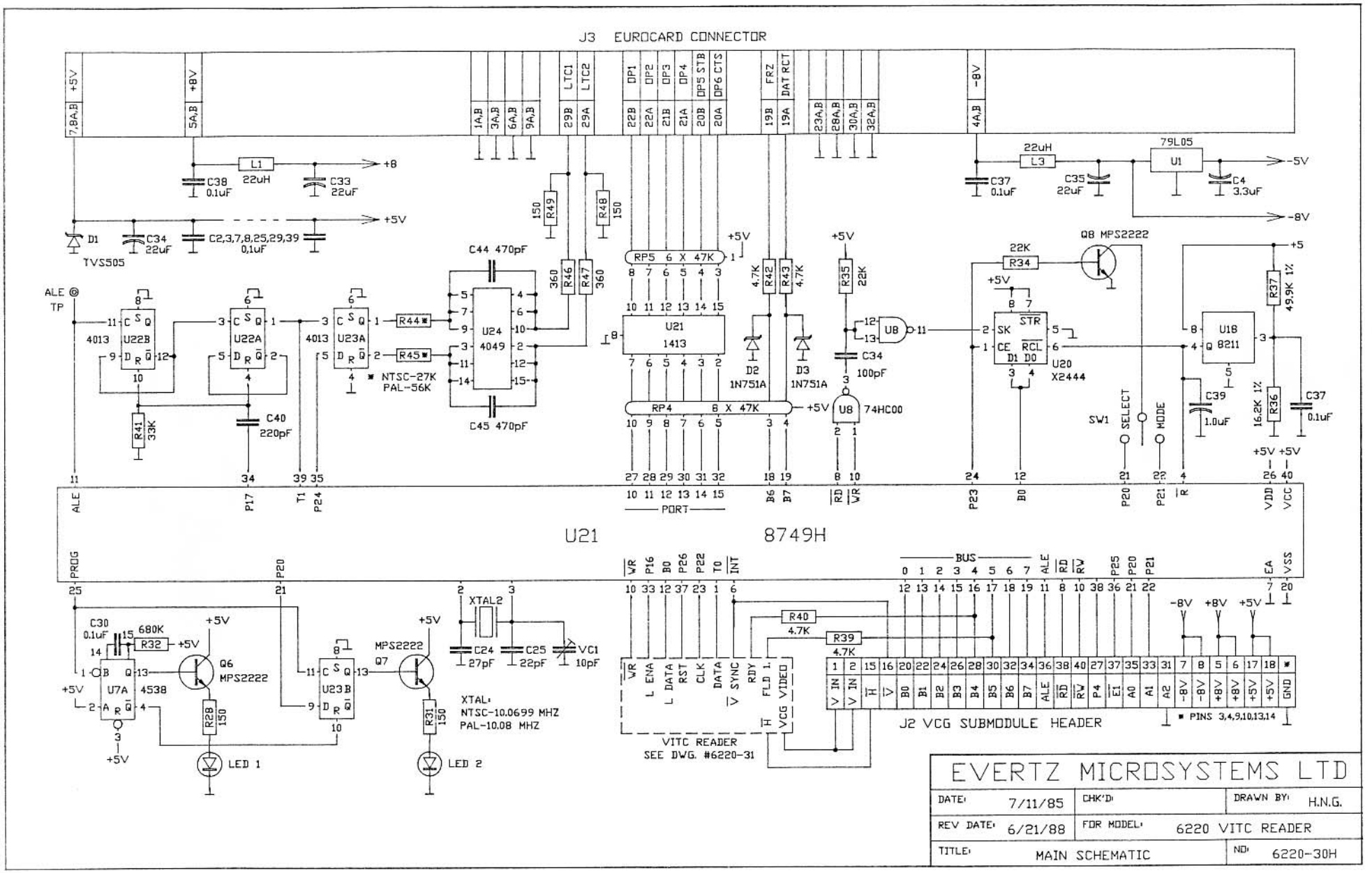

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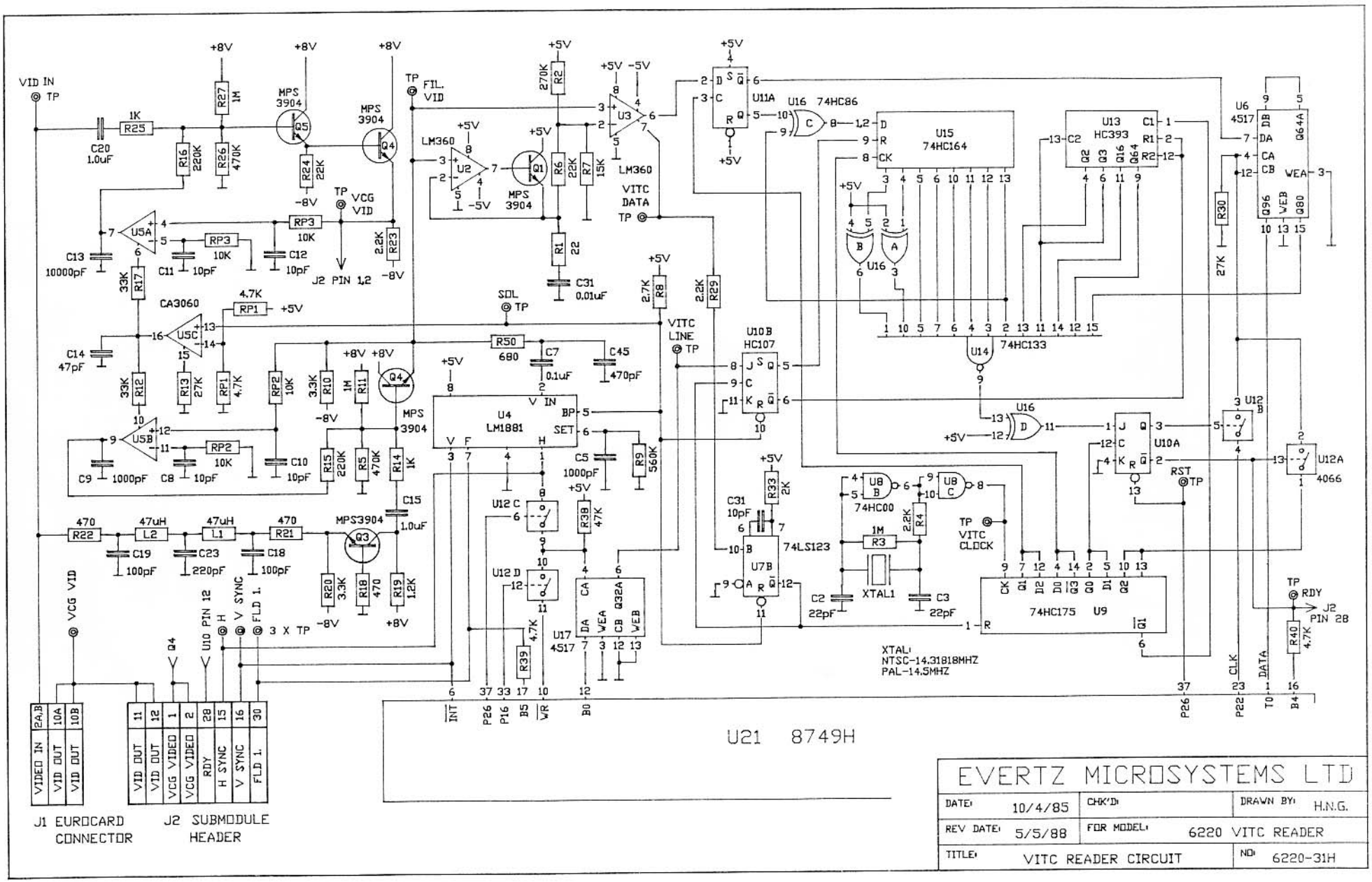
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C20 1.0uF
1K R25
R16 220K
R27 1M
R26 470K
MPS 3904 Q5
MPS 3904 Q4
R24 22K
+8V
-8V
TP VCG VID
J2 PIN 1,2
2.2K R23
RP3 10K
C13 10000pF
C11 10pF
C12 10pF
U5A
33K R17
CA3060
4.7K RP1
+5V
U5C
C14 47pF
33K R12
R13 27K
RP1 4.7K
RP2 10K
3.3K R10
1M R11
U5B
RP2 10K
C9 1000pF
C8 10pF
C10 10pF
R15 220K
R5 470K
R14 1K
C15 1.0uF
MPS3904 Q3
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47uH L2
47uH L1
470 R21
C19 100pF
C23 220pF
C18 100pF
R20 3.3K
R18 470
R19 1.2K
TP FIL. VID
270K R2
LM360 U2
MPS 3904 Q1
R6 22K
R7 15K
U3
LM360
VITC DATA TP
R1 22
C31 0.01uF
SDL TP
VITC LINE TP
R50 680
C7 0.1uF
C45 470pF
U4 LM1881
V IN
BP
SET
C5 1000pF
R9 560K
U12 C
U12 D
R38 47K
R39 4.7K
U17 4517
2.7K R8
2.2K R29
U11A
U16 74HC86
U15 74HC164
U13 HC393
U14 74HC133
U10B HC107
U10A
U12A 4066
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PAL-14.5MHZ
TP RDY
J2 PIN 28
R40 4.7K
U21 8749H
INT
P26
P16
B5
WR
B0
P22
T0
B4
CLK
DATA
J1 EURO CARD CONNECTOR
J2 SUBMODULE HEADER
VIDEO IN
VID OUT
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RDY
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V SYNC
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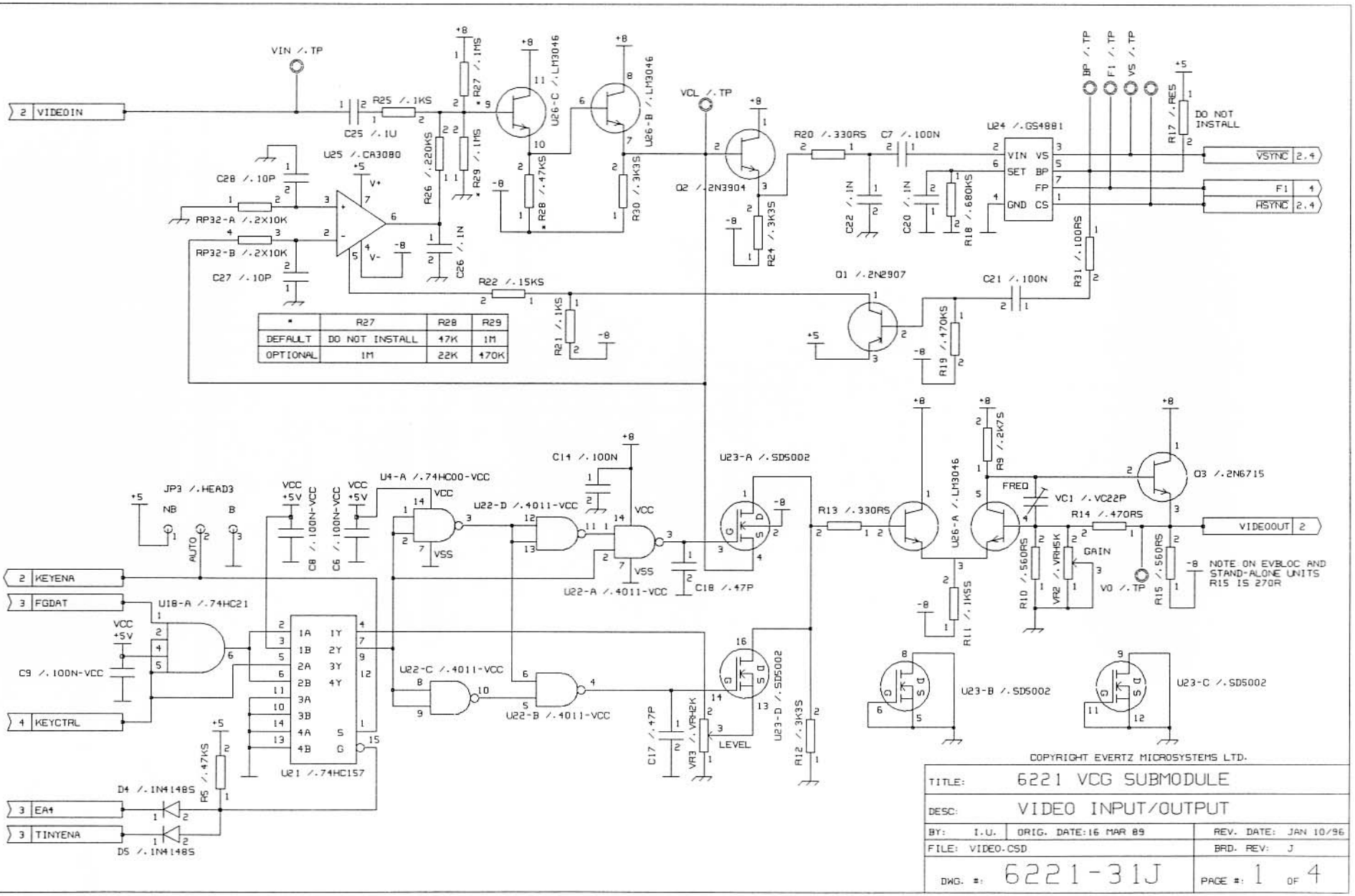
REV DATE: 5/5/88
FOR MODEL: 6220 VITC READER
TITLE: VITC READER CIRCUIT
NO: 6220-31H



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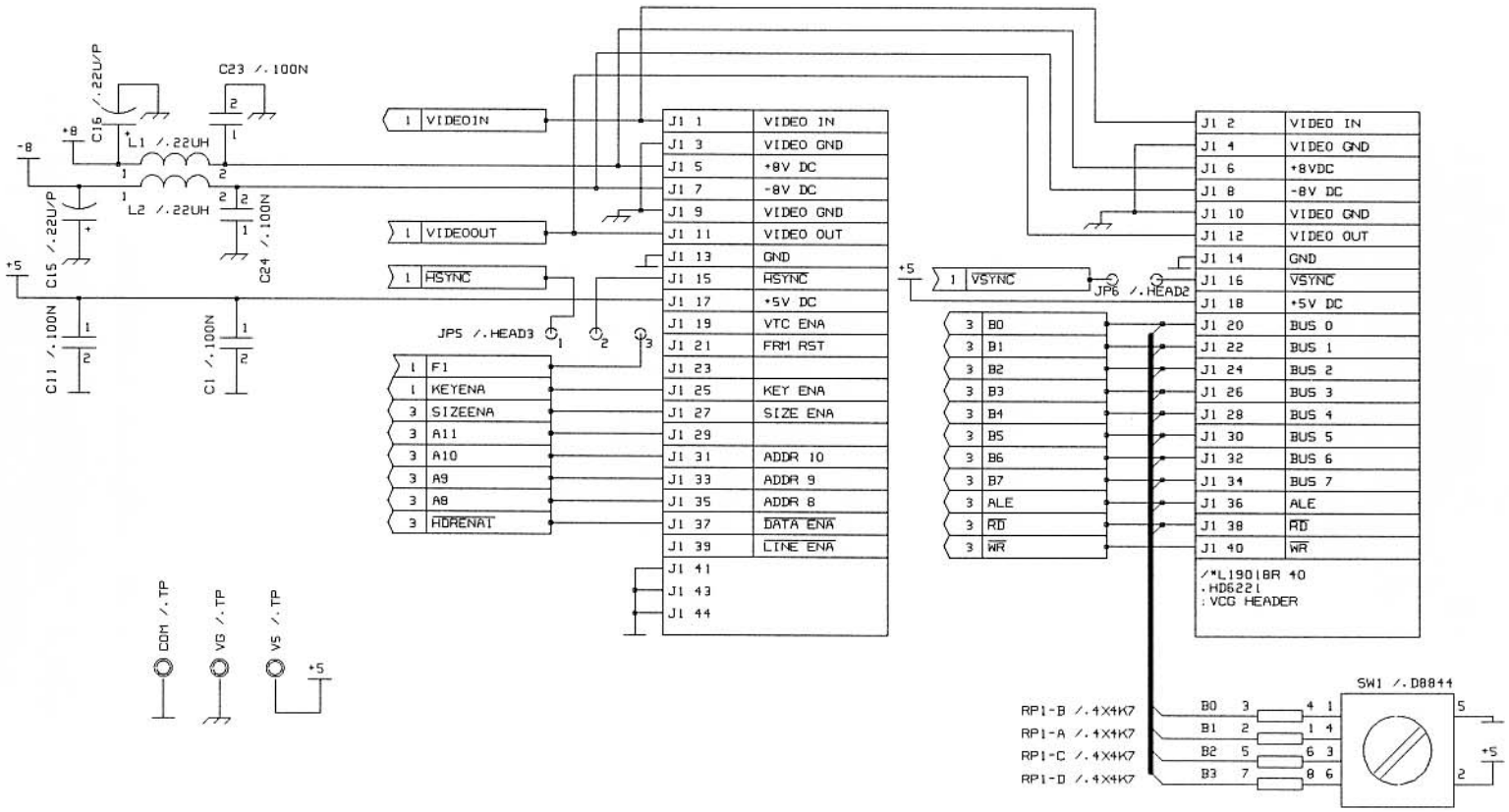
TITLE:	6221 VCG SUBMODULE		
DESC:	VIDEO INPUT/OUTPUT		
BY: I.U.	ORIG. DATE: 16 MAR 89		REV. DATE: JAN 10/96
FILE: VIDEO.CSD			BRD. REV: J
DWG. #: 6221-31J			PAGE #: 1 OF 4



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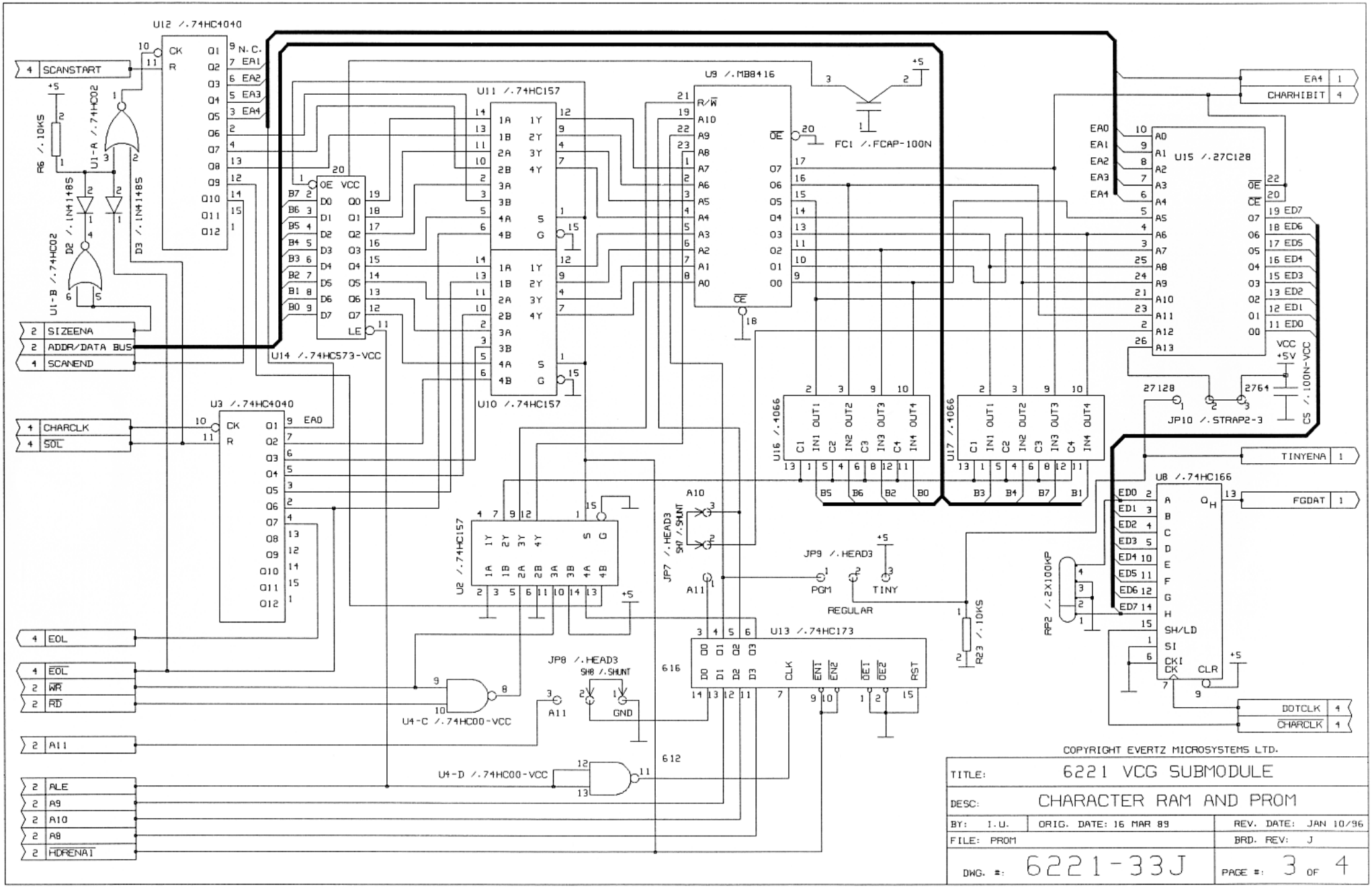
TITLE:	6221 VCG SUBMODULE	
DESC:	CONNECTOR INTERFACE	
BY: I.U.	ORIG. DATE: 16 MAR 89	REV. DATE: JAN 10/96
FILE: IF6221		BRD. REV: J
DWG. #: 6221-32J		PAGE #: 2 OF 4



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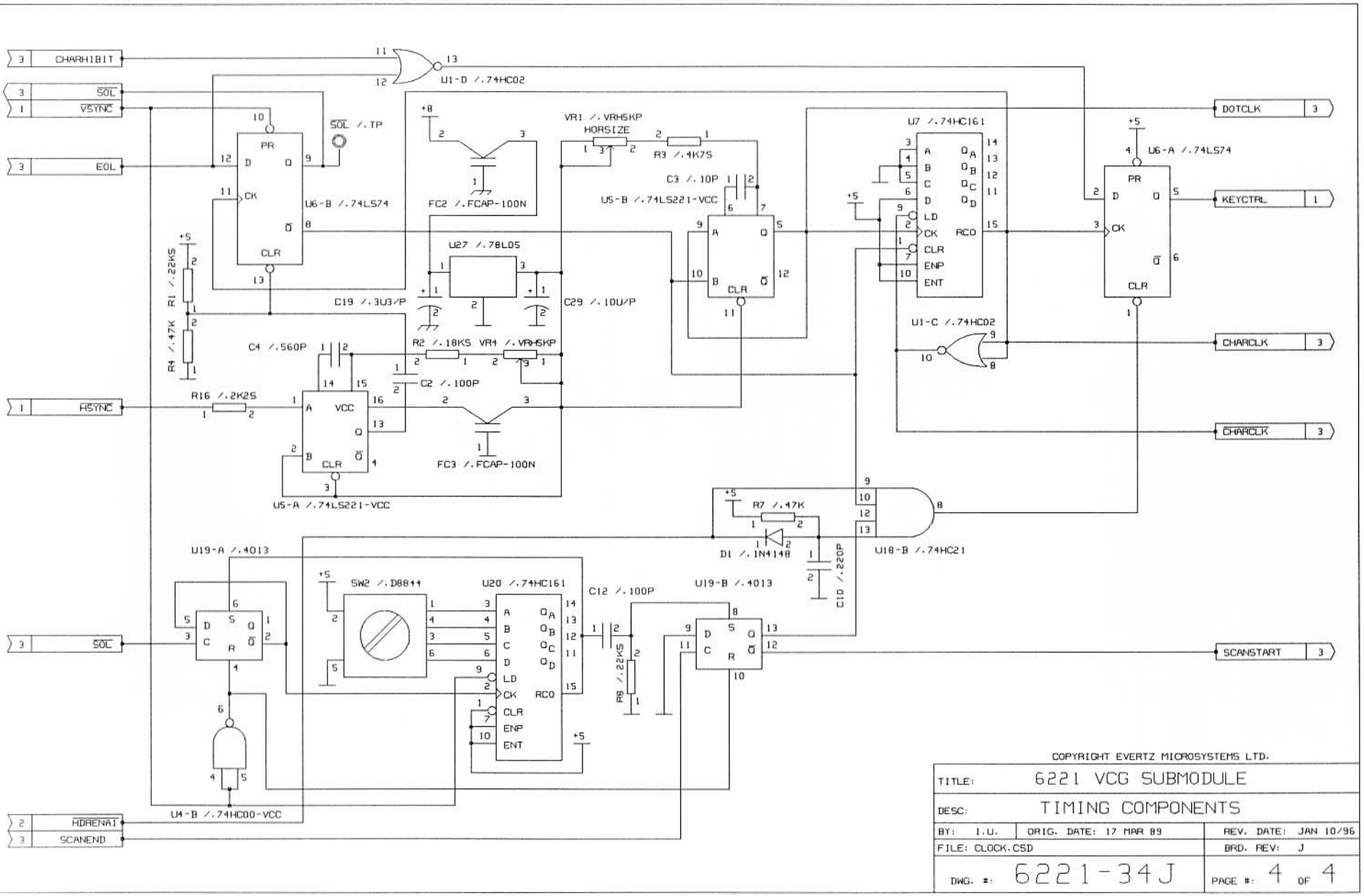
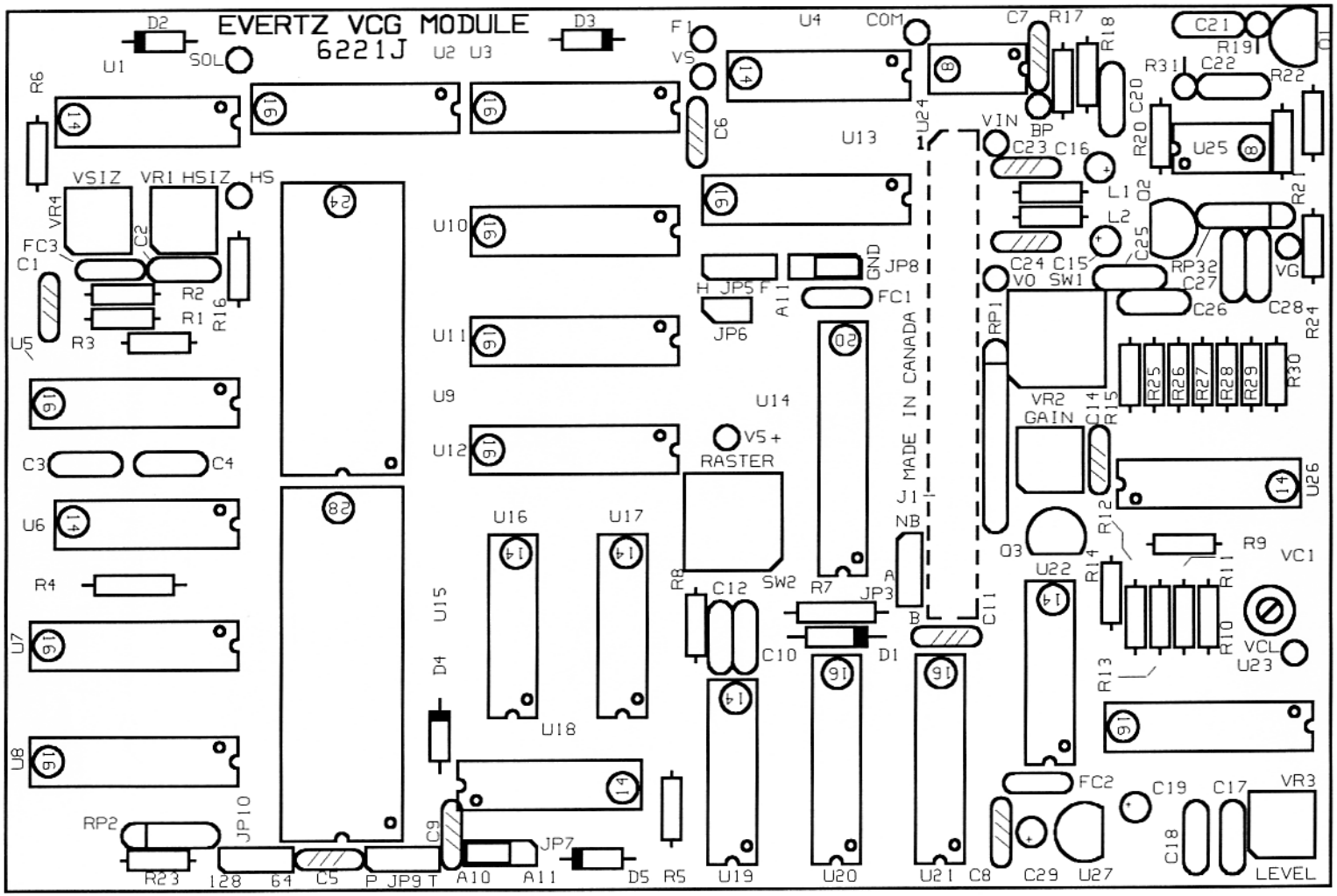
TITLE:	6221 VCG SUBMODULE		
DESC:	CHARACTER RAM AND PROM		
BY: I.U.	ORIG. DATE: 16 MAR 89		REV. DATE: JAN 10/96
FILE: PROM			BRD. REV: J
DWG. #: 6221-33J			PAGE #: 3 OF 4

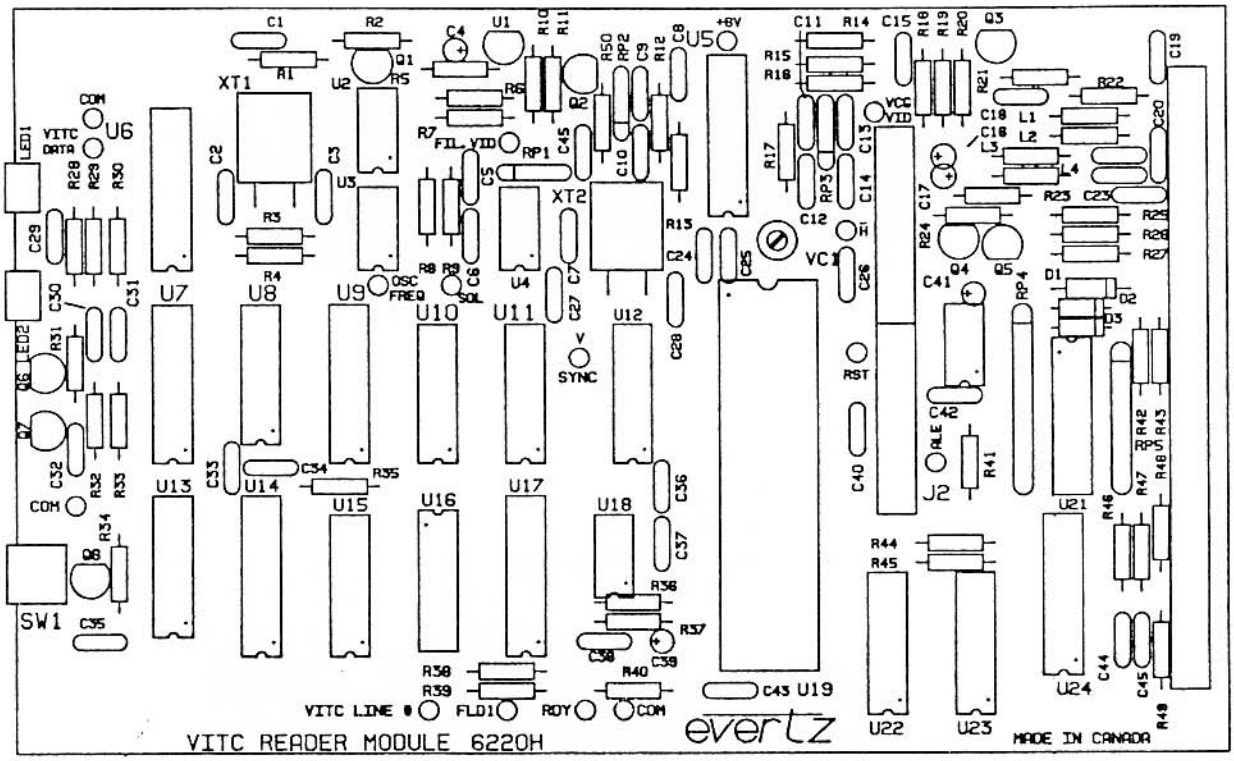

3 CHARHIBIT
3 SOL
1 VSYNC
3 EOL
1 HSYNC
3 SOL
2 HDRENA1
3 SCANEND
U1-D /.74HC02
SOL /.TP
U6-B /.74LS74
FC2 /.FCAP-100N
VR1 /.VRH5KP
HORSIZE
R3 /.4K75
C3 /.10P
U5-B /.74LS221-VCC
U27 /.78L05
C19 /.3U3/P
C29 /.10U/P
R1 /.22KS
R4 /.47K
C4 /.560P
R2 /.18KS
VR4 /.VRH5KP
C2 /.100P
R16 /.2K2S
FC3 /.FCAP-100N
U5-A /.74LS221-VCC
U7 /.74HC161
U6-A /.74LS74
U1-C /.74HC02
DOTCLK 3
KEYCTRL 1
CHARCLK 3
CHARCLK 3
R7 /.47K
D1 /.1N4148
C10 /.220P
U18-B /.74HC21
U19-A /.4013
SW2 /.D8844
U20 /.74HC161
C12 /.100P
U19-B /.4013
R8 /.22KS
SCANSTART 3
U4-B /.74HC00-VCC
COPYRIGHT EVERTZ MICROSYSTEMS LTD.
TITLE: 6221 VCG SUBMODULE
DESC: TIMING COMPONENTS
BY: I.U.
ORIG. DATE: 17 MAR 89
REV. DATE: JAN 10/96
FILE: CLOCK.CSD
BRD. REV: J
DWG. #: 6221-34J
PAGE #: 4 OF 4

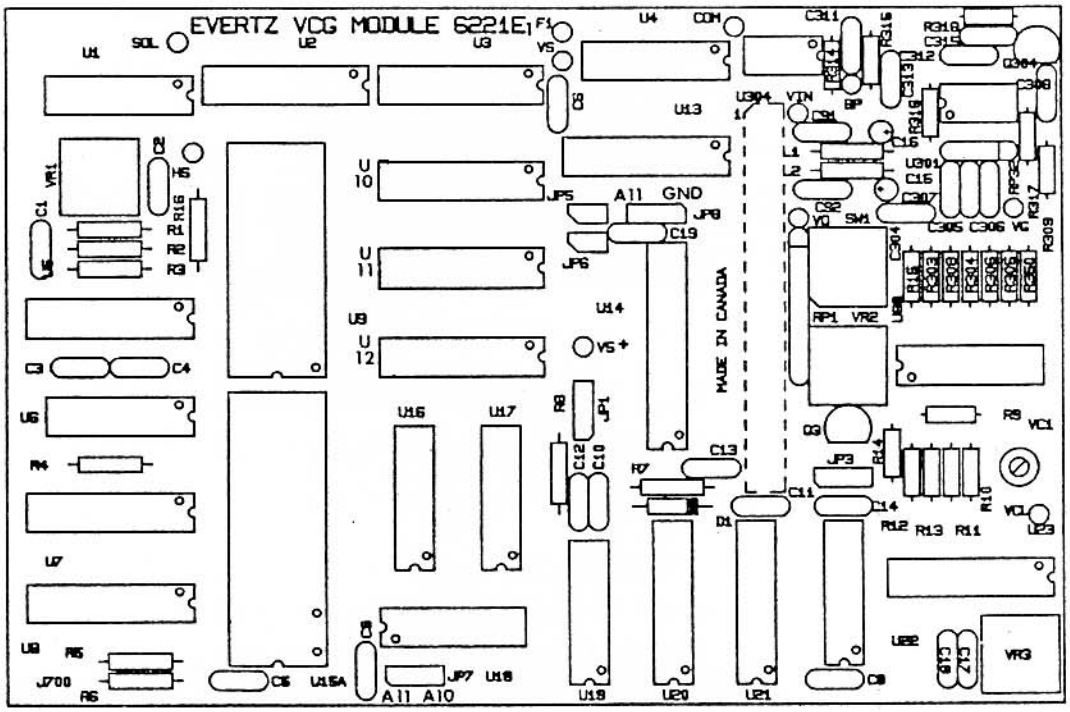


ASSEMBLY DRAWING

EVERTZ MICROSYSTEMS LTD	DATE: JUN 13/89		REV DATE: JAN 15/96
TITLE MODEL 6221 COMPONENT LAYOUT	REV: J	DWN: T.U.	DWG No.: 6221-80J

evertz	TITLE: 6220 VITC READER MODULE	LEVEL: 8-SCREEN	REV: H
		DATE: MAR 17/88	DWN: I.U.





EVERTZ	TITLE: EV6221 VCG SUB-MODULE	LEVEL: 2 COMPONENT SIDE SILKSCREEN	REV: E
		DATE: JUNE 13/89	DWN: I.U.

TITLE: MODEL 622/6221 COMPONENT LAYOUT	DATE: OCT. 27/89	DWG.NO: 622-81H

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