GRASS VALLEY GROUP

Instruction Manual

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8914
DUAL AES/EBU DELAY DISTRIBUTION AMPLIFIER

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Preface

About This Manual

This manual describes the features of a specific module of the 8900 Series Distribution Amplifier family. As part of this module family, it is subject to Safety and Regulatory Compliance described in the 8900 Series frame and power supply documentation (see the *8900 Series User's Guide*).

8914 Dual AES/EBU Delay Distribution Amplifier

Introduction

As the transition to digital video and audio accelerates, there is an increased need to delay the audio associated with broadcast video. This is due to the relatively large processing times associated with DVEs and switchers. The 8914 provides a low cost and easy-to-use solution to the lip sync errors associated with these large delays. Minimizing space requirements, the 8914 provides two fully controllable delay paths on a single board, allowing up to 20 delays (ten modules) in a two rack unit frame. If instead of two delays you require more distribution, the first channel can be passively looped to the second channel to produce seven outputs. The 8914 is also a full-featured reclocking distribution amplifier that fits inthe 8900 series frame.

A clock referenced to the applied input reclocks all outputs in each section. The delay is set using 16-position rotary switches on the front of the module. There are fine and coarse rotary adjustment switches for each delay channel.

The 8914 offers the following features:

- Two full-function delays on a single board,
- All outputs reclocked to reduce jitter,
- Up to one half second delay in approximately 2 ms increments,
- Support of 32, 44.1 and 48 KHz sample rates,
- Four outputs on channel one, three outputs on channel two,
- Loop-through input on channel one enables redundant system design,
- Accepts input cable lengths of up to 1000m (Belden 8281 or equivalent), and
- Up to twenty AES/EBU delays in a 2 RU 8900 Frame.

Module Installation

There are ten cell locations in the frame to accommodate either analog or digital modules. These are the left ten slots. Refer to Figure 1.

The two cells on the right are allocated for the power supplies. For additional information concerning the Power Supply module, refer to the Power Supply manual.

The third cell from the right is allocated for the Controller module. This module provides the interface for the forced air cover, as well as the SMPTE 269M fault reporting (health alarm) and the error detection. For additional information concerning the Controller module, refer to the Controller manual.

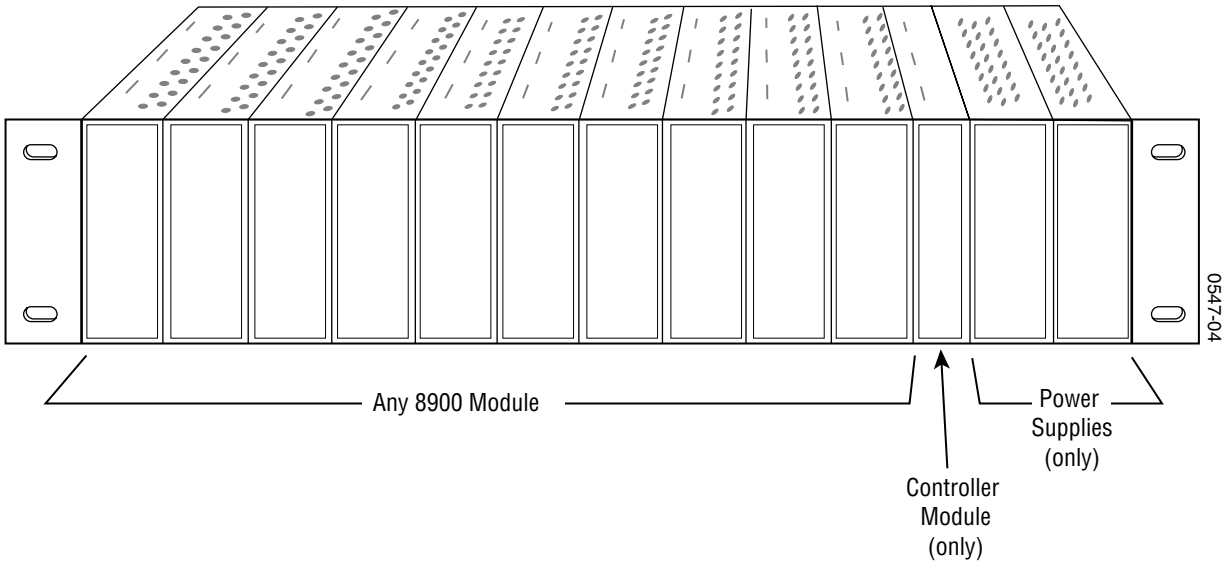

Figure 1. 8900 Series Frame

To install a module into the frame, follow these steps:

1. Insert the module into the frame, connector end first, with component side of the module facing to the right and ejector tab to the top.
2. Verify that the module connector seats properly against the backplane.
3. Press the ejector tab in to seat the module in place.

Cabling

8900 module locations are interchangeable within the frame. The maximum number of modules the frame will accept is ten. Figure 2 illustrates the rear connector plate for an 8900 Series frame.

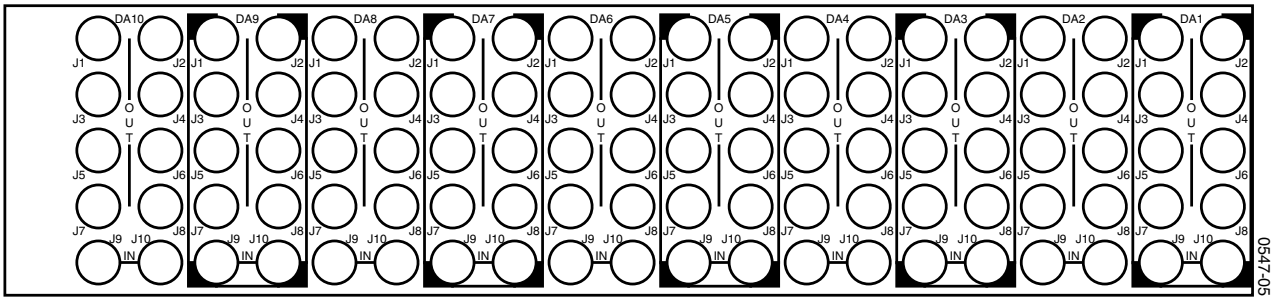

Figure 2. 8900 Series Frame Rear Connector

Note At the back of this manual are die-cut overlay cards that can be placed over the rear connector BNCs to identify the specific 8914 connector functions.

Inputs

The 8914 Dual AES/EBU Delay DA has two channels. Delay 1 is a 1x4 DA with a looping input. Delay 2 is a 1x3 DA with a terminated input. Transformer coupling on the inputs eliminates common mode noise.

For a delay channel 1 signal, connect an input source to one of the loopthrough input connectors, J9 or J10 (See Figure 3). Terminate the unused connector into 75Ω. Use J7 for input to delay channel 2. J7 is internally terminated into 75Ω.

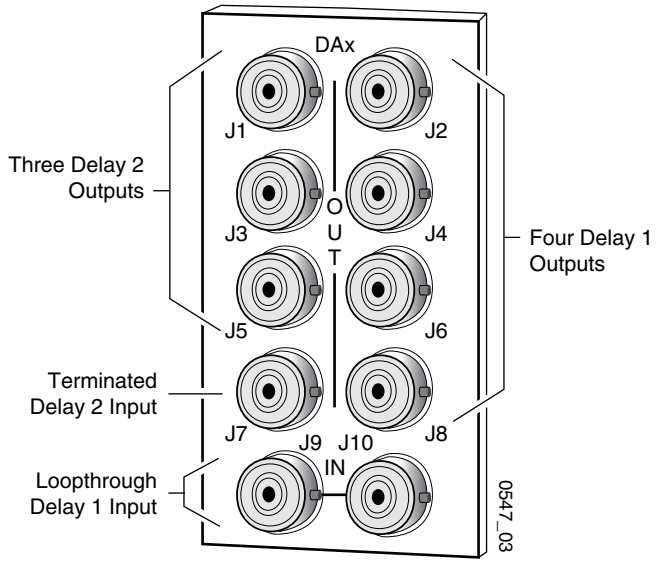

Figure 3. Typical Module Input and Outputs

Outputs

There are four identical outputs for delay channel 1— J2, J4, J6, and J8. There are three identical outputs for delay channel 2 — J1, J3, and J5. The destination equipment should have an input impedance of 75 Ω unless it has loopthrough inputs, in which case the unused loopthrough connector must be terminated into 75 Ω.

Adjustments, Testpoints, and Indicators

The 8914 DA has ground and +5V testpoints easily accessible on the front edge of the module (see Figure 4).

Between the testpoints is a green Power On LED.

Each reclocking section is phase-locked to its AES input signal. The Lock LEDs on the front of the module are on when the reclocking chip has locked on the incoming AES data stream. There is one Lock LED for each channel as shown.

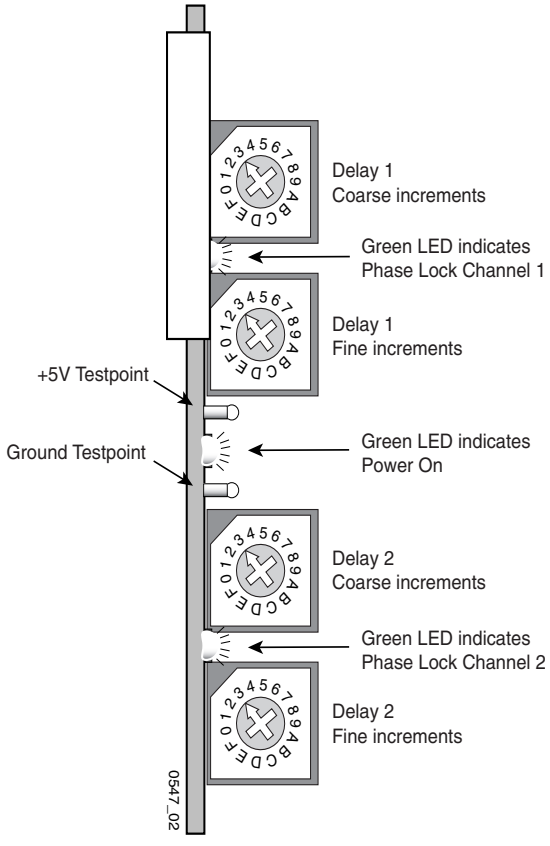

Figure 4. 8914 Adjustments, Testpoints, and Indicators

Delay Adjustments

Signal delay for each channel is set by two 16-position rotary switches that provide additive coarse and fine adjustments. The amount of both the inherent delay of the signal path and the increments of induced delay varies according to signal data rate. Table 1 provides delay figures for the three accepted AES data rates—48 KHz, 44.1 KHz, and 32 KHz.

Table 1. Delay Adjustment Settings

Input Signal	Minimum Delay (switches @ 0,0)	Adjustment	Adjustment Increment	Incremental Delay Range
48 KHz	1.2 ms	Fine	2 ms (96 frames)	2 ms to 510 ms
		Coarse	32 ms (8 blocks)	
44.1 KHz	1.305 ms	Fine	2.177 ms (96 frames)	2.177 ms to 555.9 ms
		Coarse	34.88 ms (8 blocks)	
32 KHz	1.799 ms	Fine	3 ms (96 frames)	3 ms to 765 ms
		Coarse	48 ms (8 blocks)	

48 KHz Input Signal Example

Inherent (minimum) circuit delay with no set delay adjustment (rotary switches at 0, 0) is 1.2 ms. Any switch setting above 0,0 masks the inherent delay and, starting at 2 ms, adds the selected number of delay increments.

For example, setting Coarse to 0 and Fine to 1 produces 2 ms of delay. Each additional Fine switch increment adds 2 ms.

Setting Coarse to 1 and Fine to 0 produces 32 ms of delay. Each additional Coarse switch increment adds 32 ms.

Specifications

Table 2. 8914 Specifications

Parameter	Value
Inputs	
Number	Two (1 loopthrough, 1 terminated)
Signal type	AES/EBU digital audio, per AES3id:1995 and SMPTE 276M
Connector	75Ω BNC
Return loss	> 25 dB, 0.1 to 6 MHz
Frame Rates	32, 44.1, or 48 KHz (Automatic selection)
Outputs	
Number	Seven (4 delay channel one, 3 delay channel two)
Signal type	AES/EBU digital audio, per AES3id:1995 and SMPTE 276M
Connector	75Ω BNC
Return loss	> 25 dB, 0.1 to 6 MHz
Intrinsic Jitter	< 6 ns
Performance	
Minimum Output Delay	1.2 ms
Maximum Output Delay	510 ms (127.5 AES/EBU blocks)
Environmental	
Operating temperature range	0 to 45° C, noncondensing
Non-operating temperature range	-10 to +70° C, noncondensing
Power Requirements	
Supply Voltage	+12 Volts
Power consumption	3.5 Watts
Physical	
Frame	Resides in standard 2 rack unit 8900 Series frame

Service

The 8914 modules make extensive use of surface-mount technology and programmed parts to achieve compact size and adherence to demanding technical specifications. Circuit modules should not be serviced in the field.

If your module is not operating correctly, proceed as follows:

- Check frame and module power and signal present LED.
- Check for presence and quality of input signals.
- Verify that source equipment is operating correctly.
- Check cable connections.
- Check output connections for correct I/O mapping (correct input is used for the corresponding channel output).

Refer to Figure 4 for supply voltage test points on the 8914 module.

If the module is still not operating correctly, replace it with a known good spare and return the faulty module to a designated Grass Valley repair depot. Call your Grass Valley representative for depot location.

Refer to the *Contacting Grass Valley Group* at the front of this document for the Grass Valley Customer Service Information number.

Functional Description

Refer to the block diagram in Figure 5 while reading the description.

There are 2 inputs for the module. One of these inputs is a loop-through input. The data paths are otherwise conceptually identical for both inputs. The inputs are first received by the receive circuit. Next, the Field Programmable Gate Array (FPGA) sends the data to the FIFO, which returns the data to the FPGA. Finally, the data is passed to the transmit circuit.

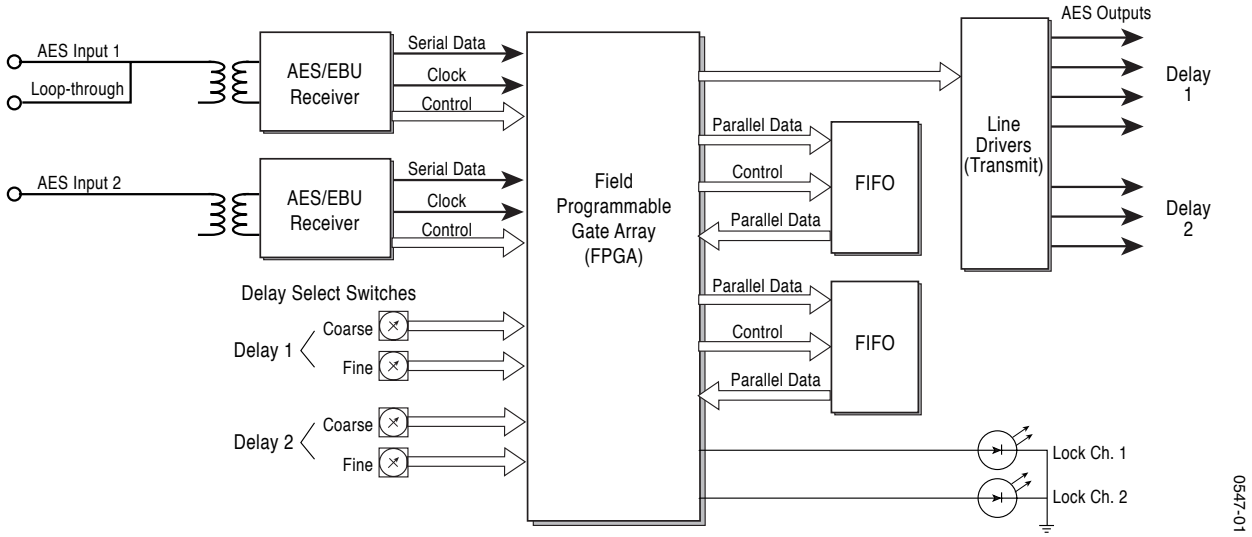

Figure 5. 8914 Dual AES/EBU Delay DA Block Diagram

Receive Circuit

This circuit features a digital audio transformer conforming to EBU standards.

The AES/EBU receiver recovers audio data and low jitter clocks from the digital audio input transmission line. The data is reclocked, and then sent to the FPGA. A special mode allows the preamble and bi-phase mark data to pass through in its entirety. The 6.144 MHz clock signal is also sent to the FPGA.

FPGA

The FPGA is a field programmable gate array containing proprietary Grass Valley control circuitry. The FPGA converts the serial AES/EBU stream to 12-bit parallel data. The width of the data corresponds to the width of the

FIFO (First In First Out) delay circuit. A small delay is introduced by the nature of the serial to parallel circuit. The output goes to the external FIFO chip.

The FIFO circuits are used to create various amounts signal delay. In the FPGA, a separate controller is provided for each data stream to the FIFOs. The two controllers perform the same functions. The controller outputs the following signals: read reset, write reset, read clock, and write clock. The read and write clocks are the same signal, and its frequency is determined by the width of the parallel data.

The amount of delay is determined by two 16-position rotary switches. Depending on input signal rate, the Fine switch delays the data by 2 to 3 ms increments. The Coarse switch delays the data by 30 to 48 ms increments. There is a minimum circuit delay of from 1.2 to 1.799 ms (for precise adjustment details, see *Adjustments, Testpoints, and Indicators on page 4*).

FIFO Circuits

The FIFO circuits create the signal delay. The FIFO receives parallel data from the FPGA. All clock and control signals are provided by the FPGA. The FIFO output is sent back to the FPGA.

Line Drivers

The delayed serial data is passed to the Line Driver (transmit) circuit.

Frequency Lock LEDs

The logic to turn on and off the Signal Lock LEDs is provided by the three Error pins from the AES/EBU receiver. A no lock error condition (Lock LED off) indicates that the phase-lock loop in the receiver is not locked to the incoming data stream or the input signal is not present.

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