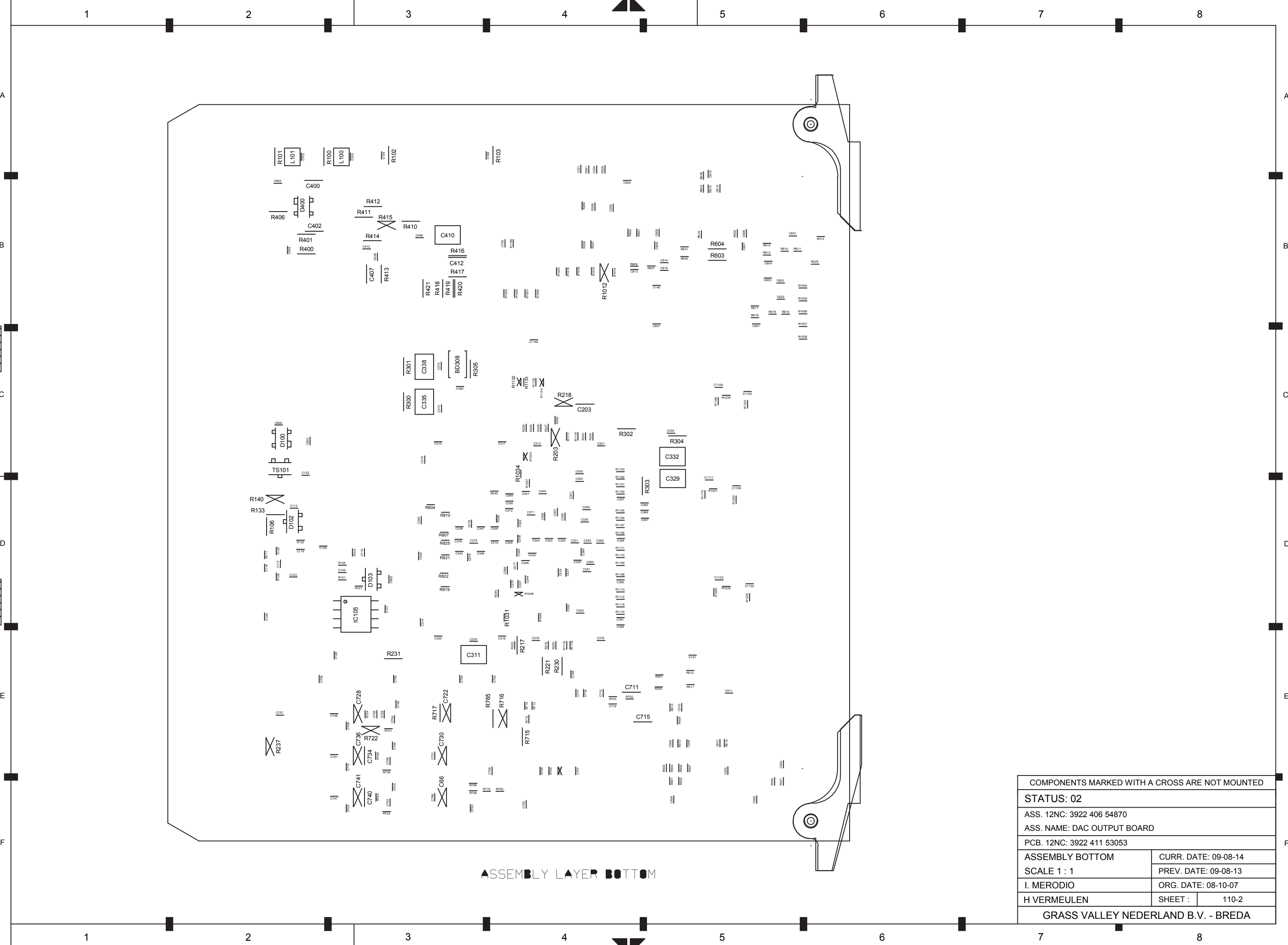




GRASS VALLEY
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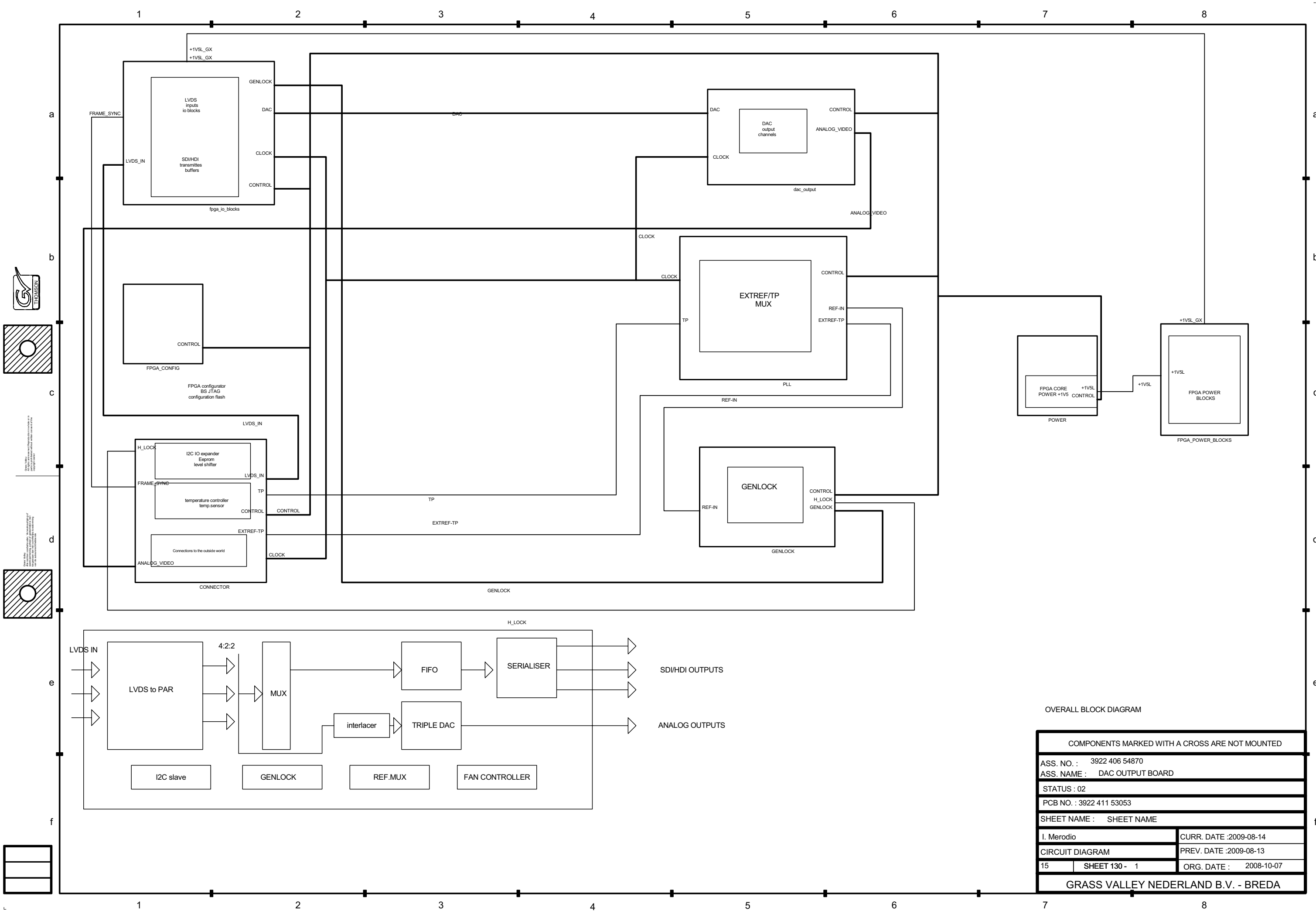
GRASS VALLEY
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ASSEMBLY LAYER BOTTOM

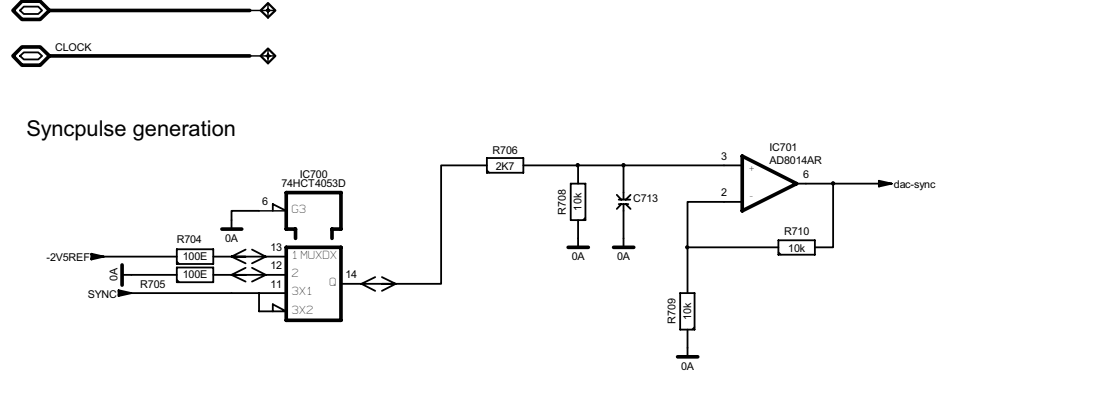
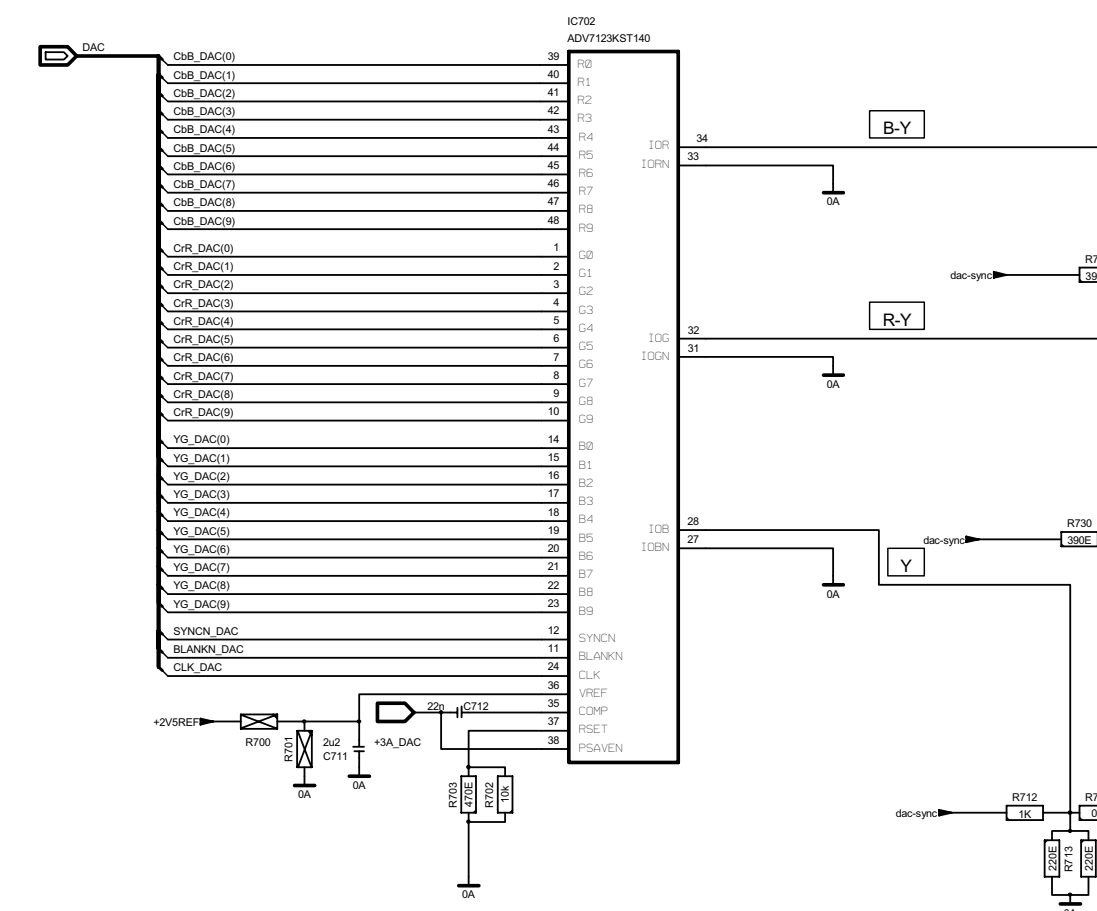
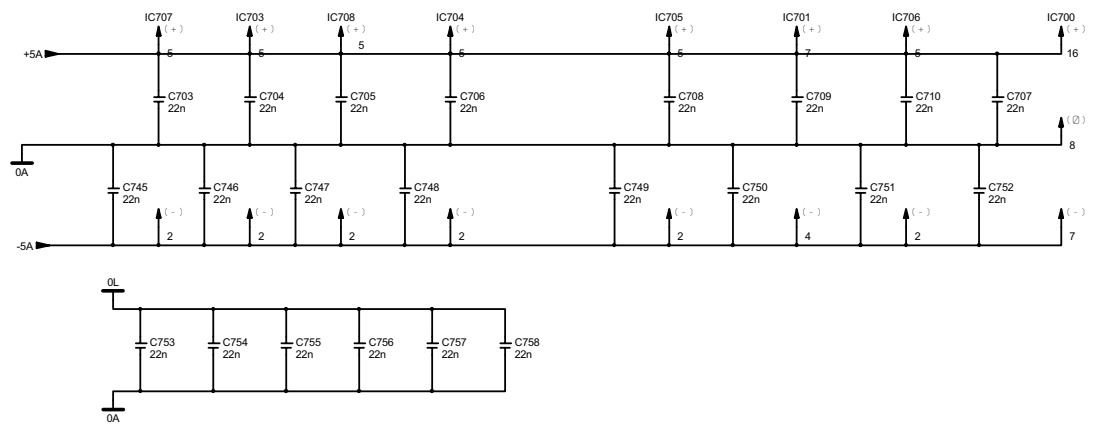
COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
STATUS: 02		
ASS. 12NC: 3922 406 54870		
ASS. NAME: DAC OUTPUT BOARD		
PCB. 12NC: 3922 411 53053		
ASSEMBLY BOTTOM	CURR. DATE: 09-08-14	
SCALE 1 : 1	PREV. DATE: 09-08-13	
I. MERODIO	ORG. DATE: 08-10-07	
H VERMEULEN	SHEET :	110-2
GRASS VALLEY NEDERLAND B.V. - BREDA		



OVERALL BLOCK DIAGRAM

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio		CURR. DATE :2009-08-14
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 1	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

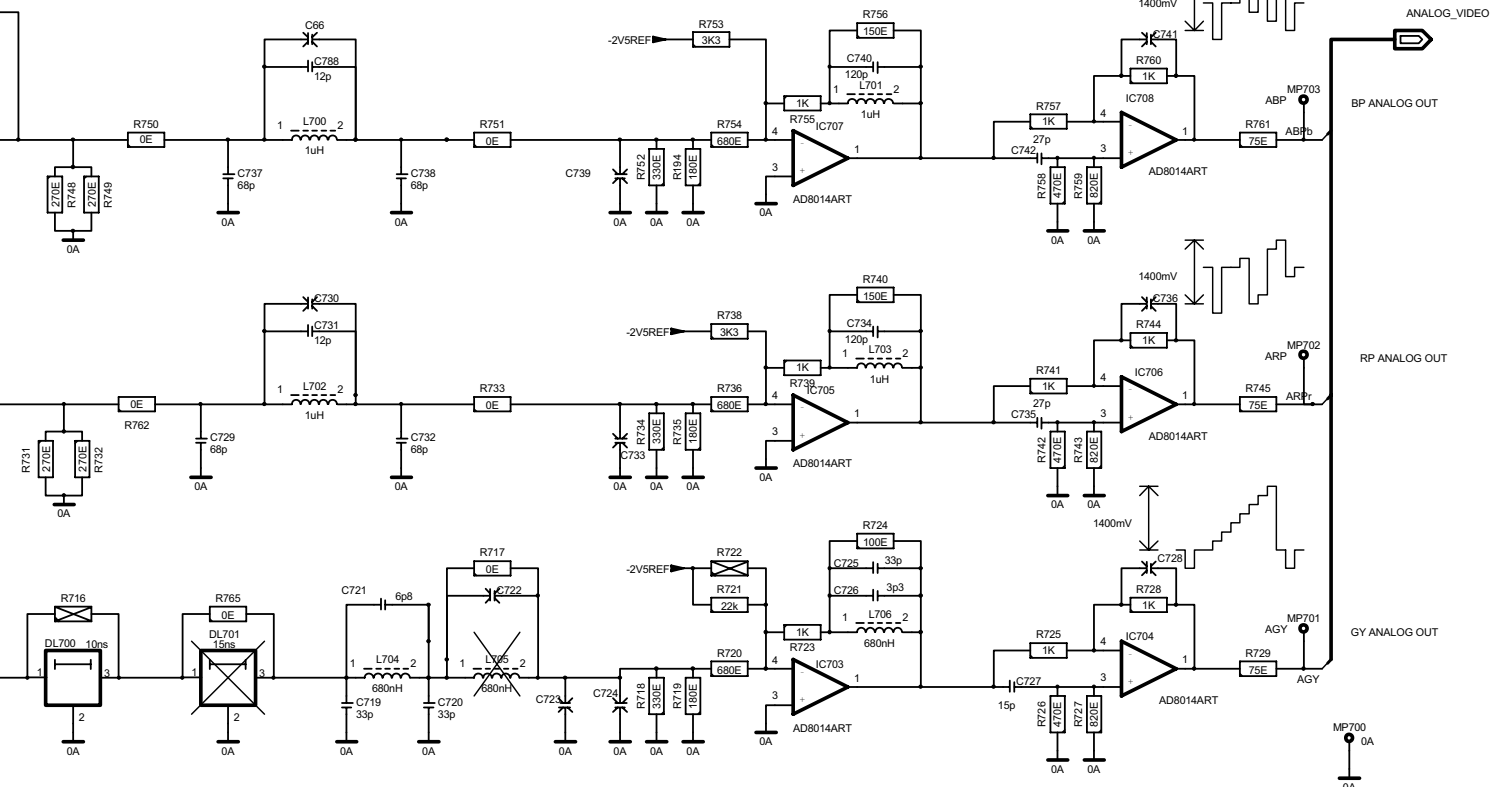
DA CONVERTER



Low Pass Filter:
Y = 30 MHz,
Pr = Pb = 15 MHz

DC shift +
Sinx/x correction

Group delay correction

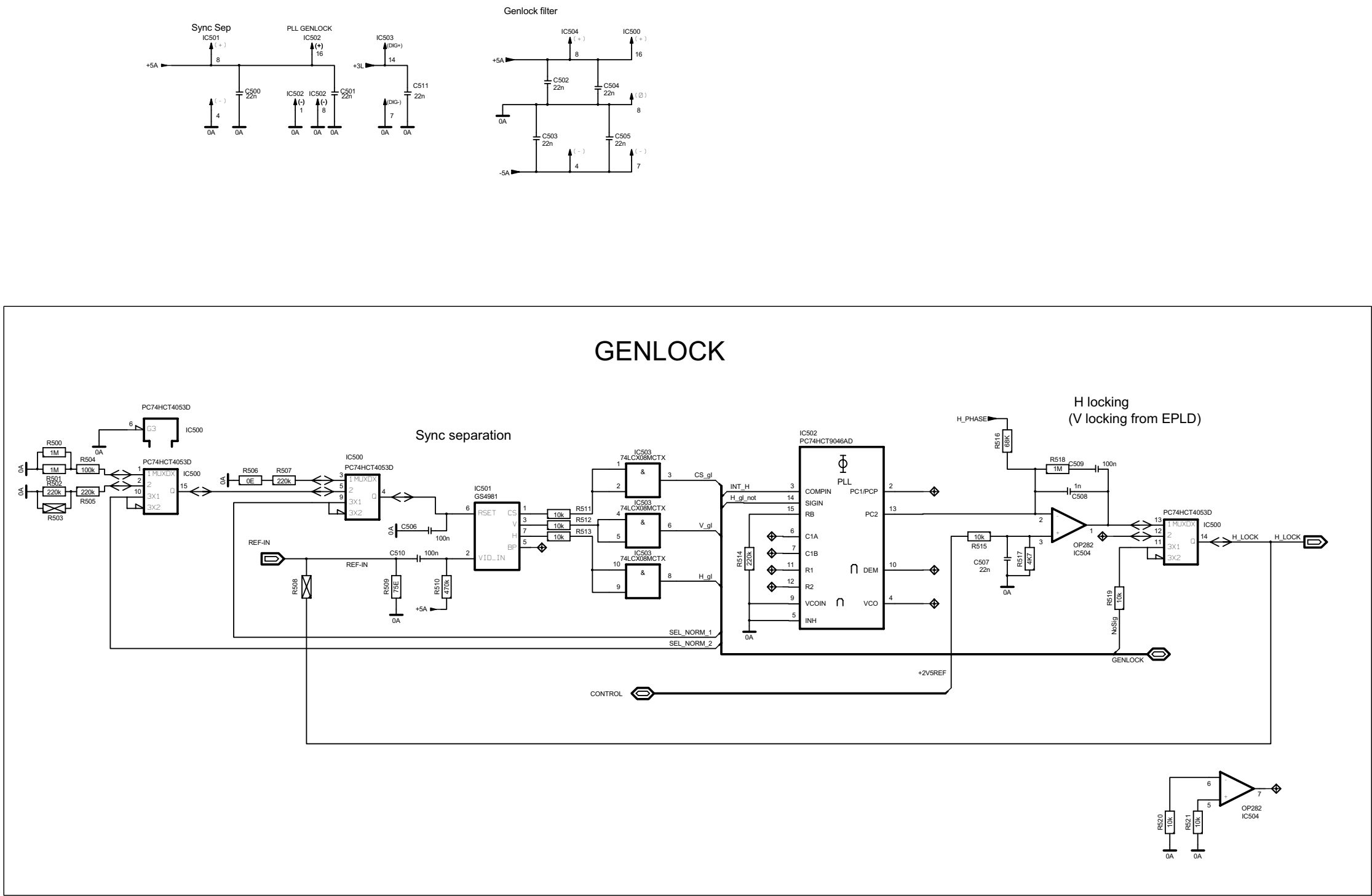


DAC SUPPLY

Dac output #700

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED	
ASS. NO. : 3922 406 54870	
ASS. NAME : DAC OUTPUT BOARD	
STATUS : 02	
PCB NO. : 3922 411 53053	
SHEET NAME : SHEET NAME	
I. Merodio	CURR. DATE :2009-08-14
CIRCUIT DIAGRAM	PREV. DATE :2009-08-13
15	SHEET 130 - 2
ORG. DATE : 2008-10-07	
GRASS VALLEY NEDERLAND B.V. - BREDA	

GENLOCK



GENLOCK #500

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED

ASS. NO. : 3922 406 54870

ASS. NAME : DAC OUTPUT BOARD

STATUS : 02

PCB NO. : 3922 411 53053

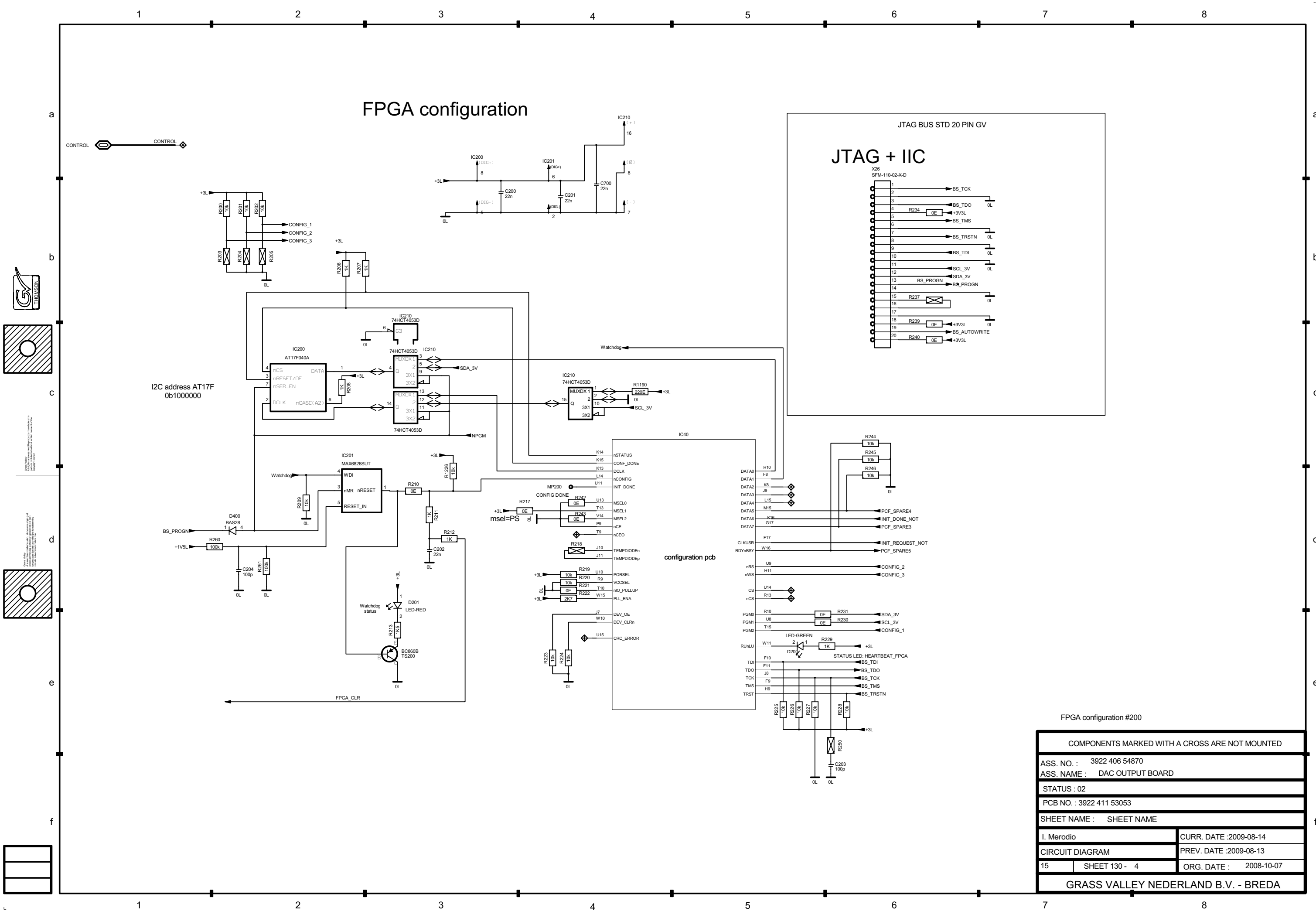
SHEET NAME : SHEET NAME

I. Merodio CURR. DATE :2009-08-14

CIRCUIT DIAGRAM PREV. DATE :2009-08-13

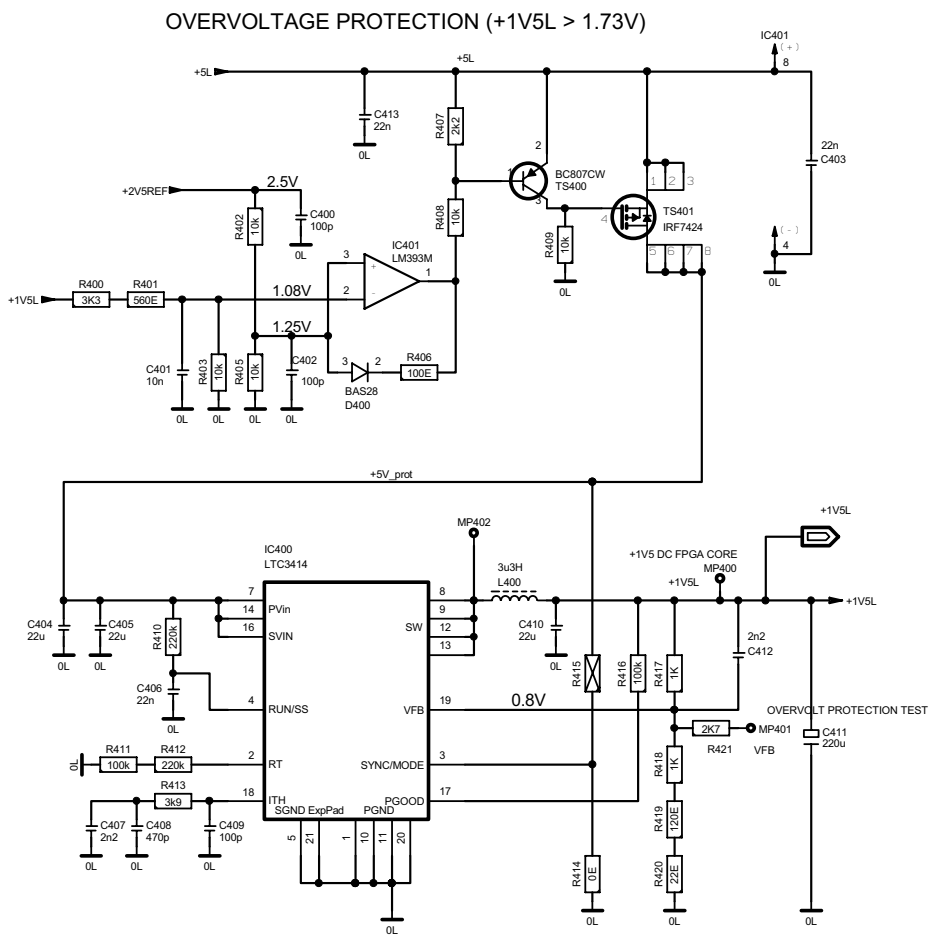
15 SHEET 130 - 3 ORG. DATE : 2008-10-07

GRASS VALLEY NEDERLAND B.V. - BREDA

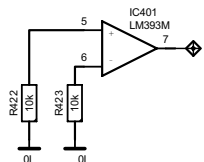


FPGA configuration #200		
COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio		CURR. DATE :2009-08-14
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 4	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

POWER STRATIX GX

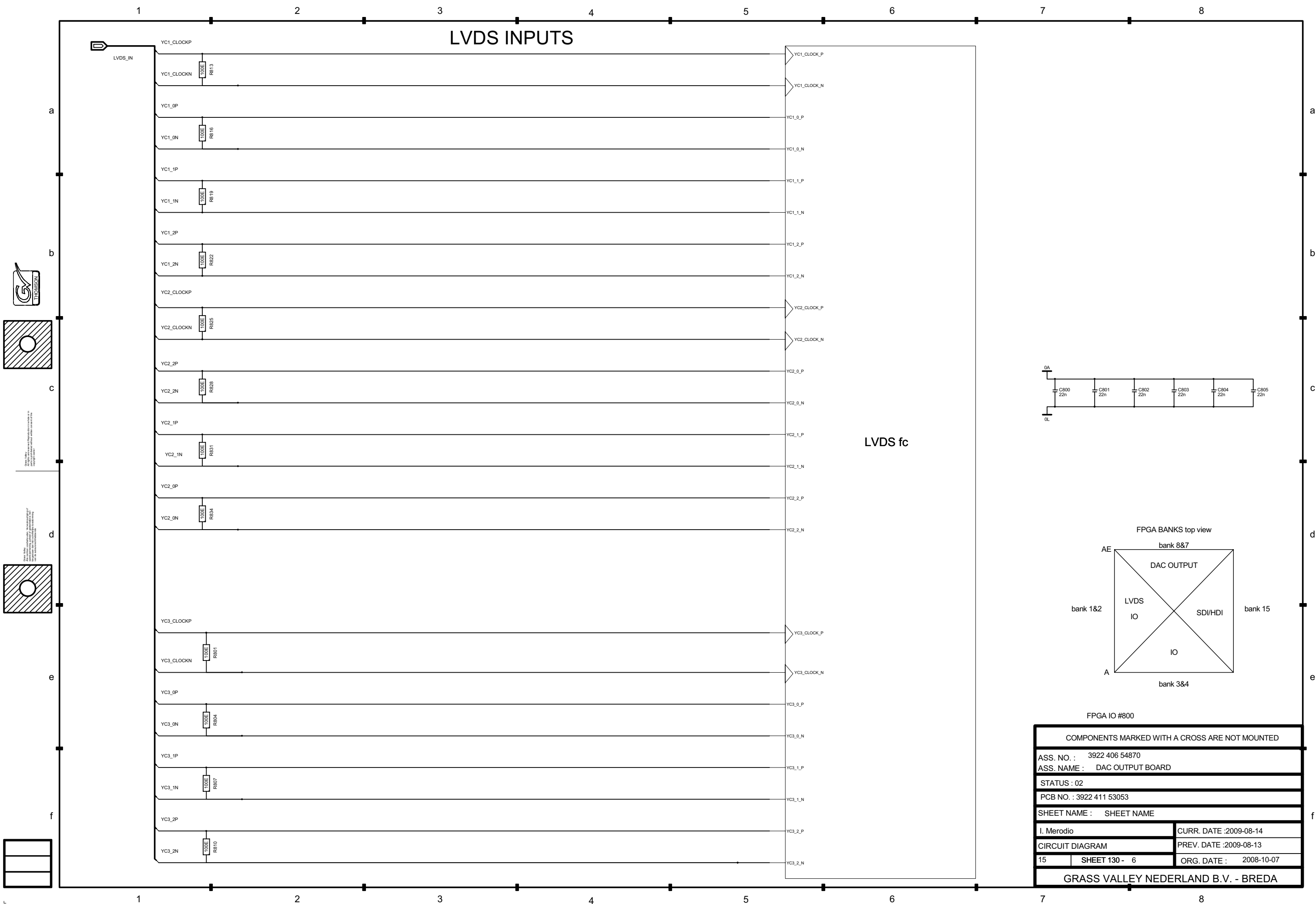


CONTROL



FPGA CORE POWER #400

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio		CURR. DATE :2009-08-14
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 5	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		



FPGA DAC CONTROL

The diagram illustrates the internal architecture of the FPGA DAC control system, showing the connection between various DAC blocks and their outputs.

DAC fc Block:

- CbB_DAC (0) to CbB_DAC (9):** Connected to DAC_bB<0> through DAC_bB<9>.
- CrR_DAC (0) to CrR_DAC (9):** Connected to DAC_rR<0> through DAC_rR<9>.
- YG_DAC (0) to YG_DAC (9):** Connected to DAC_Yg<0> through DAC_Yg<9>.
- BLANKN_DAC:** Connected to BLANKN_DAC.
- CLK_DAC:** Connected to CLK_DAC.
- SYNCN_DAC:** Connected to SYNCN_DAC.

DAC Output:

The DAC output is connected to the DAC pin, which is labeled as DAC.

FPGA BANKS top view:

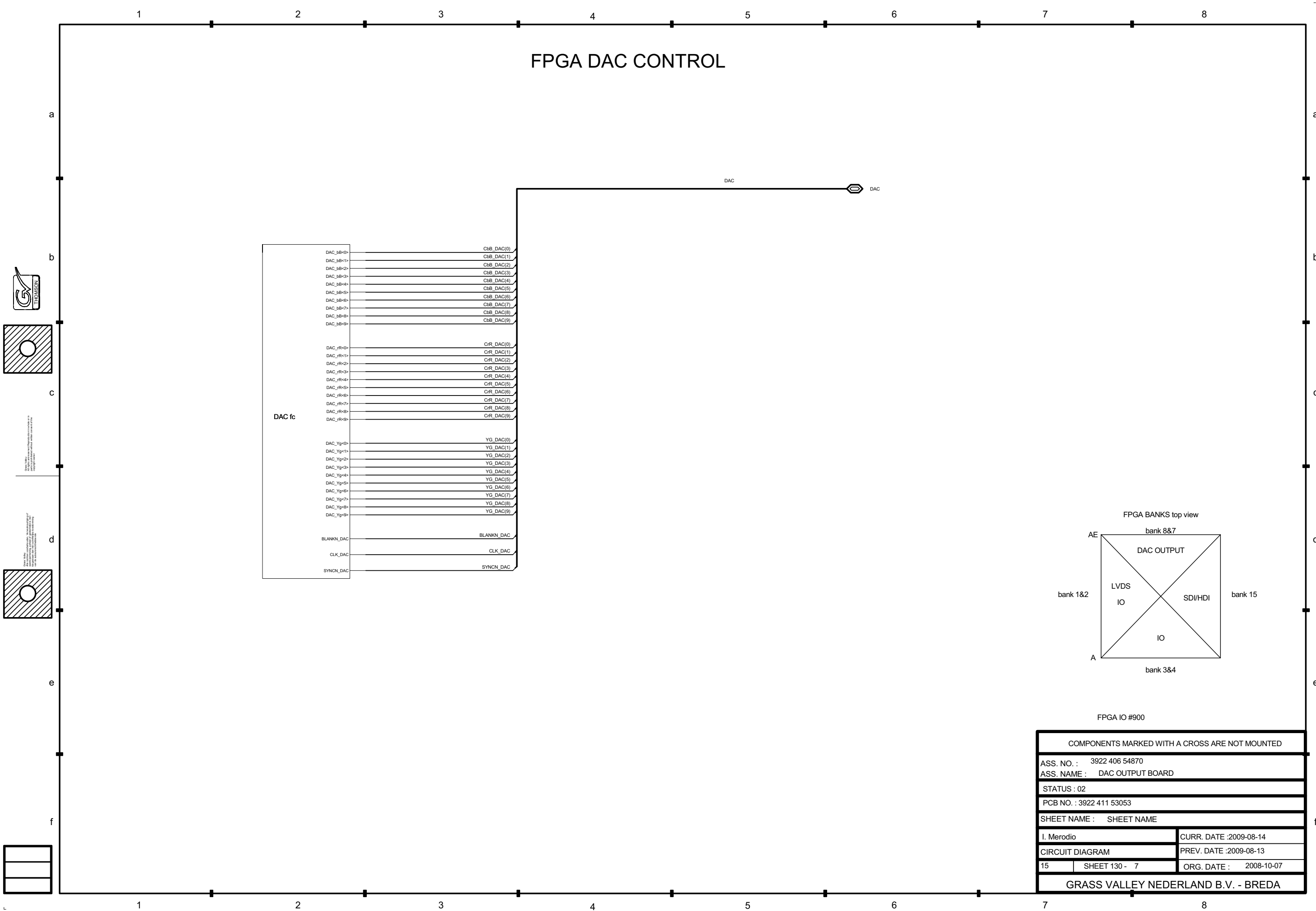
The top view shows the arrangement of FPGA banks and their connections:

- bank 8&7:** DAC OUTPUT
- bank 15:** SDI/HDI
- bank 3&4:** IO
- bank 1&2:** LVDS IO

FPGA IO #900:

The bottom right corner contains a table summarizing the components and status:

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio	CURR. DATE :2009-08-14	
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 7	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

[illegible][illegible]

FPGA DAC CONTROL

The diagram illustrates the internal architecture of the FPGA DAC control system, showing the connection between various DAC blocks and their outputs.

DAC fc Block:

- CbB_DAC (0) to CbB_DAC (9):** Connected to DAC_bB<0> through DAC_bB<9>.
- CrR_DAC (0) to CrR_DAC (9):** Connected to DAC_rR<0> through DAC_rR<9>.
- YG_DAC (0) to YG_DAC (9):** Connected to DAC_Yg<0> through DAC_Yg<9>.
- BLANKN_DAC:** Connected to BLANKN_DAC.
- CLK_DAC:** Connected to CLK_DAC.
- SYNCN_DAC:** Connected to SYNCN_DAC.

DAC Output:

The DAC output is connected to the DAC pin, which is labeled as DAC.

FPGA BANKS top view:

The top view shows the distribution of DAC outputs across the FPGA banks:

- bank 8&7:** DAC OUTPUT
- bank 15:** SDI/HDI
- bank 3&4:** IO
- bank 1&2:** LVDS IO

FPGA IO #900:

The following table provides details about the components and assembly information:

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio	CURR. DATE :2009-08-14	
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 7	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

FPGA DAC CONTROL

The diagram illustrates the internal architecture of the FPGA DAC control system, showing the connection between various DAC blocks and their outputs.

DAC fc Block:

- CbB_DAC (0) to CbB_DAC (9):** Connected to DAC_bB<0> through DAC_bB<9>.
- CrR_DAC (0) to CrR_DAC (9):** Connected to DAC_rR<0> through DAC_rR<9>.
- YG_DAC (0) to YG_DAC (9):** Connected to DAC_Yg<0> through DAC_Yg<9>.
- BLANKN_DAC:** Connected to BLANKN_DAC.
- CLK_DAC:** Connected to CLK_DAC.
- SYNCN_DAC:** Connected to SYNCN_DAC.

DAC Output:

The DAC output is connected to the DAC pin, which is labeled as DAC.

FPGA BANKS top view:

The top view shows the distribution of DAC outputs across the FPGA banks:

- bank 8&7:** DAC OUTPUT
- bank 15:** SDI/HDI
- bank 3&4:** IO
- bank 1&2:** LVDS IO

FPGA IO #900:

The bottom right corner contains a table summarizing the components and status:

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio	CURR. DATE :2009-08-14	
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 7	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

FPGA DAC CONTROL

The diagram illustrates the internal architecture of the FPGA DAC control system, showing the connection between various DAC blocks and their outputs.

DAC fc Block:

- CbB_DAC (0) to CbB_DAC (9):** Connected to DAC_bB<0> through DAC_bB<9>.
- CrR_DAC (0) to CrR_DAC (9):** Connected to DAC_rR<0> through DAC_rR<9>.
- YG_DAC (0) to YG_DAC (9):** Connected to DAC_Yg<0> through DAC_Yg<9>.
- BLANKN_DAC:** Connected to BLANKN_DAC.
- CLK_DAC:** Connected to CLK_DAC.
- SYNCN_DAC:** Connected to SYNCN_DAC.

DAC Output:

The DAC output is connected to the DAC pin, which is labeled as DAC.

FPGA BANKS top view:

The top view shows the distribution of DAC outputs across the FPGA banks:

- bank 8&7:** DAC OUTPUT
- bank 15:** SDI/HDI
- bank 3&4:** IO
- bank 1&2:** LVDS IO

FPGA IO #900:

The components are marked with a cross, indicating they are not mounted.

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio	CURR. DATE :2009-08-14	
CIRCUIT DIAGRAM		PREV. DATE :2009-08-13
15	SHEET 130 - 7	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

[illegible][illegible][illegible][illegible]

FPGA DAC CONTROL

The diagram illustrates the internal architecture of the FPGA DAC control system, showing connections between various DAC blocks and their outputs.

DAC fc Block:

- CbB_DAC (0) to CbB_DAC (9):** Connected to DAC_bB<0> through DAC_bB<9>.
- CrR_DAC (0) to CrR_DAC (9):** Connected to DAC_rR<0> through DAC_rR<9>.
- YG_DAC (0) to YG_DAC (9):** Connected to DAC_Yg<0> through DAC_Yg<9>.
- BLANKN_DAC:** Connected to BLANKN_DAC.
- CLK_DAC:** Connected to CLK_DAC.
- SYNCH_DAC:** Connected to SYNCH_DAC.

DAC Output:

The DAC output is connected to the DAC pin, which is labeled DAC.

FPGA BANKS top view:

The top view shows the arrangement of FPGA banks and IO pins:

- bank 8&7:** DAC OUTPUT
- bank 15:** SDI/HDI
- bank 3&4:** IO
- bank 1&2:** LVDS IO

FPGA IO #900:

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED

ASS. NO. : 3922 406 54870
ASS. NAME : DAC OUTPUT BOARD

STATUS : 02

PCB NO. : 3922 411 53053

SHEET NAME : SHEET NAME

I. Merodio
CIRCUIT DIAGRAM

Curr. DATE : 2009-08-14
Prev. DATE : 2009-08-13

15 | SHEET 130 - 7 | ORG. DATE : 2008-10-07

GRASS VALLEY NEDERLAND B.V. - BREDA

FPGA DAC CONTROL

The diagram illustrates the internal architecture of the FPGA DAC control system, showing connections between various DAC blocks and their outputs.

DAC fc Block:

- CbB_DAC (0) to CbB_DAC (9):** Connected to DAC_bB<0> through DAC_bB<9>.
- CrR_DAC (0) to CrR_DAC (9):** Connected to DAC_rR<0> through DAC_rR<9>.
- YG_DAC (0) to YG_DAC (9):** Connected to DAC_Yg<0> through DAC_Yg<9>.
- BLANKN_DAC:** Connected to BLANKN_DAC.
- CLK_DAC:** Connected to CLK_DAC.
- SYNCH_DAC:** Connected to SYNCH_DAC.

DAC Output:

The DAC output is connected to the DAC pin, which is labeled DAC.

FPGA BANKS top view:

The top view shows the arrangement of FPGA banks and IO pins:

- bank 8&7:** DAC OUTPUT
- bank 15:** SDI/HDI
- bank 3&4:** IO
- bank 1&2:** LVDS IO

FPGA IO #900:

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED

ASS. NO. : 3922 406 54870
ASS. NAME : DAC OUTPUT BOARD

STATUS : 02

PCB NO. : 3922 411 53053

SHEET NAME : SHEET NAME

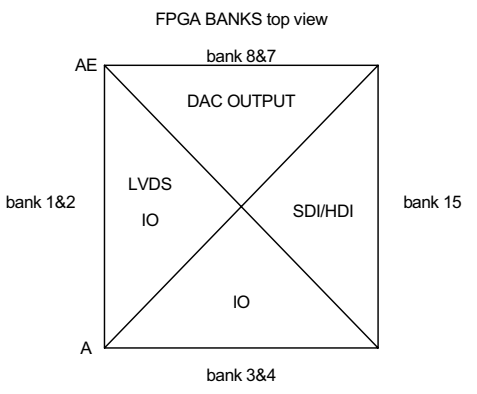
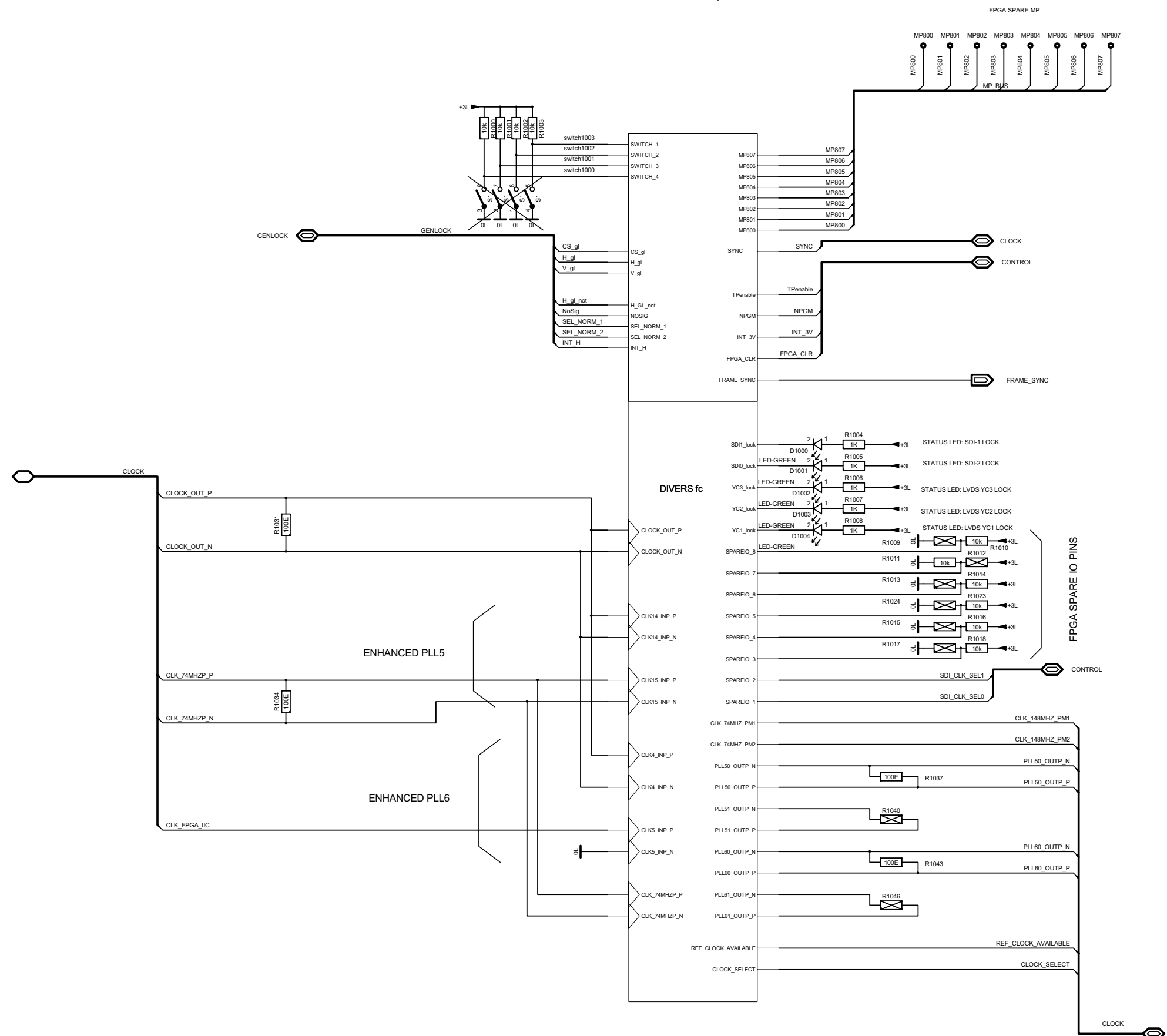
I. Merodio
CIRCUIT DIAGRAM

Curr. DATE : 2009-08-14
Prev. DATE : 2009-08-13

15 | SHEET 130 - 7 | Org. DATE : 2008-10-07

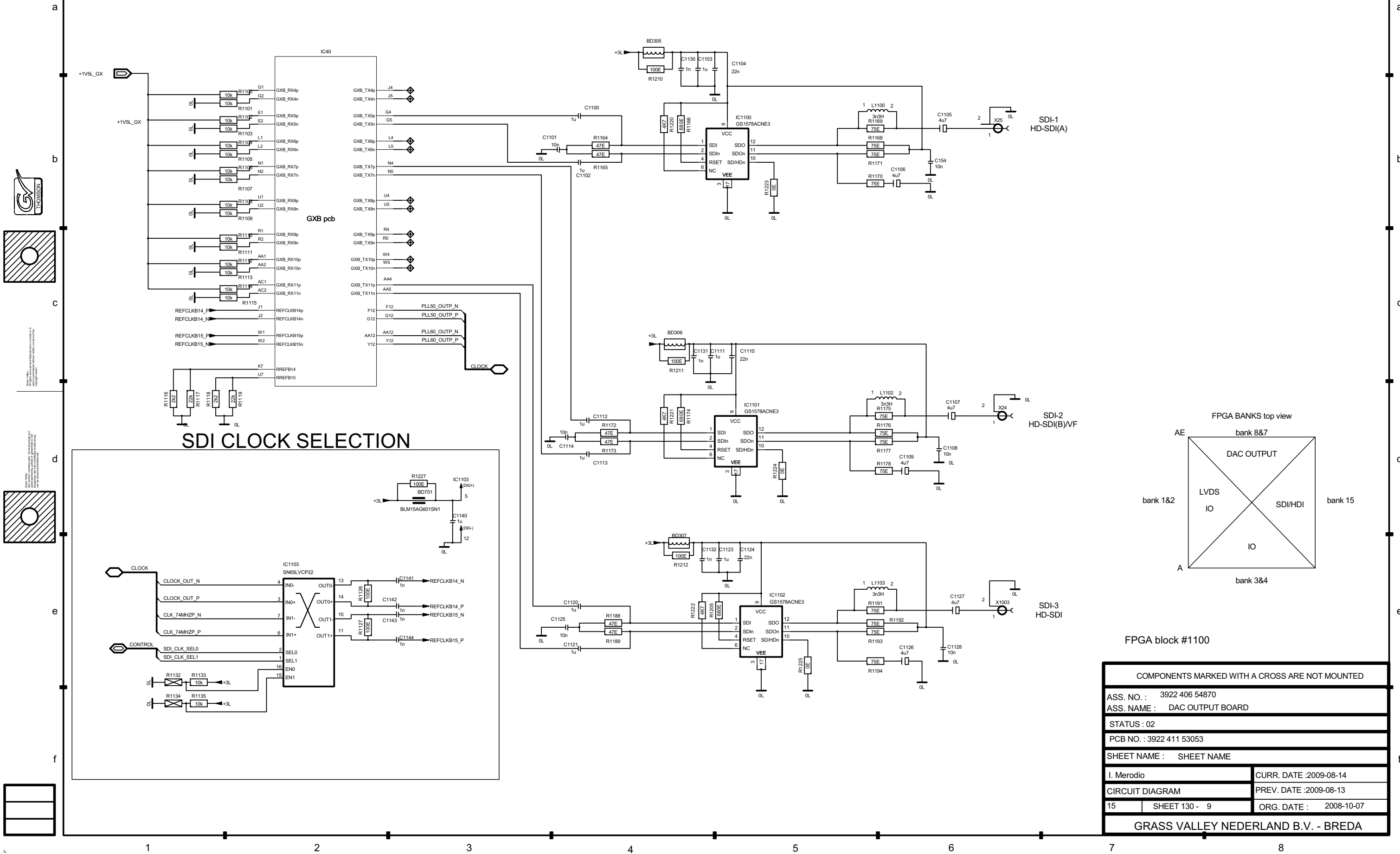
GRASS VALLEY NEDERLAND B.V. - BREDA

FPGA IO BANKS FOR GENLOCK, CLOCKS and DIVERS



FPGA IO #1000		
COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED		
ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio	CURR. DATE :2009-08-14	
CIRCUIT DIAGRAM	PREV. DATE :2009-08-13	
15	SHEET 130 - 8	ORG. DATE : 2008-10-07
GRASS VALLEY NEDERLAND B.V. - BREDA		

FPGA IO SDI/HDI CHANNELS



SDI CLOCK SELECTION

FPGA block #1100

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED

ASS. NO. : 3922 406 54870		
ASS. NAME : DAC OUTPUT BOARD		
STATUS : 02		
PCB NO. : 3922 411 53053		
SHEET NAME : SHEET NAME		
I. Merodio	CURR. DATE :2009-08-14	
CIRCUIT DIAGRAM	PREV. DATE :2009-08-13	
15	SHEET 130 - 9	ORG. DATE : 2008-10-07

GRASS VALLEY NEDERLAND B.V. - BREDA

FPGA POWER

FPGA POWER

FPGA POWER #300

COMPONENTS MARKED WITH A CROSS ARE NOT MOUNTED

ASS. NO. : 3922 406 54870

ASS. NAME : DAC OUTPUT BOARD

STATUS : 02

PCB NO. : 3922 411 53053

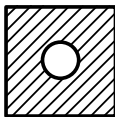
SHEET NAME : SHEET NAME

I. Merodio CURR. DATE :2009-08-14

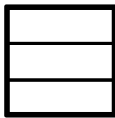
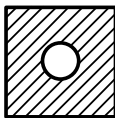
CIRCUIT DIAGRAM PREV. DATE :2009-08-13

15 SHEET 130 - 13 ORG. DATE : 2008-10-07

GRASS VALLEY NEDERLAND B.V. - BREDA



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