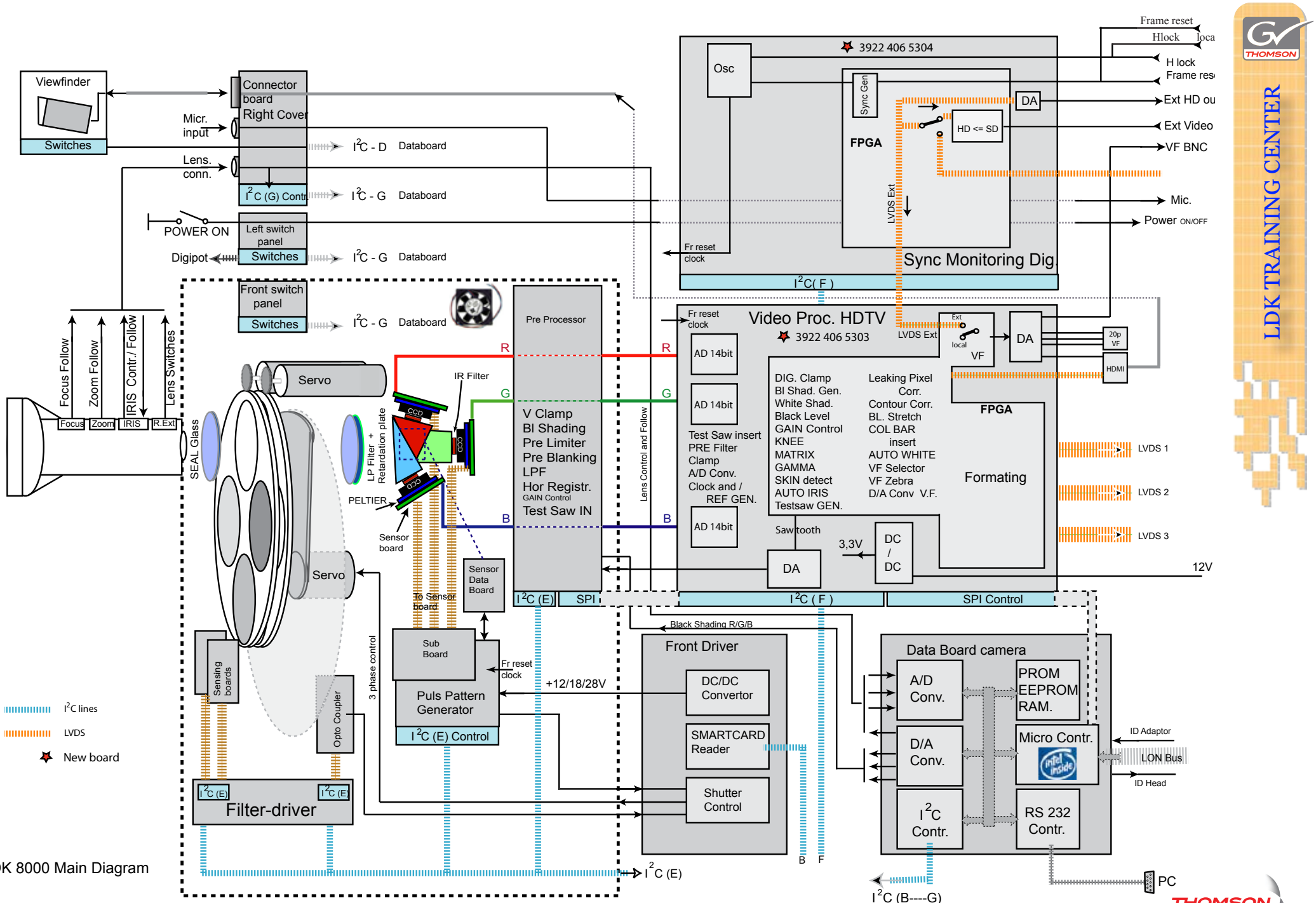
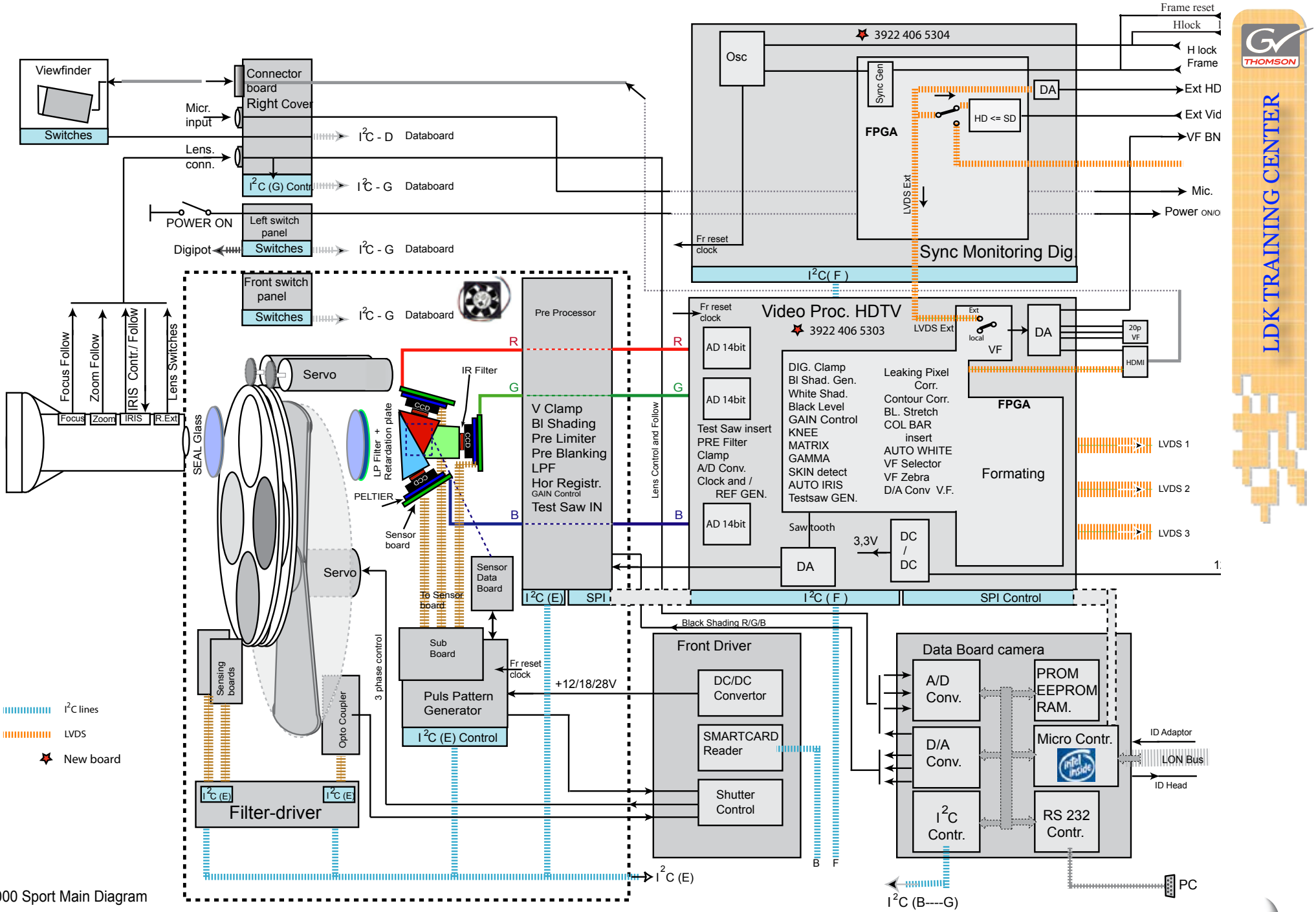
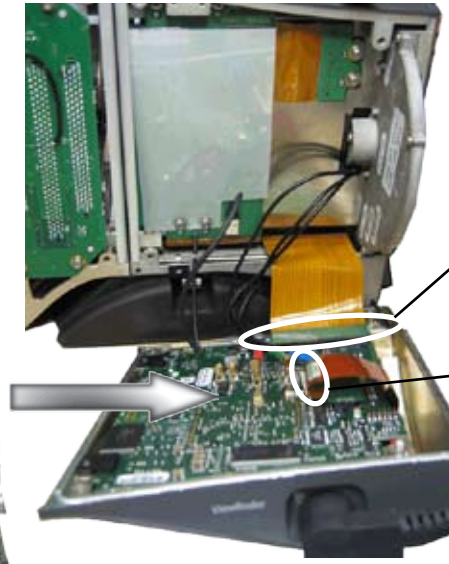

Viewfinder
Switches
Connector board
Right Cover
Micr. input
Lens. conn.
I²C - D
Databoard
I²C (G) Contr
I²C - G
Databoard
POWER ON
Left switch panel
Switches
Digipot
I²C - G
Databoard
Front switch panel
Switches
I²C - G
Databoard
Focus Follow
Zoom Follow
IRIS Contr./ Follow
Lens Switches
Focus
Zoom
IRIS
R.Ext
Servo
Servo
SEAL Glass
IR Filter
LP Filter + Retardation plate
CCD
PELTIER
Sensor board
Sensor Data Board
To Sensor board
Pre Processor
R
G
B
V Clamp
Bl Shading
Pre Limiter
Pre Blanking
LPF
Hor Registr.
GAIN Control
Test Saw IN
Lens Control and Follow
I²C (E)
SPI
Osc
3922 406 5304
Sync Gen
FPGA
HD <= SD
DA
LVDS Ext
Fr reset clock
Sync Monitoring Dig
I²C(F)
Frame reset
Hlock
H lock
Frame res
Ext HD ou
Ext Video
VF BNC
Mic.
Power ON/OFF
Video Proc. HDTV
3922 406 5303
Fr reset clock
AD 14bit
AD 14bit
AD 14bit
Test Saw insert
PRE Filter
Clamp
A/D Conv.
Clock and / REF GEN.
DIG. Clamp
Bl Shad. Gen.
White Shad.
Black Level
GAIN Control
KNEE
MATRIX
GAMMA
SKIN detect
AUTO IRIS
Testsaw GEN.
Leaking Pixel Corr.
Contour Corr.
BL. Stretch
COL BAR insert
AUTO WHITE
VF Selector
VF Zebra
D/A Conv V.F.
FPGA
Formating
Ext
local
VF
DA
20p VF
HDMI
LVDS 1
LVDS 2
LVDS 3
Sawtooth
DA
3,3V
DC / DC
12V
I²C (F)
SPI Control
Black Shading R/G/B
Front Driver
DC/DC Convertor
SMARTCARD Reader
Shutter Control
B
F
Data Board camera
A/D Conv.
D/A Conv.
I²C Contr.
PROM EEPROM RAM.
Micro Contr.
RS 232 Contr.
ID Adaptor
LON Bus
ID Head
PC
I²C (B----G)
Sub Board
Puls Pattern Generator
I²C (E) Control
Fr reset clock
+12/18/28V
3 phase control
Sensing boards
Opto Coupler
Filter-driver
I²C (E)
I²C (E)
I²C (E)
I²C lines
LVDS
New board
LDK 8000 Main Diagram
HD Heads
LDK TRAINING CENTER
THOMSON
images & beyond

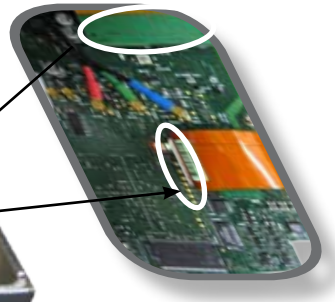


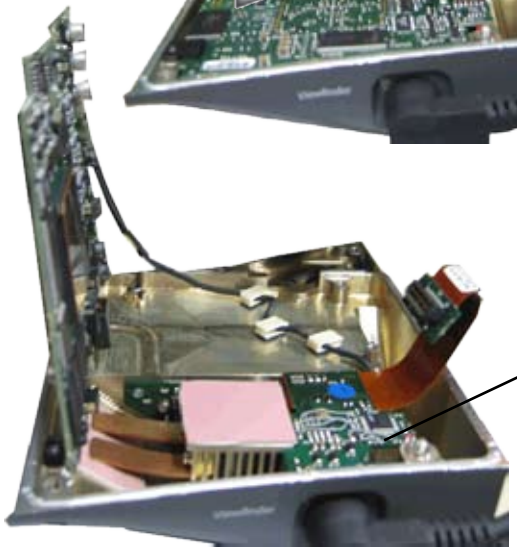
LDK 8000 Sport Main Diagram

HD Heads

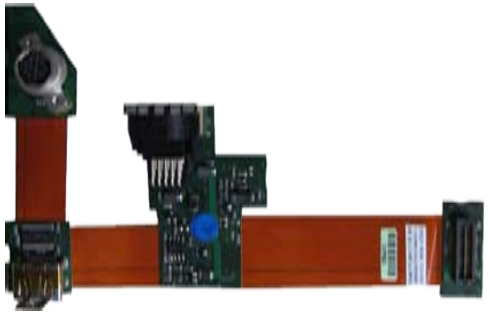


Remove connectors





DVP Board HDTV
3922 406 53030



Conn board Right Cover
3922 406 53101

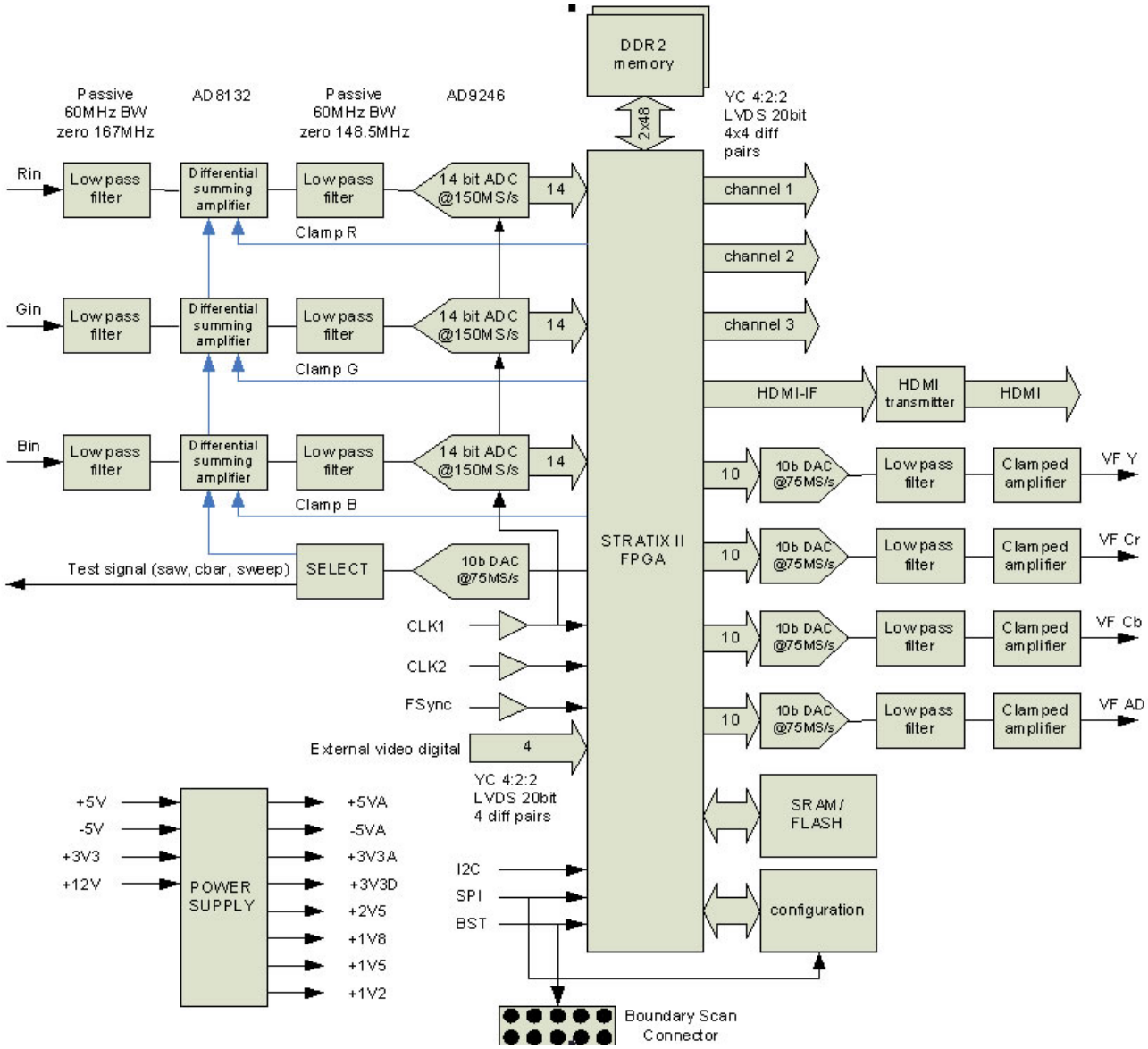
Changed
LDK 6000 => 8000

Digital Video processor LDK 8000

The Digital Video Processor LDK8000 board digitizes and processes camera video signals and deliver these signals to subsequent system parts for transmission or recording.
Also a separate video signal to be displayed on a viewfinder needs to be derived.

Main functions of the board are:

1. Digitize RGB video signal from pre-processor at 14bit precision and maximum 148.5MSPS.
2. Accept a digital external video signal from the Sync Mon Dig board to be displayed in the viewfinder.
3. Process video signal (FPGA)
   Corrections for analogue phenom ena origination in front.
   Format conversion like progressive segmented frame conversion and 3:2 pull down conversion.
   “Asic a2” and “Asic b2” processing viewfinder signal processing.
4. Generate analogue YCrCb output signals for a viewfinder with analogue interface.
5. Generate digital YCrCb output signals for a viewfinder with HDMI interface.
6. Generate 3 channels of lvds formatted digital interface to the DAC output board.



Sync Monitoring board LDK 8000

3922 406 53041

As the VF-functionality will move to the DVP-board,
also this board needs a re-design.
The board will have two main functions:
Master sync generator.

This board distributes the clock pulses for the camera to the DVP-board, the front module and the DAC-output board (adapter). The signals H-LOCK and FRAME RESET coming from the adapter are used to synchronize the camera with the base station or the Ext Ref input signal.
The frequency of the clock pulses depends on the video standard in which the camera is operating (37,125, 55 MHz or 74.25 MHz).

Frame rate converter for the external signal.

As it takes too much interconnection for the DAC-output board to do the up-conversion of the (SD) Ext VF signal, this up-conversion is implemented on this board.

The analog SD-signal enters the camera head and is converted to an (HD-) LVDS signal for the DVP-board.
At the DVP-board the signal is mixed/switched with the local VF-signal.
The board also has a LVDS input for the external signal.
This is the EXT input when a 10Ge fiber adapter is being used (future).In this case the signal can be transmitted directly to the DVP-board.

Another reason to choose for this function on this board and not in the adapter is the compatibility with the old triax-adapter

The VF-functionality
(inserting text, cadres, switching, DA conversion etc)
is transferred to the DVP-board.
The FPGA for this new Sync-monitoring can be cheaper as it has less functionality and also the dissipation of this board will drop.