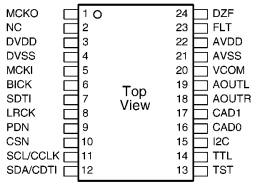
5.17 IC BLOCK DIAGRAMS

■ AK4363VF-X [ASAHI KASEI]
(Stereo CMOS D/A Converter and Phase Locked Loop)

Pin Layout

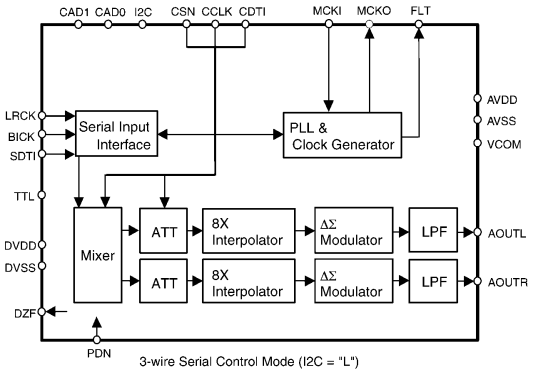


Pin/Function

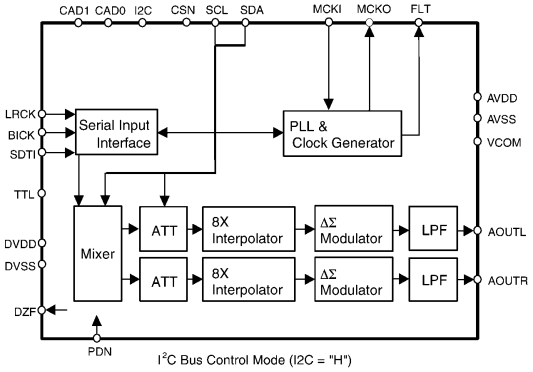
No.	Pin Name	I/O	Description
1	MCKO	O	Master Clock Output Pin EXT = "0" : System clock is output from PLL circuit (PLL mode), EXT = "1" : Same frequency as MCKI is output (External mode)
2	NC	-	No Connect Nothing should be connected externally to this pin.
3	DVDD	-	Digital Power Supply Pin, +2.7~ +5.5V
4	DVSS	-	Digital Ground Pin, 0V
5	MCKI	I	System Clock Input Pin EXT = "0" : 27MHz (PLL mode), EXT = "1" : Other frequency (External mode)
6	BICK	I	Serial Data Clock Pin
7	SDTI	I	Serial Data Input Pin
8	LRCK	I	Serial Input Channel Clock Pin
9	PDN	I	Power-Down Pin When "L", the circuit is in power-down mode. The AK4363 should always be reset upon power-up.
10	CSN	I	Chip Select Pin at 3-wire Serial control mode This pin should be connected to DVDD at I²C Bus control mode.
11	SCL	I	Control Clock Pin at I²C bus control mode
	CCLK	I	Control Clock Pin at 3-wire serial control mode
12	SDA	I/O	Control Data Input/Output Pin at I²C Bus control mode
	CDTI	I	Control Data Input Pin at 3-wire serial control mode
13	TST	I	Test pin This pin should be connected to DVSS.
14	TTL	I	Digital Input Level Select Pin "L" : CMOS, "H" : TTL
15	I2C	I	Control Mode Select Pin "L" : 3-wire Serial, "H" : I²C Bus
16	CAD0	I	Chip Address Select 0 Pin
17	CAD1	I	Chip Address Select 1 Pin
18	AOUTR	O	Rch Analog Output Pin
19	AOUTL	O	Lch Analog Output Pin
20	VCOM	O	Common Voltage Output Pin, AVDD/2 Used for analog common voltage. Large external capacitor is used to reduce power supply noise.
21	AVSS	-	Analog Ground Pin
22	AVDD	-	Analog Power Supply Pin
23	FLT	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resister and one capacitor in series. (See"SYSTEM DESIGN".)
24	DZF	O	Zero Input Detect Pin When SDTI follows a total 8192 LRCK cycles with "0" input data or RSTN = "0", this pin goes to "H".

Note: No input pins should be left floating.

Block Diagram

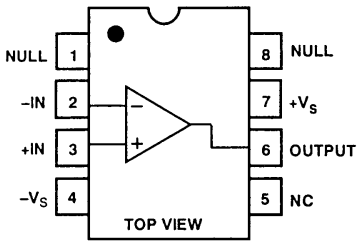


3-wire Serial Control Mode (I2C = "L")



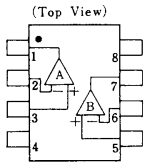
I²C Bus Control Mode (I2C = "H")

■ AD817AR-X [ANALOG DEVICES]
(Hi-Speed Low Power Op.Amp)



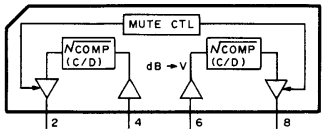
NC = NOT CONNECTED

■ BA10393F-XE [ROHM]
(Dual Comparator)



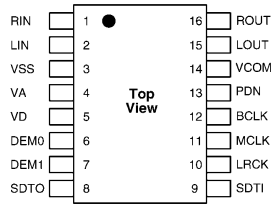
Pin
1. A OUTPUT
2. A–INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B–INPUT
7. B OUTPUT
8. V⁺

■ BA6138F-X [ROHM]
(1/2 square-law compression amplifiers)



■ AK4552VT-X [ASAHI KASEI]
(Degital Audio A/D & D/A Converter)

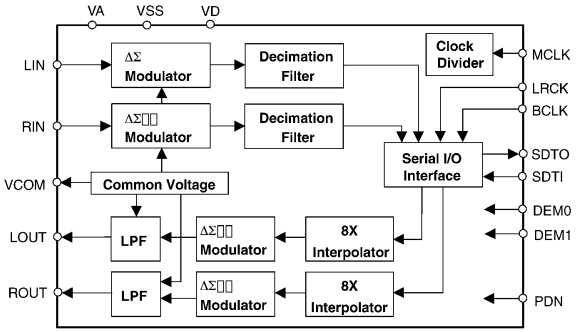
Pin Layout



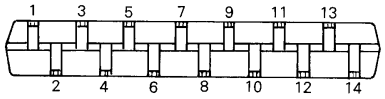
Pin/Function

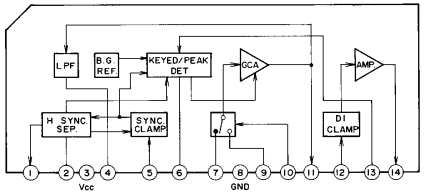
No.	Pin Name	I/O	Function
1	RIN	I	Rch Analog Input Pin
2	LIN	I	Lch Analog Input Pin
3	VSS	-	Ground Pin
4	VA	-	Analog Power Supply Pin
5	VD	-	Digital Power Supply Pin
6	DEM0	I	De-emphasis Control Pin
7	DEM1	I	De-emphasis Control Pin
8	SDTO	O	Audio Serial Data Output Pin
9	SDTI	I	Audio Serial Data Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	MCLK	I	Master Clock Input Pin
12	BCLK	I	Audio Serial Data Clock Pin
13	PDN	I	Power-Down & Reset Mode Pin "L": Power-down and Reset, "H": Normal operation
14	VCOM	O	Common Voltage Output Pin, 0.45 x VA
15	LOUT	O	Lch Analog Output Pin
16	ROUT	O	Rch Analog Output Pin

Block Diagram

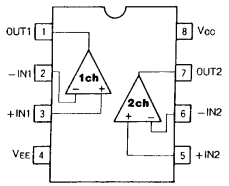


■ AN3916-/LF/ [MATSUSHITA]
(Video AGC)

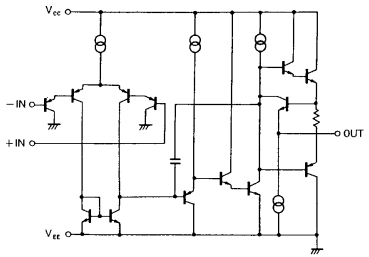




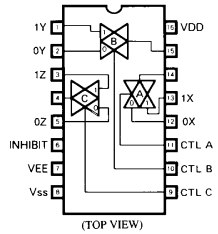
■ BA10358F-XE [ROHM]
(Dual Ground Sense Op.Amp)



(Top View)



■ CD4053BPW-X [RCA]
(Triple 2 Channel Analog Multiplexers/Demultiplexers)

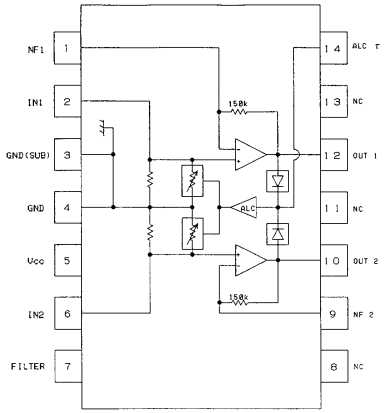


TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL
INHIBIT	C	B	A	4053BP 4053BF
L	L	L	L	0X, 0Y, 0Z
L	L	L	H	1X, 0Y,0Z
L	L	H	L	0X, 1Y, 0Z
L	L	H	H	1X, 1Y, 0Z
L	H	L	L	0X, 0Y, 1Z
L	H	L	H	1X, 0Y, 1Z
L	H	H	L	0X, 1Y, 1Z
L	H	H	H	1X, 1Y, 1Z
H	*	*	*	NOTE

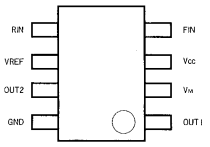
* Don't Care.

■ BA3314F-X [ROHM]
(Dual Pre-Amp. for Audio Signal)

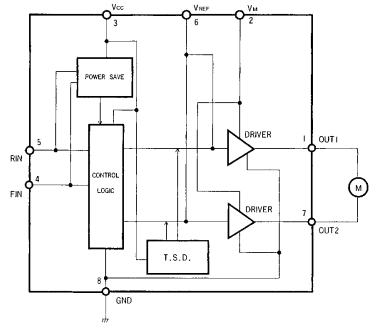


(Top View)

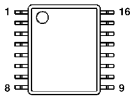
■ BA6417F-X [ROHM]
(Reversible Motor Driver)



Top view

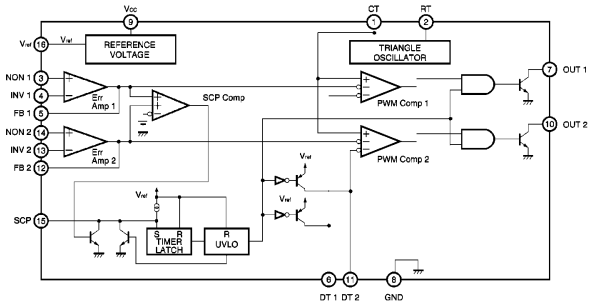


■ BA9743AFV-X [ROHM]
(2-channel Switching Regulator Controller)

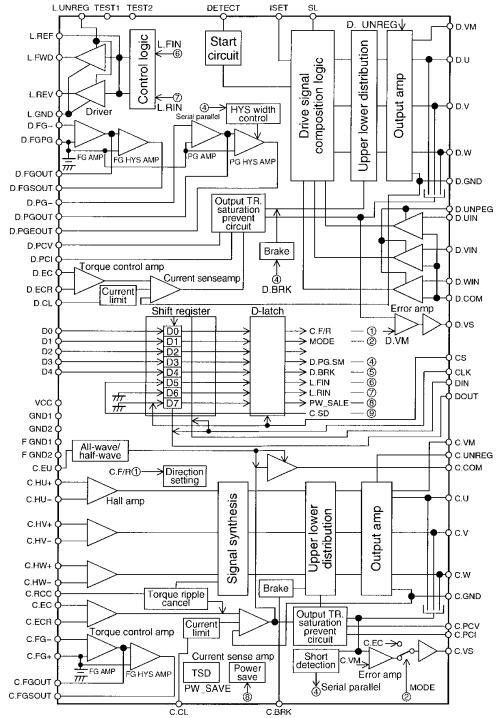


(Top View)

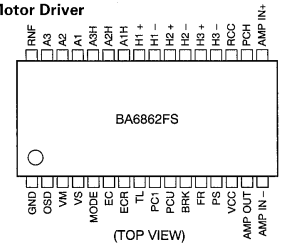
Block Diagram



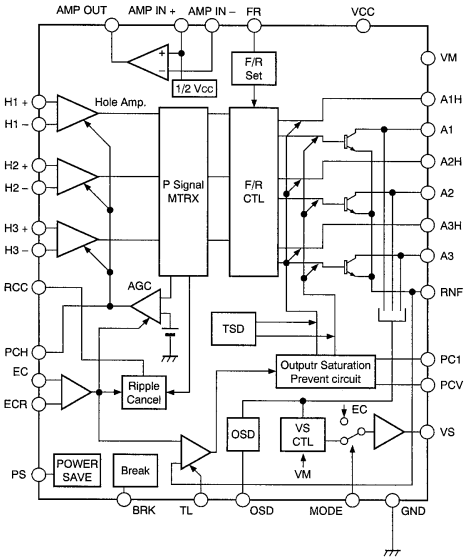
■ BA6865KV [ROHM]
(Motor Driver Controller)



■ BA6862FS-X [ROHM]
(Motor Driver

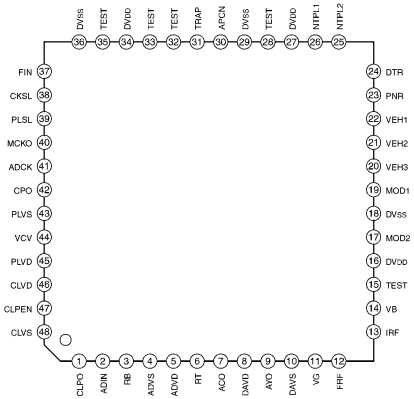


(TOP VIEW)

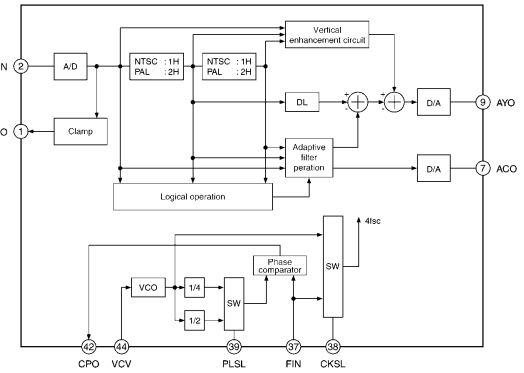


Pin No.	Symbol	Function
1	GND	GND
2	OSD	Output detect for short circuit
3	VM	Power source for motor drive
4	VS	Control for motor drive
5	MODE	Current/Voltage switching
6	EC	Torque control
7	ECR	Torque reference
8	TL	Torque limited
9	PCI	Output saturation prevent level (low level)
10	PCV	Output saturation prevent level (high level)
11	BRK	Break input H : Break L : Movement
12	FR	Foward/Reverse CTL input
13	PS	Power save H : Stand-by L : Movement
14	VCC	
15	AMP OUT	Amplifire output
16	AMP IN –	Amplifire input (–)
17	AMP IN +	Amplifire input (+)
18	PCH	Hole amp, AGC phase compareter
19	RCC	Ripple cancel
20	H3 –	Hole signal input
21	H3 +	Hole signal input
22	H2 –	Hole signal input
23	H2 +	Hole signal input
24	H1 –	Hole signal input
25	H1 +	Hole signal input
26	A1H	Pre motor drive output
27	A2H	Pre motor drive output
28	A3H	Pre motor drive output
29	A1	Motor drive output
30	A2	Motor drive output
31	A3	Motor drive output
32	RNF	GND for motor drive

■ CXD2064Q [SONY]
(DIGITAL COM FILTER (NTSC/PAL))



(Top View)

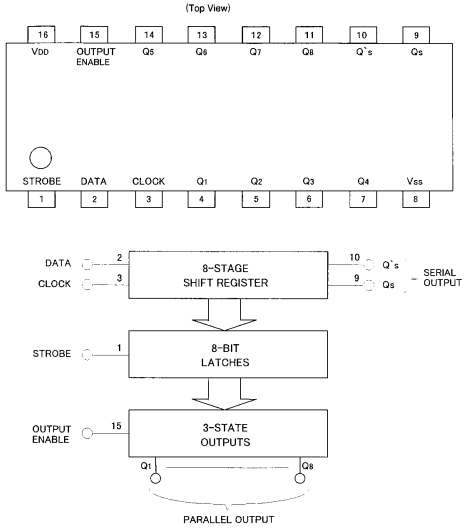


Pin Description

Pin No.	Symbol	I/O	Description
1	CLPO	O	Internal clamp circuit current output. Connect to ADIN when using the internal clamp. Leave this pin open when not in use.
2	ADIN	I	Comb filter analog input (A/D converter input).
3	RB	O	Reference bottom voltage for the A/D converter (0.52V typ.).
4	ADVS	—	A/D converter analog ground.
5	ADVD	—	A/D converter analog power supply. (5.0V)
6	RT	O	Reference top voltage for the A/D converter (2.60V typ.).
7	ACO	O	Analog chroma signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
8	DAVD	—	D/A converter analog power supply. (5.0V)
9	AYO	O	Analog luminance signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
10	DAVS	—	D/A converter analog ground.
11	VG	O	D/A converter related pin. Connect a capacitor of approximately 0.1µF between this pin and the analog power supply (DAVD).
12	VRF	I	Sets the full-scale value of the Y and C-channel D/A converter output signal.
13	IRF	O	Connect a resistor of "16R" (16 times the output resistor "R" of the D/A converter).
14	VB	O	D/A converter related pin. Connect to the analog ground (DAVS) via a capacitor of approximately 0.1µF.
15	TEST	I	Test pin. Normally fix to "Low".
16	DV_{DD}	—	Digital power supply. (5.0V)
18	DV_{SS}	—	Digital ground.
17	MOD2	I	Y/C separation mode setting. MOD2 L L Adaptive processing mode; H L BPF separation mode; H H Through mode
19	MOD1	I	
20	VEH3	I	Vertical enhancement setting. Can be set in 8 stages from VEH3 VEH2 VEH1: LLL (off) to HHH (max.)
21	VEH2	I	
22	VEH1	I	
23	PNR	I	L: NTSC/H: PAL, M-PAL, N-PAL
24	DTR	I	Normally fix to "Low".
25	NTPL2	I	NTSC/PAL/M-PAL/N-PAL mode setting. NTPL2 NTPL1 L L NTSC; L H PAL; H L M-PAL; H H N-PAL
26	NTPL1	I	
27	DV_{DD}	—	Digital power supply. (5.0V)

Pin No.	Symbol	I/O	Description
28	TEST	I	Test pin. Normally fix to "Low".
29	DV_{SS}	—	Digital ground.
30	APCN	I	Horizontal aperture correction circuit setting. Low: Off, High: On.
31	TRAP	I	Trap filter setting. Low: Off, High: On.
32	TEST	I	Test pin. Normally open or fix to "Low".
33	TEST	I	Test pin. Normally open or fix to "Low".
34	DV_{DD}	—	Digital power supply. (5.0V)
35	TEST	I	Test pin. Normally open or fix to "Low".
36	DV_{SS}	—	Digital ground.
37	FIN	I	Clock input. Input the burst-locked fsc (2fsc) when using the internal PLL. Input the burst-locked 4fsc when not using the internal PLL.
38	CKSL	I	PLL control. Low: The internal PLL is not used. The clock (4fsc) which is input to FIN is supplied internally. High: The internal PLL is used. VCO oscillation output 4fsc clock is supplied internally.
39	PLSL	I	Selects the clock input to FIN. Low: fsc, High: 2fsc. When inputting 4fsc to FIN (when not using the internal PLL), this pin may be set to either "Low" or "High".
40	MCKO	O	Clock (4fsc) output.
41	ADCK	I	Clock input for A/D converter. Normally connect to MCKO.
42	CPO	O	PLL phase comparator output. Leave open when not using the PLL.
43	PLVS	—	PLL analog ground.
44	VCV	I	VCO control voltage input. Connect to PLVS when not using the PLL.
45	PLVD	—	PLL analog power supply. (5.0V)
46	CLVD	—	Clamp D/A converter analog power supply. (5.0V)
47	CLPEN	I	Clamp circuit enable pin. Low: Clamp on, High: Clamp off.
48	CLVS	—	Clamp D/A converter analog ground.

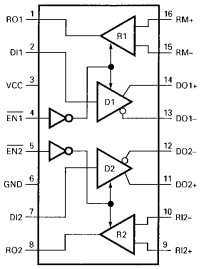
■ BU4094BCFV-X [ROHM]
(8-Stage Shift/Store Register)



■ DS8922M-X [NATIONAL SEMICONDUCTOR]
(RS-422 Dual Differential Line Driver and Receiver Pairs)

Connection Diagrams

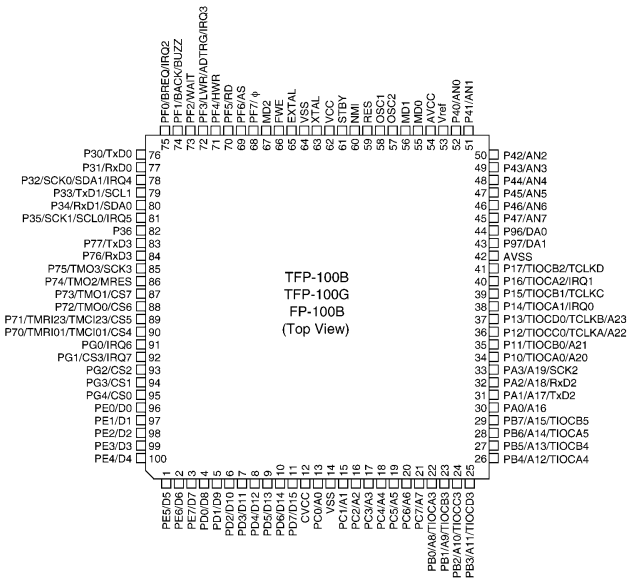
DS8922A Dual-In-Line



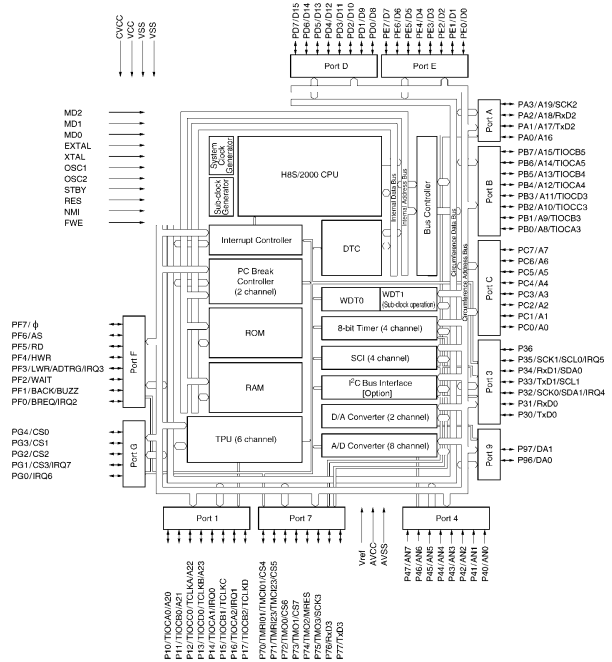
Top View

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

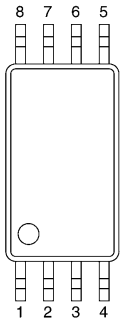
■ HD64F2238RFA13 [HITACHI]
(16-Bit Single Chip Micro Computer)



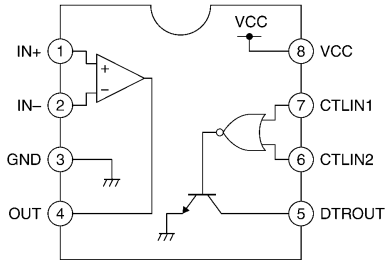
Block diagram



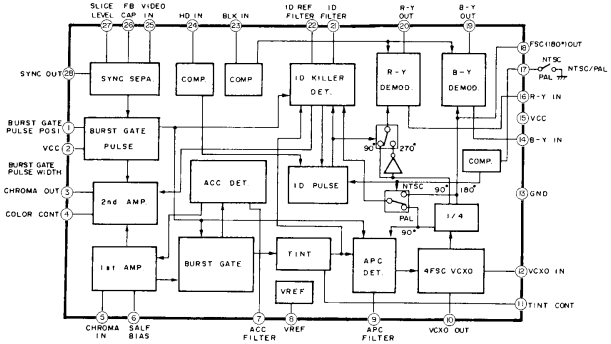
■ JCY0136-X [ROHM]
(High frequency operational amplifier for DVC)



Block diagram

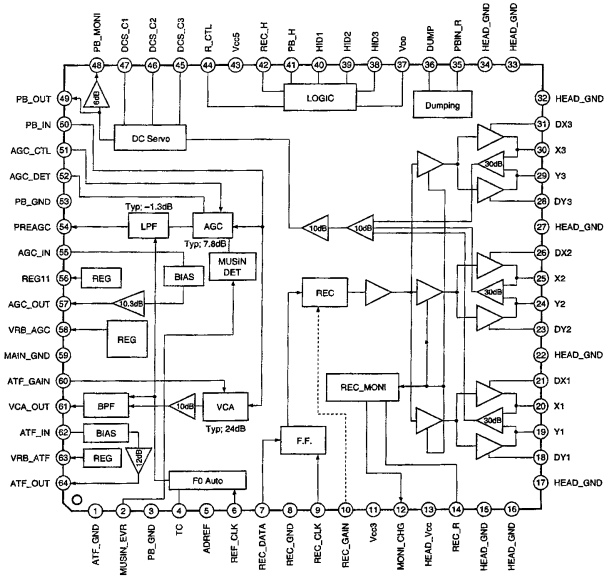


■ M51271FP-X [MITSUBISHI]
(Component Decoder)



■ JCY0132 [SONY]
(REC/PLAY amplifier for digital VCR)

Block diagram



Pin description

Pin No.	Pin name	Description	Pin No.	Pin name	Description
1	ATF_GND	Ground terminal	36	DUMP	HEAD resonance control terminal at playback mode
2	MUSIN_EVR	EVR terminal for non-signal detection level adjustment of AGC circuit	37	VDD	VDD power supply terminal
3	PB_GND	Ground terminal	38	HID3	Mode control terminal, channel select of playback amplifier and control of recording current measurement circuit
4	TC	Time constant terminal for F0 auto PLL circuit	39	HID2	Mode control terminal, channel select of recording/playback amplifier
5	ADREF	ADREF power supply terminal ADREF	40	HID1	Mode control terminal, channel select of recording/playback amplifier
6	REF_CLK	Reference clock input terminal for F0 auto PLL	41	PB_H	Mode control terminal, ON/OFF of playback circuit
7	REC_DATA	REC DATA input terminal	42	REC_H	Mode control terminal, ON/OFF of recording circuit
8	REC_GND	Ground terminal	43	Vcc5	Vcc5 power supply terminal
9	REC_CLK	REC CLOCK input terminal	44	R_CTL	Mode control terminal, ON/OFF of recording current output
10	REC_GAIN	Adjusting terminal for recoding current	45	DCS_C3	Time constant terminal for DC servo circuit
11	Vcc3	Vcc3 power supply terminal	46	DCS_C2	Time constant terminal for DC servo circuit
12	MONI_CHG	Monitor terminal for recording current output level : REC mode, Quick charge pulse input terminal of TC terminal : PB mode	47	DCS_C1	Time constant terminal for DC servo circuit
13	HEAD_Vcc	Power supply terminal of R/P amplifier section	48	PB_MONI	PB amplifier monitor terminal
14	REC_R	External resistor connecting terminal for recording current output level monitor	49	PB_OUT	PB amplifier output terminal
15	HEAD_GND	Ground terminal	50	PB_IN	PB MAIN/ATF input terminal
16	HEAD_GND	Ground terminal	51	AGC_CTL	AGC control terminal for MAIN family
17	HEAD_GND	Ground terminal	52	AGC_DET	Time constant terminal for MAIN family
18	DY1	Damping resistor connecting terminal	53	PB_GND	Ground terminal
19	Y1	HEAD terminal	54	PREAGC	AGC+LPF output terminal for MAIN family
20	X1	HEAD terminal	55	AGC_IN	10.3dB amplifier input terminalfor MAIN family
21	DX1	Damping resistor connecting terminal	56	REG11	Regulator 1.1V output terminal
22	HEAD_GND	Ground terminal	57	AGC_OUT	Output terminal for MAIN family
23	DY2	Damping resistor connecting terminal	58	VRB_AGC	Bottom reference voltage output terminal for A/D converter of MAIN family
24	Y2	HEAD terminal	59	MAIN_GND	Ground terminal
25	X2	HEAD terminal	60	ATF_GAIN	VCA control terminal for ATF family
26	DX2	Damping resistor connecting terminal	61	VCA_OUT	VCA+BPF output terminal for ATF family
27	HEAD_GND	Ground terminal	62	ATF_IN	12dB amplifier input terminal for ATF family
28	DY3	Damping resistor connecting terminal	63	VRB_ATF	Bottom reference voltage output terminal for A/D converter of ATF family
29	Y3	HEAD terminal	64	ATF_OUT	Output terminal for ATF family
30	X3	HEAD terminal			
31	DX3	Damping resistor connecting terminal			
32	HEAD_GND	Ground terminal			
33	HEAD_GND	Ground terminal			
34	HEAD_GND	Ground terminal			
35	PBIN_R	External resistor connecting terminal for playback reference current			

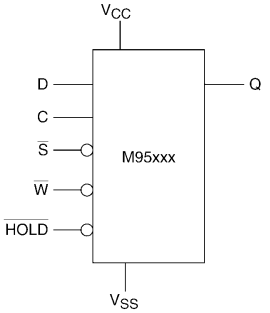
■ M95320-WMN6-X [ST MICROELECTRONICS]
(64/32 Kbit Serial SPI Bus EEPROM)

(Top View)

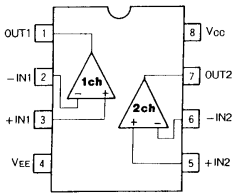
Signal Names

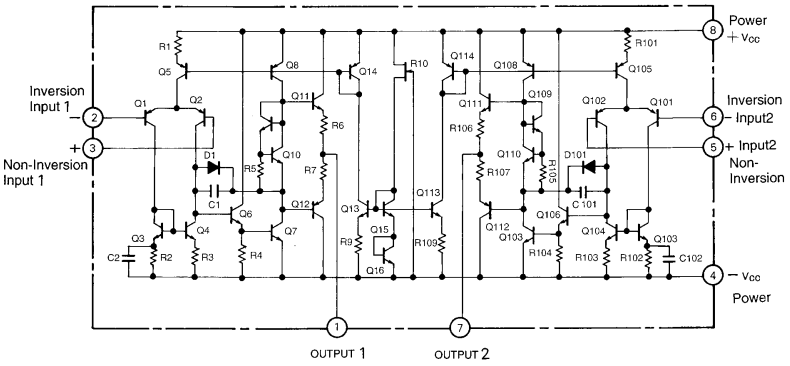
C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Logic Diagram

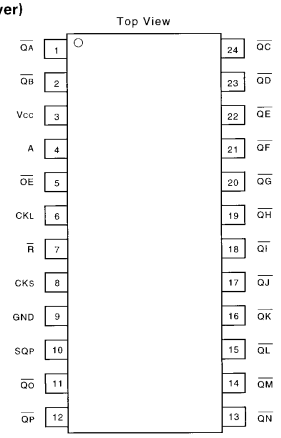


■ M5218AFP-X [MITSUBISHI]
(Dual Op.Amp.)

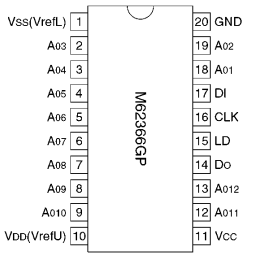




■ M66311FP-X [MITSUBISHI]
(LED Driver)



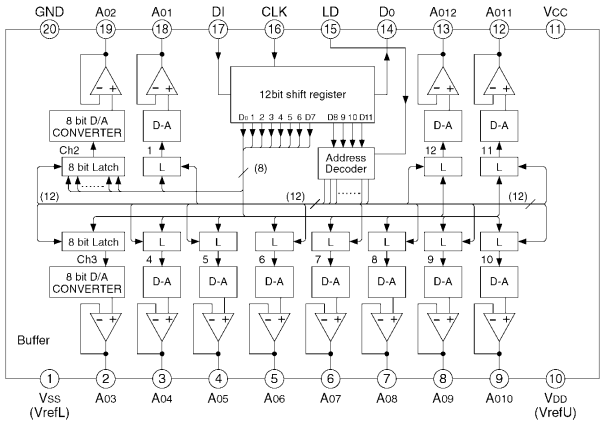
■ M62366GP-X [MITSUBISHI]
(8bit 12channel D/A converter)



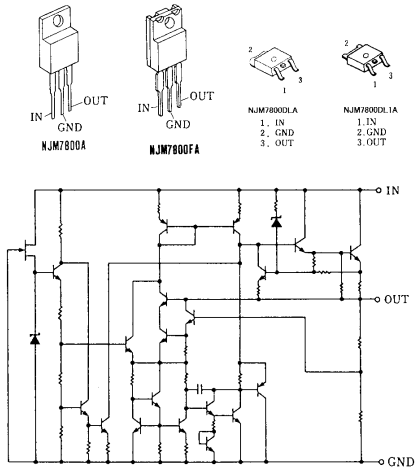
(TOP VIEW)

Pin No.	Symbol	Function
⑰	DI	Serial data input terminal to input 12-bit long serial data
⑭	DO	Terminal to output MSB data of 12-bit shift register
⑯	CLK	Shift clock input terminal.Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
⑮	LD	When H-level signal is input to this terminal,the value stored in 12-bit shift register is loaded in decoder and D-A converter output register
⑱ ⑲ ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑫ ⑬	A01 A02 A03 A04 A05 A06 A07 A08 A09 A010 A011 A012	8-bit D-A converter output terminal
⑪	VCC	Power supply terminal
⑳	GND	GND terminal
⑩	VDD	D-A converter upper reference voltage input terminal
①	VSS	D-A converter lower reference voltage input terminal

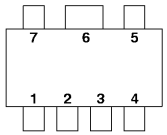
Block Diagram



■ NJM78M05DL1A-X [JRC]
(3-Terminal Positive Voltage Regulator (+5V))



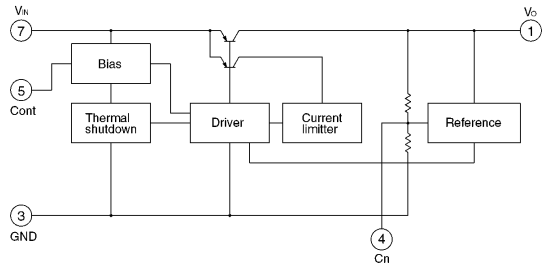
■ MM1565AF-X [MITSUMI]
(500mA Regulator (5V))



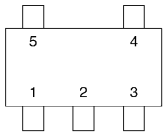
(TOP VIEW)

1	VO
2	NC
3	GND
4	Cn
5	CONT
6	Sub
7	VIN

Block Diagram



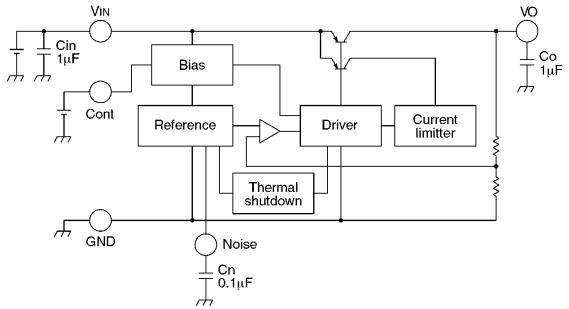
■ MM1571JN-X [MITSUMI]
(1.8V Regulator)



SOT-25A
(TOP VIEW)

1	VIN
2	GND
3	Cont
4	Noise
5	VO

Block Diagram



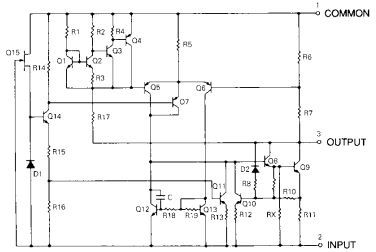
■ MM1572FN-X [MITSUMI]
(Refer to MM1571JN-X.)

■ MM1572KN-X [MITSUMI]
(Refer to MM1571JN-X.)

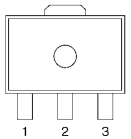
■ NJM79L05UA-X [JRC]
(3-Terminal Negative Voltage Regulator (-5V))

1. COMMON
2. IN
3. OUT

NJM79L00UA



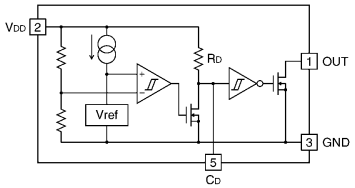
■ NJU7222U30-X [JRC]
(3-Terminal Positive Voltage Regulator)



1. GND
2. INPUT
3. OUTPUT

■ RN5VD26AA-X [RICHO]
(Voltage detector)

Block diagram

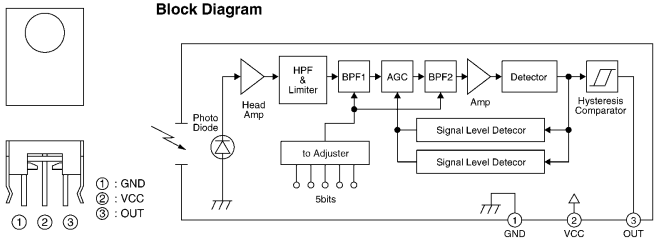


Pin descriptions

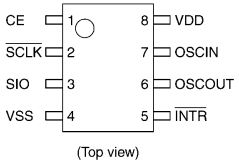
Pin Number	Pin Name	Pin Description
1	OUT	Output terminal
2	VDD	Power supply terminal
3	GND	Ground terminal
4	NC	Not connect
5	CD	External capacitor connecting terminal for delay

■ SBX3071-52 [SONY]
(Remote Control Receiver)

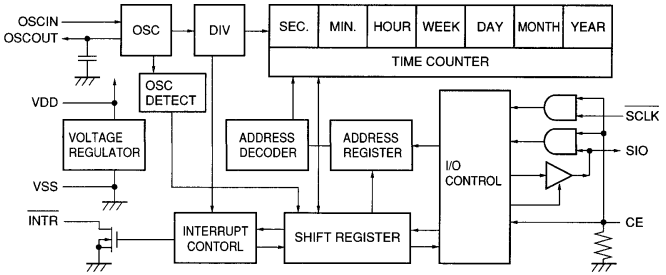
Block Diagram



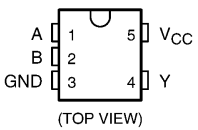
■ RS5C314-X [RICHO]
(CMOS Realtime Clock)



Block diagram



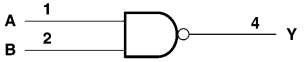
■ SN74AHC1G00K-X [TEXAS INSTRUMENTS]
(Single 2-Input Positive NAND Gate)



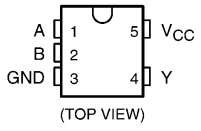
FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
H	H	L
L	X	H
X	L	H

Logic diagram (positive logic)



■ SN74AHC1G32K-X [TEXAS INSTRUMENTS]
(Single 2-Input Positive OR Gate)

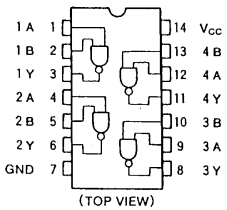


FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
H	X	H
X	H	H
L	L	L

Logic diagram (positive logic)

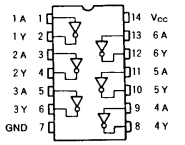
■ SN74AHC00PW-X [TEXAS INSTRUMENTS]
(Quad 2-Input NAND Gates)



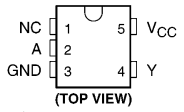
TRUE Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

■ SN74AHC04PW-X [TEXAS INSTRUMENTS]
(Hex Inverters)



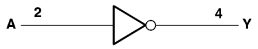
■ SN74AHC1GU04K-X [TEXAS INSTRUMENTS]
(Single Inverter Gate)



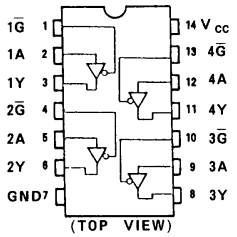
NC – No internal connection

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H



■ SN74AHCT125PW-X [TEXAS INSTRUMENTS]
(Quad Bus Buffer Gates With 3-State Outputs)

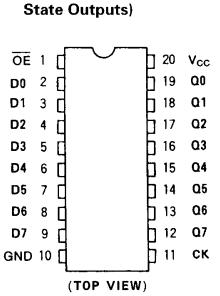


TC74HC125A TRUE Table

INPUTS G	INPUTS A	OUTPUTS Y
H	X	Z
L	L	L
L	H	H

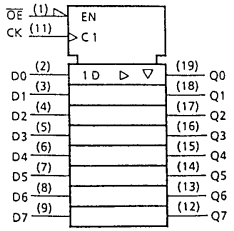
X : Don't Care
Z : High Impedance

■ SN74AHC574PW-X [TEXAS INSTRUMENTS]
(Octal D-Type EDGE-Trigger Flip-Flop With NON Inverted 3-State Outputs)



(TOP VIEW)

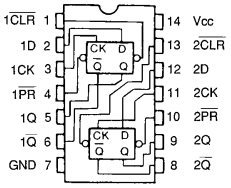
Logic



INPUTS			OUTPUT
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance
Qn : No Change

■ SN74AHC74PW-X [TEXAS INSTRUMENTS]
(Dual D-Type Flip-Flop with Preset and Clear)



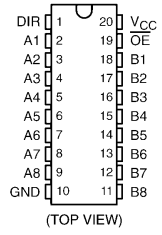
(Top View)

TRUE Table

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	L	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

■ SN74AHC245DGV-X [TEXAS INSTRUMENTS]
(Octal Bus Transceivers with 3-State Outputs)

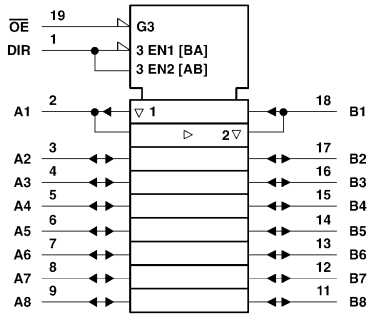


(TOP VIEW)

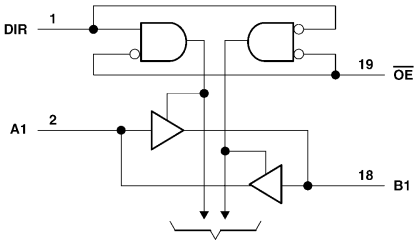
FUNCTION TABLE
(each transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Logic symbol

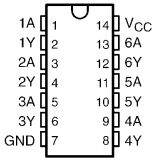


Logic diagram (positive logic)



To Seven Other Channels

■ SN74AHCT04PW-X [TEXAS INSTRUMENTS]
(Hex Inverters)

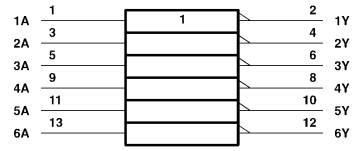


(TOP VIEW)

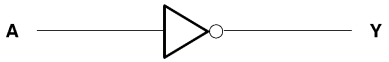
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

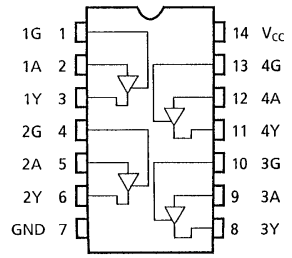
Logic symbol



Logic diagram, each inverter (positive logic)



■ SN74LV126ADGV-X [TEXAS INSTRUMENTS]
(Bus Buffer Gates with 3-State Output)

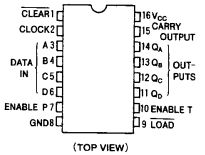


(TOP VIEW)

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't Care
Z : High Impedance

■ SN74HC161APW-X [TEXAS INSTRUMENTS]
(Synchronous 4-Bit Counters Binary, Direct Clear)



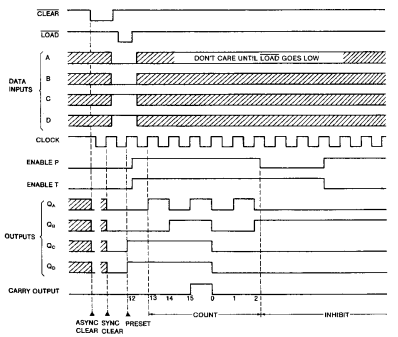
(TOP VIEW)

• THRU TABLE

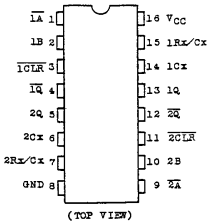
INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X	↑	A	B	C	D	Preset Data
H	H	X	L	X	No change				Do not count
H	H	L	X	X	No change				Do not count
H	H	H	H	↑	Count up				Count

Note X : Don't care
A,B,C,D : Logic level of input data
Carry : CARRY=ENT·QA·QB·QC·QD

Timing chart



■ TC74VHC221AFT-X [TOSHIBA]
(Dual Monostable Multivibrators (With Schmitt Trigger Input))

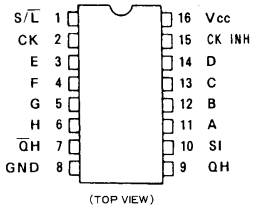


True Table

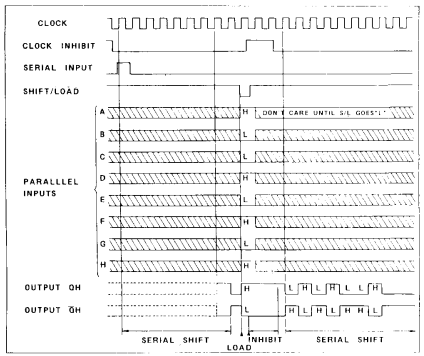
INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	CL	Q	$\overline{Q}$	
↓	H	H	⎍	⎍	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	⎍	H	⎍	⎍	OUTPUT ENABLE
L	H	⎍	⎍	⎍	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

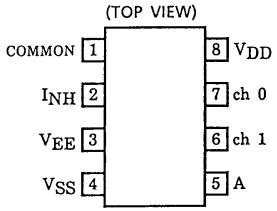
■ SN74LV165ADGV-X [TEXAS INSTRUMENTS]
(8-Bit Serial or Parallel-In/Serial Out Shift Registers)



Timing chart



■ TC4W53FU-X [TOSHIBA]
(2-Channel Multiprexer)



Truth table

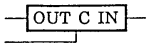
CONTROL C	IMPEDANCE BETWEEN IN-OUT ※
H	$0.5\sim5\times10^{2}\Omega$
L	$>10^{9}\Omega$

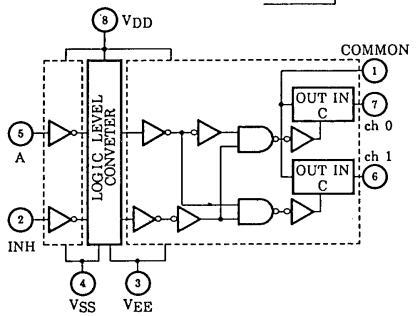
※ Don't Care

Truth table

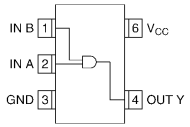
CONTROL INPUT		ON CHANNEL
INH	A	
L	L	ch 0
L	H	ch 1
H	※	NONE

※ Don't Care





■ TC7SET08F-X [TOSHIBA]
(2-input AND GATE)

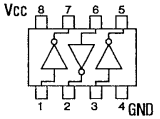


(TOP VIEW)

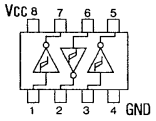
TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

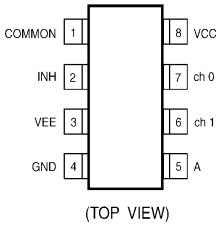
■ TC7W04F-X [TOSHIBA]
(Triple Inverter Gate)



■ TC7W14FU-X [TOSHIBA]
(Schmitt Trigger Triple Inverte Gate)



■ TC7W53FU-X [TOSHIBA]
(2-Channel Multiplexer/Demultiplexer)



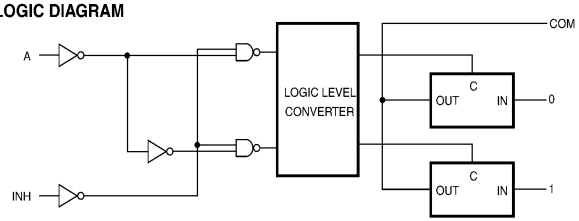
(TOP VIEW)

TRUTH TABLE

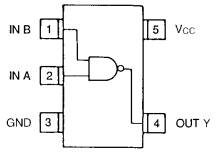
CONTROL INPUT		ON CHANNEL
INH	A	
L	L	ch 0
L	H	ch 1
H	x	NONE

x : Don't care

LOGIC DIAGRAM

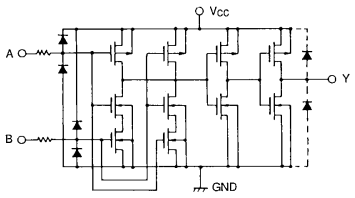


■ TC7SH00FU-X [TOSHIBA]
(2-Input NAND Gate)

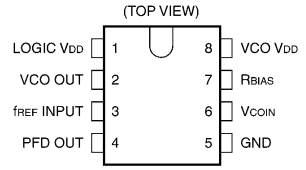


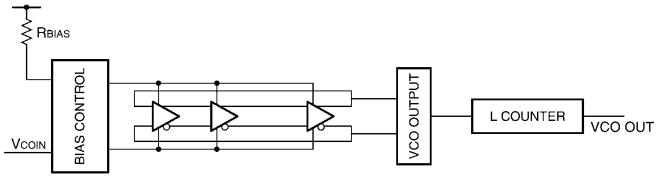
TRUE Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

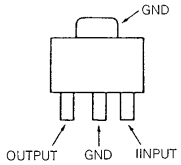


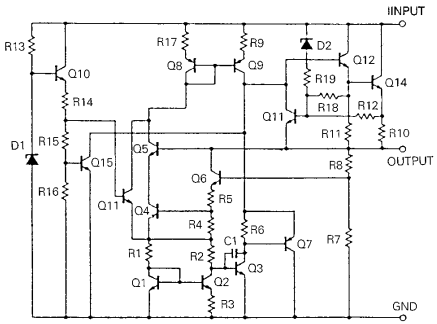
■ TLC2940IPW-X [TEXAS INSTRUMENTS] (75MHz CMOS VCO)



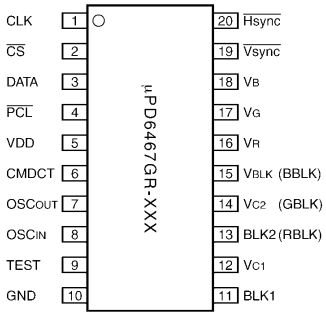


■ UPC78L05T-W [NEC] (3-Terminal Positive Voltage Regulator (+5V))



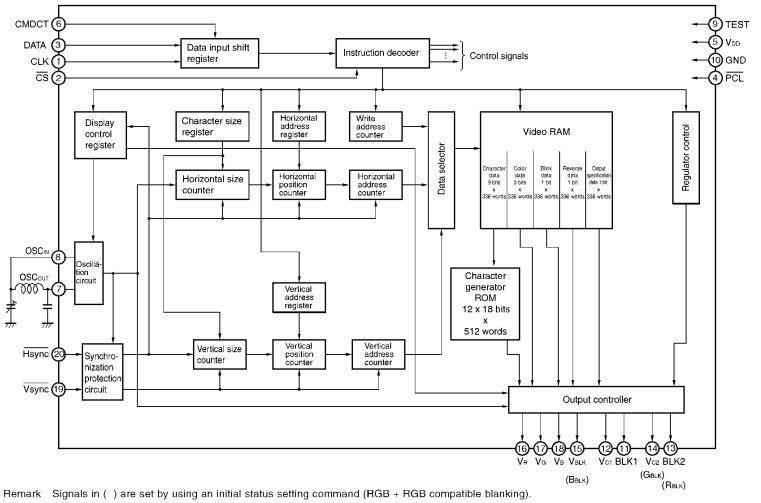


■ UPD6467GR-519-X [NEC] (ON-SCREEN CHARACTER DISPLAY)



(Top View)

BLOCK DIAGRAM



Remark Signals in ( ) are set by using an initial status setting command (RGB + RGB compatible blanking).