SECTION 4

TECHNICAL DESCRIPTION

CONTENTS

4.1 PRODUCT OUTLINE 4-1
4.2 MECHANISM 4-1
4.2.1 Mechanism out line 4-1
4.2.2 Regarding standard cassette 4-1
4.2.3 Cassette housing operation outline 4-2
4.2.4 Switches 4-4
4.2.5 Reel motor 4-4
4.2.6 Tension 4-4
4.2.7 Mode sensor 4-5
4.3 SYSTEM CONTROL 4-5
4.3.1 Outline 4-5
4.3.2 Communication specifications 4-5
4.3.3 Communication timing 4-5
4.3.4 SYSCON (IC2001) CPU port functions 4-6
4.3.5 MSD CPU (IC302) port functions 4-8
4.3.6 RS-422A command list 4-14

SECTION 4
TECHNICAL DESCRIPTION

4.1 PRODUCT OUTLINE

(1) DV Standard/Mini cassette compatible
(2) 4.5 hours consecutive recording/playback possible using Standard cassette (DV270)
(3) 5.25-inch half hight bay size compact design (mechanism unit only)
(4) Layout-free with horizontal and vertical positioning capability

4.2 MECHANISM

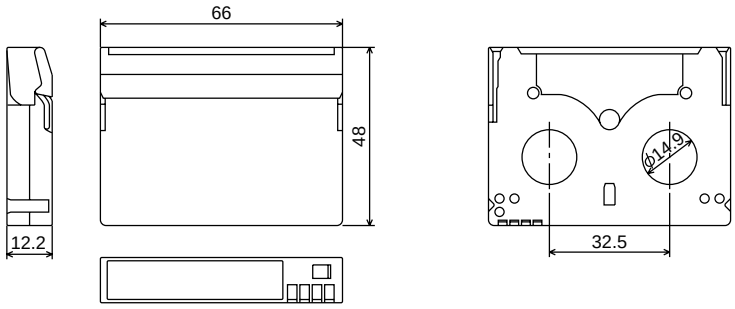
4.2.1 Mechanism out line

Item	AG-DV2500
Compatible cassette	Mini/Standard Cassette compatible
Loading system	Front loading
Head cleaner	Yes (solenoid)
Reel drive	Reel motor (1 motor)
FWD/REV reel switching	Swing gear switching
Tension control	Tension band method (SUP/TU dual control)

4.2.2 Regarding standard cassette

AG-DV2500 is newly compatible with DV standard size cassettes. Fig. 4.2.1 shows a size comparison with conventional Mini cassette. All dimensions differ, including cassette thickness in addition to height and width.

• Mini Cassette



• Standard Cassette

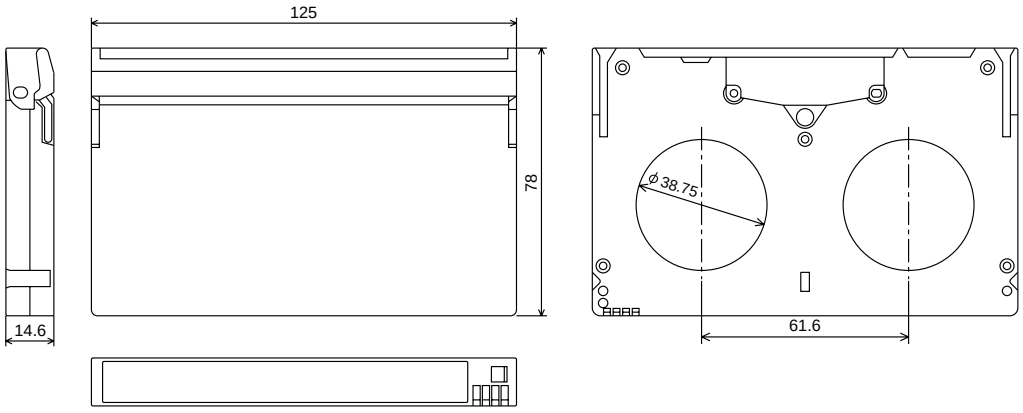


Fig. 4.2.1 Comparison Between Mini Cassette and Standard Cassette

4.2.3 Cassette housing operation outline

(1) Inserted cassette type detection

In its initial state, the reel disk is in the standard position, and only when a mini cassette is inserted it changes to the mini cassette position. As explained in Section 2, it is the reel change plate (Fig. 4.2.5) that changes the position of the reel disk.

As previously compared in 4.2.1, the thickness of standard and mini cassettes differ.

Standard cassette thickness : 14.6 mm

Mini cassette thickness : 12.2 mm

Based on this difference, it is differentiated within the cassette housing whether the inserted cassette is standard or mini.

1) When a mini cassette is inserted

The reel disk position changes to the mini cassette position at the same time the cassette housing performs the intake movement.

The reel change bracket (Fig. 4.2.3) located on the right side of the cassette housing is linked to the reel change plate (Fig. 4.2.4), so when the cassette housing intake movement occurs the reel change plate also moves, thereby changing to the mini cassette position.

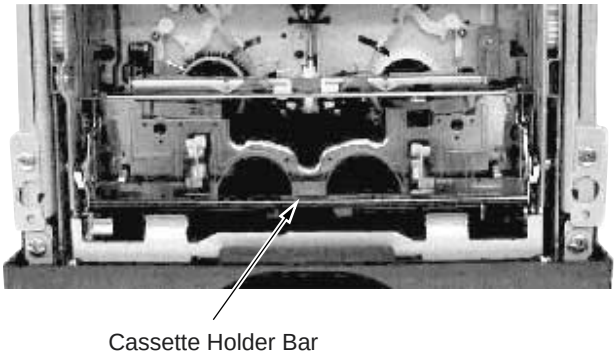


Fig. 4.2.2 Cassette Holder Bar

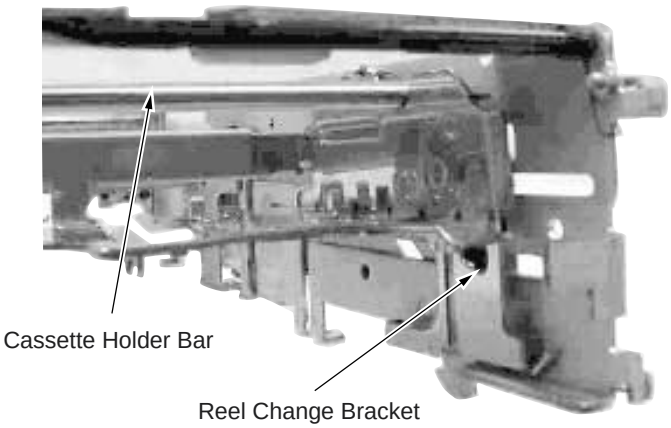


Fig. 4.2.3 Reel Change Bracket

2) When a standard cassette is inserted

The cassette holder bar (Fig. 4.2.2) is pushed up for the amount of thickness differential in relation to mini cassette, and in conjunction the reel change bracket (Fig. 4.2.3) located on the right side of the cassette housing moves upward. As a result, the link with the reel change plate (Fig. 4.2.4) becomes free, and the reel disk becomes held in the standard position even while the cassette housing is undergoing the intake movement.

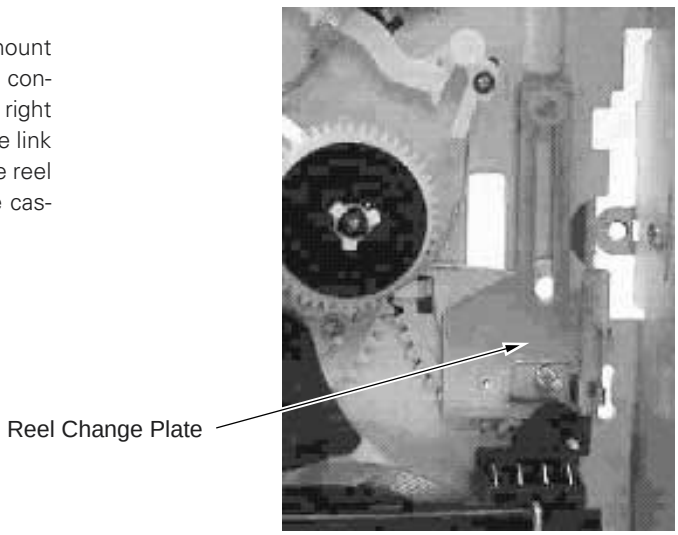


Fig. 4.2.4 Reel Change Plate

(2) Mini Cassette Incorrect Insertion Prevention Function

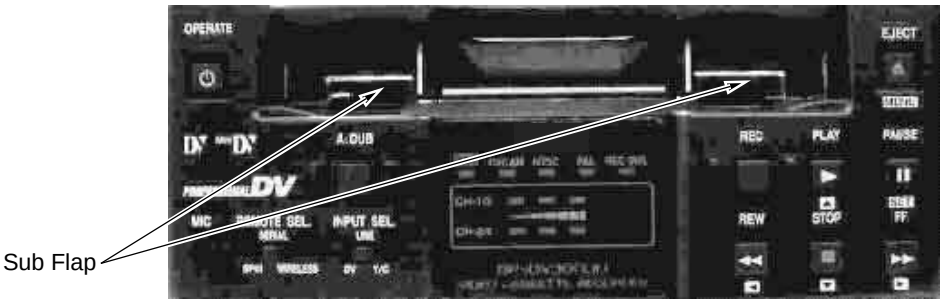


Fig. 4.2.5 Sub Flap

Sub flaps are attached on the cassette guide assembly located on the bottom end of the cassette housing door. These two sub flaps are designed to open when both are pressed simultaneously, and in the case of a mini cassette it is impossible for both to be pressed at the same time. So even if an inserted mini cassette touches against one of the sub flaps, the sub flaps will act as a brake to prevent erroneous loading of a mini cassette.

CAUTION

Even with standard cassettes, if the cassette is inserted skewed or diagonally offset in relation to the sub flaps, the sub flaps may not open and cassette insertion may not be possible. When inserting a standard cassette, be sure to insert so that the sides are parallel to the sub flaps.

(3) Intake/Eject Detection

Two housing switches (HW, HW2) are equipped on the front left side of the main deck. (See Fig. 4.2.6)
In the initial status in which no cassette is inserted (NO cassette mode), switch HW is pressed and switch HW2 is not pressed.

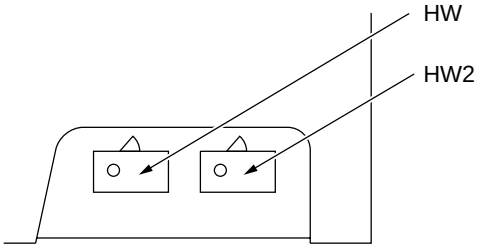


Fig. 4.2.6 Cassette Housing Switch

Mode	HW	HW2	S3
EJECT (Initial)	ON	OFF	OFF
INTAKE Detect	OFF	OFF	OFF
INTAKE END	OFF	OFF	ON
EJECT END	ON	ON	OFF

Table 4.2.1

Intake : When a cassette is inserted, the HW switch goes OFF, which causes detection of cassette insertion. After this the motor begins intake action.

Intake complete : When cassette intake is completed, in conjunction with the housing movement the main deck's switch lever slides, causing the MECHA board S3 (cassette switch) to be pressed, and intake completion is detected. (See Fig. 4.2.7)

Eject : When ejecting the cassette, both switches HW and HW2 are momentarily ON, and eject completion is detected. And from here, it returns to the initial status of switch HW=ON, HW2=OFF.

4.2.4 Switches

This is a description of how the various switches equipped on the mechanism operate, as shown in table 4.2.2.

Switch name	Operation	Location
HW	Cassette intake detection switch	Fig. 4.2.6
HW2	Cassette eject detection switch	Fig. 4.2.6
S1 (Mecha board)	Standard cassette detection switch	Fig. 4.2.7 ①
S2 (Mecha board)	SUP reel lock release switch*	Fig. 4.2.7 ②
S3 (Mecha board)	Cassette intake completion detection switch	Fig. 4.2.7 ③

Table 4.2.2 Switches

* Condition of SUP reel lock release switch operation :
After cassette intake, tape is pulled out of the take-up side for loading, but when a virgin tape is inserted it switches over to pull out from the supply side since it is not possible to pull out from the take-up side.
Immediately following tape intake completion, when the Begin sensor detects tape leader the cassette housing motor moves further to the loading side and, after the switches lever release the SUP brake, S2 is turned ON and brake release is detected.

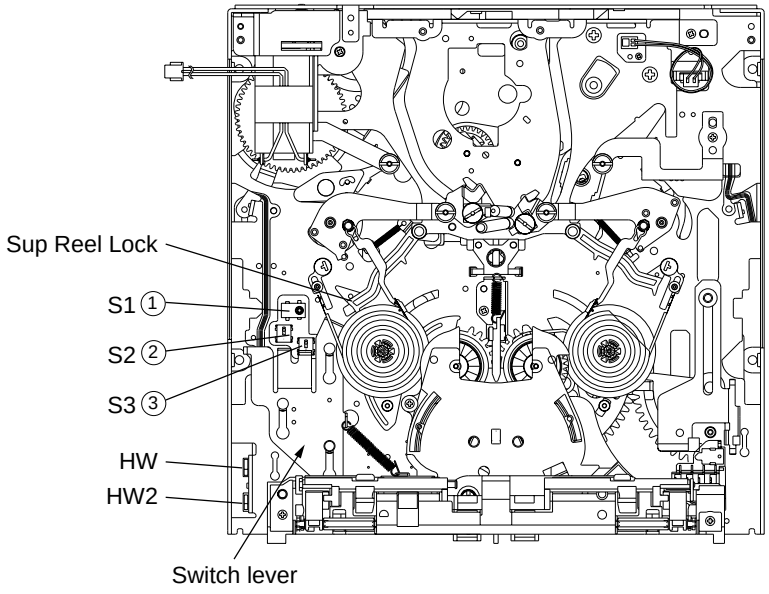


Fig. 4.2.7 Switch Location

4.2.5 Reel motor

The AG-DV2500 has adoped an independent one-reel motor, besides a capstan motor. As a result, quicker response when switching from Play to Reverse Search or Forward Search modes has been attained, greatly improving operability and the durability.

And as shown in table 4.2.3 the speeds of capstan search and FF/REW are also accelerated.

		AG-DV2500
CAPSTAN Search SPEED		Approx. 20X speed
FF/REW TIME	Mini (DVM60)	Under 75 sec.
	Standerd (DV270)	Under 200 sec.

Table 4.2.3

4.2.6 Tension

The AG-DV2500 have double tension control for supply/take-up.
The AG-DV2500 uses double tension control to regulate the tension differential caused by winding and modes used, obtaining a uniform tape tension for stable tape transport.

4.2.7 Mode sensor

The AG-DV2500's mode sensor adopts the variable resistor method (MECHA board VR1) which uses changes in resistance to detect the position of the mechanism. The changed voltage, brought about by changes in the resistance value due to mechanism position, is sent to DV/CPU IC302 to made to the A/D conversion. The mechanism position is judged by this.

Mode sensor voltage	Mechanism position	Mode
0.273 ± 0.03 V	UNLOAD END position	NO CASSETTE MODE
1.314 ± 0.03 V	BRAKE position	FF/REW → Modes in which tension band is used as brake for stopping
1.691 ± 0.03 V	FAST position	FF/REW MODE
2.111 ± 0.03 V	STOP position	STAND-BY OFF
2.716 ± 0.03 V	SEARCH position	PLAY/REC/SEARCH/STAND-BY ON

Table 4.2.4 Voltage and Mechanism Position Comparison

* Voltage figures shown are target values for software control, and may differ somewhat from the actual voltage. Please regard them as rough estimates.

4.3 SYSTEM CONTROL

4.3.1 Outline

The control system is comprised of the SYSCON CPU (IC2001) on the MAIN board assembly, and the VCR (MSD) CPU (IC302) on the DV/CPU board assembly. Both of these are connected by a bus called the MS_BUS, and communicate via serial data transfer

Communication type	Clock synchronous serial communication
Communication speed	1.68 Mbps
Data length	8bit x 25
Bit order	MSB head
Clock generation source	SYS CPU
Data direction	Full duplex

Table 4.3.1 MS_BUS Communication Settings

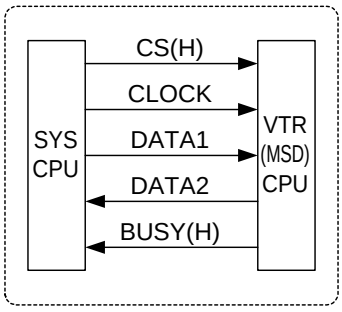


Fig. 4.3.1 MS BUS Connection

4.3.2 Communication specifications

(1) SYSCON CPU turns the CS from "L" → "H" and communication begins.
(2) SYSCON CPU confirms that the BUSY terminal is "L", and transmits data at CLOCK1.68MHz as well as receives data from the VCR (MSD) CPU.
(3) VCR (MSD) CPU also sends and receives data in accordance with CLK. However, if it is not yet ready for communication it sets the BUSY terminal to "H" and notifies the SYSCON CPU.
(4) When the BUSY terminal is "H", SYS CPU skips the current communication and waits until the next block (400 µs later) to see if it is "L" and then starts communication.
(5) After 25 Bytes are communicated, CS is set to "L" and communication ends.

4.3.3 Communication timing

In synchronization with internal reference sync, communication takes place once every 16.6 ms (NTSC) or 20 ms (PAL). Byte interval is 400 µs. When necessary the contents of the communication are changed at the 1st2nd field.

4.3.4 SYSCON (IC2001) CPU port functions

Pin No.	Port Name	Reference	I/O	Description
1	PE5	TP2004		Not used
2	PE6	HOUSING_SW	I	H : Insert cassette tape
3	PE7	CASS_SW	I	L : Complate to intake cassette tape
4	PD0	DAC_CS (H)	O	IC201 chip select
5	PD1	165_CS	O	IC2006/IC2007 chip select
6	PD2	4094_CS	O	IC3009/IC3010 chip select
7	PD3	AUD_DACTL_CS (L)	O	IC1006 (AUDIO DA) chip select
8	PD4	66311_DATA	O	IC2008 data
9	PD5	PON_MAIN (H)	O	
10	PD6	PON_UNIT (H)	O	
11	PD7	AUDREF12 (H)	O	Corresponds to audio level for consumer VTR.
12	CVCC	Power supply	+3V	
13	PC0	SDI	I	IC2006/IC2007 serial pin.
14	VSS	Power supply	GND	
15	PC1	S_DATA	O	IC2008/IC2010/IC201
16	PC2	S_CLK	O	IC2006/IC2008/IC2009/IC2010/IC201 clock
17	PC3	AUDIN_MUTE (H)	O	For muting the audio input
18	PC4	AUD_SYS_MUTE	O	For muting the audio output
19	PC5	AUDOUT_SMUT	O	For muting the search level
20	PC6	AUD_DACTL_CK	O	Audio DA clock
21	PC7	AUD_DACTL_DT	O	Audio DA data
22	PB0/TIOCA3	66311_CLK	O	IC208 clock
23	PB1/TIOCB3	66311_CSK	O	IC208 data
24	PB2/TIOCC3	WIRELESS_REM	I	Wireless remote input
25	PB3/TIOCD3	SERIAL_REM	I	Serial remote input
26	PB4/TIOCA4	NTSC (L)	O	VIDEO
27	PB5/TIOCB4	BWO (L)	O	VIDEO
28	PB6/TIOCA5	CPS (L)	O	VIDEO
29	PB7/TIOCB5	66311_RST	O	IC2008 RESET
30	PA0	ODD_EVEN	I	
31	PA1/TxD2	SYSCPU_TRXD	O	TCCS (For factory use)
32	PA2/RxD2	SYSCPU_TTXD	I	
33	PA3/SCK2	SYSCPU_TCK		YDC clock input
34	P10/TIOCA0	E2_DI	I	EEPROM
35	P11/TIOCB0	E2_DO	O	
36	P12/TIOCC0/TCLKA	E2_CLK	O	
37	P13/TIOCD0/TCLKB	E2_CS	O	
38	P14/TIOCA1/IRQ0	RTC_INT	I	RTC (Real time clock) IC2002
39	P15/TIOCB1/TCLKC	RTC_CS	O	
40	P16/TIOCA2/IRQ1	RTC_CLK	O	
41	P17/TIOCB2/TCLKD	RTC_SIO	I/O	
42	AVSS	Analog GND	GND	
43	P97/DA1			Not used
44	P96/DA0			Not used
45	P47/AN7			Not used
46	P46/AN6			Not used
47	P45/AN5			Not used
48	P44/AN4			Not used
49	P43/AN3	CIN_DC	I	
50	P42/AN2	LEVEL_DET_DC	I	Low battery detection

Pin No.	Port Name	Reference	I/O	Description
51	P41/AN1	METER_CH1	I	AUDIO indicator
52	P40/AN0	METER_CH2	I	
53	Vref	Analog reference	-	
54	AVCC	Analog power	+3V	
55	MD0	Mode terminal 0	I	Pullup (not used)
56	MD1	Mode terminal 1	I	Pullup (not used)
57	OSC2	Subclock (32.768kHz)	I	X2002
58	OSC1	Subclock (32.768kHz)	I	
59	RES	Reset input	I	From IC2004
60	NMI	NMI	I	Pullup (not used)
61	STBY	Standby	I	Pullup (not used)
62	VCC	Power	+3V	
63	XTAL	Clock	I	X2001
64	VSS	Power	GND	
65	EXTAL	External clock	I	X2001
66	FEW	Flush light enable	I	For Rewrite
67	MD2	Mode terminal 2	I	Operation mode setup
68	PF7/ϕ	System clock (TP2002)	O	
69	PF6	SWIN_NTSC	I	REAR NTSC/PAL slid SW
70	PF5	TP2021		Not used
71	PF4	FAN_STOP (H)	I	Not used
72	PF3/-ADTRG/IRQ3	OPERATE	I	Operate SW
73	PF2	EJECT	I	Pull-up from EJECT SW AL3V
74	PF1/BUZZ	TP2023	-	Not used
75	PF0/IRQ2	WAKE_UP	I	Start interrupt key input from standby mode
76	P30/TxD0	OSD_DATA	O	OSD (UART0)
77	P31/RxD0	OSD_CS	O	
78	P32/SCK0/SDA1/IRQ4	OSD_CLK	O	
79	P33/TxD1/SCL1	422_Tx	O	RS-422 (UART1)
80	P34/RxD1/SDA0	422_Rx	I	
81	P35/SCK1/SCL0/IRQ5	8029VD	I	IC208 CSYNC
82	P36	OSD_RST	O	OSD
83	P77/TxD3	MS_OUT	O	MS BUS (UART3)
84	P76/RxD3	MS_IN	I	
85	P75/TMO3/SCK3	MS_CLK	O	
86	P74/TMO2/MRES	SCR_LR	I	Not used
87	P73/TMO1	SCR_UD	I	Not used
88	P72/TMO0	V_MUTE	O	
89	P71/TMRI23/TMCI23	MSD_RESET		Reset output to VCR (MSD) microcomputer
90	P70/TMRI01/TMCI01	MSD_CS	O	Interface with VCR (MSD) microcomputer
91	PG0/IRQ6	SYS_OUTV	I	VIDEO V TIMING
92	PG1/IRQ7	SYS_INV	I	
93	PG2	MSD_READY	O	Interface with VCR (MSD) microcomputer
94	PG3	8029CS	O	IC208 control
95	PG4	8029CLK	O	
96	PE0	8029SDI	O	
97	PE1	8029SDO	I	
98	PE2	8029RST	O	
99	PE3	8029AMUTE	O	
100	PE4	V_PB (H)	O	VIDEO

Table 4.3.2 SYSCON Terminal Function

4.3.5 MSD CPU (IC302) port functions

Pin No.	Port Name	Reference	I/O	Description
1	ND	OPEN	-	Not used
2	ND	OPEN	-	Not used
3	VSS	D_GND	-	GND for digital
4	P01/D1	STD_CASS_SW	I	Standard cassette switch
5	P05/D5	START_SEL_2	O	Standard sensor sensibility selection
6	P11/D9	REEL_FWD_CTL	O	Reel motor direction control
7	NC (VDDF)	VOUT_25	I	Power for digital
8	VSS	D_GND	-	GND for digital
9	P26/D22/SBI1	EEPR_SDI	I	For EEPROM communication
10	P30/D24/SBT1	EEPR_SCL	O	For EEPROM communication
11	P35/D29/SBO3	MS_IN	O	Data for MS_BUS communication
12	P40/PWM1/TM0IO	DRUM_REF	O	DRUM_REF (MDA)
13	P51/IRQ1	DRUM_FG	I	DRUM_FG
14	P57/IRQ7	GND (10k)	O	Not used
15	NC (VDDF)	VOUT_25	I	Power for digital
16	P61/IRQ9	GNDÅi10kÅj	O	Not used
17 — 20	ND	OPEN	-	Not used
21	VDDH	AL_3VSYS	I	Power for digital
22	VOUT	VOUT_25	O	Power for VDD and VDDF
23	P14/D12	HOUSING_IN	O	Housing control
24	P03/D3	HOUSING2_SW	I	HW2/mini cassette eject switchs
25	P07/D7	END_SEL_2	O	End sensor sensibility
26	P13/D11	HOUSING_SW	I	Housing control
27	P20/D16/SBIB	CLN_SOL	O	Cleaner solenoid drive
28	P22/D18/SBTB	MSD_RDY	O	For MS_BUS communication
29	P32/D26/SBO2	LED_1SW	O	Front panel LED 1
30	VDDH	AL_3VSYS	I	Power for digital
31	VSS	D_GND	-	GND for digital
32	P53/IRQ3	GND (10k)	O	Not used
33	P25/D21/SBT0	MIC_3	O	CLK for cassette MIC communication
34	P33/D27/SBT2	EEPR_CS	O	For EEPROM communication
35	P63/IRQ11	GND (10k)	O	Not used
36	ND	OPEN	-	Not used
37	ND	OPEN	-	Not used
38	PU1/WE3/SRAS	OPEN	O	Not used
39	LON	AL_3VSYS (1k)	I	Use for regulator
40	NMIRQ	AL_3VSYS	O	Not used
41	VDDH	AL_3VSYS	I	Power for digital
42	P04/D4	START_SEL_1	O	Standard sensor sensibility selection
43	P06/D6	END_SEL_1	O	End sensor sensibility selection
44	P15/D13	HOUSING_OUT	O	Housing control
45	P17/D15	CAP_BRK	O	MDA control
46	NC (VSS)	D_GND	-	GND for digital
47	P23/D19/SBI0	MIC_1	O	For cassette MIC communication
48	P31/D25/SBI2	LED_2_SW	O	Front panel LED2
49	P37/D31/PWM0	CAP_REF	O	CAP_REF (MDA)
50	P41/PWM2/TM1IO	MECHA_REF	O	Mode/Housing motor control voltage
51	P43/PWM4	OPEN	O	Not used
52	P34/D28/SBI3	MS_OUT	I	Data for MS_VUS communication
53	P54/IRQ4	GND (10k)	O	Not used

Pin No.	Port Name	Reference	I/O	Description
54	P62/IRQ10	GND	O	Not used
55	P80/ICR0	DRUM_FG	I	DRUM_FG
56	P81/ICR1	CAP_FG	I	CAP_FG
57	PT2/SBT9	OPEN	O	Not used
58	PS1/SBO4	MDA_IN	O	For MDA communication
59	PU0/WE2/SCAS	OPEN	O	Not used
60	PS3/SBI5	OPEN	O	Not used
61	VOUT	VOUT_25	O	Power for VDD and VDDF
62	P00/D0	TAPE_LED	O	For TAPE_LED
63	VSS	D_GND	-	GND for digital
64	VDDH	AL_3VSYS	I	Power for digital
65	P16/D14	MECHA_VM_CTL	O	Switching the MECHA VM
66	P24/D20/SBO0	MIC_2	O	For cassette MIC communication
67	VSS	D_GND	-	GND for digital
68	P42/PWM3/TM2IO	REEL_REF	O	Reel motor control voltage
69	P55/IRQ5	GND (10k)	O	Not used
70	P52/IRQ2	DRUM_PG	I	DRUM_PG
71	P56/IRQ6	GND(10k)	O	Not used
72	P84/ICR4	SUP_REEL_SENSOR	I	SUP_REEL_SENSOR
73	VSS	D_GND	-	GND for digital
74	P60/IRQ8	GND (10k)	O	Not used
75	P83/ICR3	TU_REEL_SENSOR	I	TU_REEL_SENSOR
76	PS4/SBO5	OPEN	O	Not used
77	PT0/SBI9	OPEN	O	Not used
78	PR4/A23/KI4/SDCLKO	GND (10k)	O	Not used
79	PS5/SBT5	OPEN	O	Not used
80	PT1/SBO9	OPEN	O	Not used
81	VSS	D_GND	-	GND for digital
82	P02/D2	SP_LOCK_SW	I	SP lock detection switch
83	P10/D8	REEL_BRK	O	Reel motor brake
84	P12/D10	CASETTE_SW	I	CASSETTE SW
85	P21/D17/SBOB	A_MUTE	O	Audio mute
86	P27/D23/SBO1	EEPR_SDO	O	EEPROM communication
87	P36/D30/SBT3	MS_CLK	I	CLK for MS_BUS communication
88	P50/IRQ0	MSD CS	I	MSD CS
89	ND	OPEN	-	Not used
90	P90/ICR8	FRP	I	Interface with IC103
91	P82/ICR2	REEL_FG	I	Reel FG input
92	P86/ICR6	SRV_FRP	I	Interface with IC103
93	P85/ICR5	HID1	I	Interface with IC103
94	P87/ICR7	DET_VD	I	Analog input detection
95	PR6/A25/KI6	GND (10k)	O	Not used
96	PS2/SBT4	MDA_CLK	O	For MDA communication
97	VDDH	AL_3VSYS	I	Power for digital
98	VSS	D_GND	-	GND for digital
99 — 108	ND	OPEN	-	Not used
109	NC (VSS)	D_GND	-	GND for digital
110	VDD2	AL_3VSYS	I	Power for digital
111	P92/ICR10	SPA	I	Interface with IC103
112	VSS	D_GND	-	GND for digital

Pin No.	Port Name	Reference	I/O	Description
113	P91/ICR9	TSR	I	Interface with IC103
114	PR3/A22/KI3/SCKE	GND (10k)	O	Not used
115	PR5/A24/KI5/SDCLKI	GND (10k)	O	Not used
116	PQ2/A18	DV_RST	O	Interface with IC103
117	PS0/SBI4	MDA_CS	O	For MDA communication
118	PR7/KI7/PWM5	GND (10k)	O	Not used
119 — 127	ND	OPEN	-	Not used
128	PA1/SBO6	OPEN	O	Not used
129	P94/ICR12	SRV_TRK	I	Interface with IC103
130	PA3/SBI7	OPEN	O	Not used
131	PA0/SBI6	OPEN	O	Not used
132	PA2/SBT6	OPEN	O	Not used
133	PQ1/A17	CLK27SEL	O	Interface with IC103
134	PR0/A19/KI0	GND (10k)	O	Not used
135	PQ0/A16	NTSC_L	I	NTSC_L
136	PR2/A21/KI2/SWE	GND (10k)	O	Not used
137	PR1/A20/KI1	GND (10k)	O	Not used
138 — 146	ND	OPEN	-	Not used
147	PB3/WDOVF	OPEN	O	Not used
148	P93/ICR11	OUT_V	I	MVD0 (DVSYS)
149	PA5/SBT7	OPEN	O	Not used
150	PA4/SBO7	OPEN	O	Not used
151	PB2/IRQ14	OPEN	O	Not used
152	VSS	D_GND	-	GND for digital
153	PL5/PWM6	OPEN	O	Not used
154	PL4/TM7IO	V_MUTE	I	V MUTE (DVSYS)
155	PL3/TM6IO	OPEN	O	Not used
156	PL2/TM5IO	SCR_UD	O	Not used
157 — 165	ND	OPEN	-	Not used
166	PC3/SY0OT3	OPEN	-	Not used
167	PB0/IRQ12	OPEN	O	Not used
168	PB1/IRQ13	INV	I	ODD/EVEN distinguish
169	PB4/BR	OPEN	O	Not used
170	VSS	D_GND	-	GND for digital
171	PL0/TM3IO	OPEN	O	Not used
172	PK6/TM36IO	HID3	O	Interface with IC1
173	PL1/TM4IO	SCR_LR	O	Not used
174	PK4/TM34IO	PBH	O	Interface with IC1
175	PK3/TM33IO	REEL_LED	O	TU_REEL_LED
176 — 184	ND	OPEN	-	Not used
185	PC5/SY1OT1/SBO8	OPEN	O	Not used
186	PC0/SY0OT0	HID1	O	TO P/R IC1
187	PB5/BG	OPEN	O	Not used
188	PC2/SY0OT2	OPEN	-	Not used
189	PC4/SY1OT0/SBI8	OPEN	I	Not used
190	OSCI	Supply the external clock	I	40MHz
191	PK2/TM32IO	REC_SAFE	I	REC_SAFTY_SW
192	PK0/TM30IO	OPEN	O	Not used
193	VDD	VOUT_25	I	Power for digital
194	VSS	D_GND	-	GND for digital

Pin No.	Port Name	Reference	I/O	Description
195 — 203	ND	OPEN	-	Not used
204	VSS	D_GND	-	GND for digital
205	PD0/TM10IO	OPEN	O	Not used
206	PC1/SY0OT1	OPEN	-	Not used
207	VDD2	AL_3VSYS	I	Power for digital
208	PC6/SY1OT2/SBT8	OPEN	-	Not used
209	OSCO		O	40MHz
210	FRQS	VTR_TAUX	I	For rewrite
211	PK7/TM37IO	MONI_CHG	O	Interface with P/R
212	CKSEL	VTR_TTxD	I	For rewrite
213	MMOD1	VTR_TCK	I	For rewrite
214 — 222	ND	OPEN	-	Not used
223	NC (VSS)	D_GND	-	GND for digital
224	PE1/TM20IOB	GND (10k)	O	Not used
225	PC7/SY1OT3	OPEN	-	Not used
226	PD3/TM13IO	OPEN	O	Not used
227	PD2/TM12IO	OPEN	O	Not used
228	MMOD0	VTR_TRXD	I	For rewrite
229	PJ1/EXMOD1	VTR_TAUX3	I	For rewrite
230	PK5/TM35IO	REC_H	O	Interface with P/R
231	VDDH	AL_3VSYS	I	Power for digital
232	PVSS	A_GND	I	GND for analog
233 — 241	ND	OPEN	-	Not used
242	VDD	VOUT_25	I	Power for digital
243	PE7/TM23IOB	GND (10k)	O	Not used
244	PD1/TM11IO	OPEN	O	Not used
245	PE3/TM21IOB	FFREW_H	O	Not used
246	PD5/TM15IO	OPEN	O	Not used
247	PVDD	AL_3VSYS	I	Power for analog
248	PP7/ADM15/A15	ADM15	I/O	Interface with IC103
249	PK1/TM31IO	OPEN	O	Not used
250	RST	VTR_RESET	I	For rewrite
251 — 261	ND	OPEN	-	Not used
262	PE4/TM22IOA	GND (10k)	O	Not used
263	PD4/TM14IO	OPEN	O	Not used
264	PE5/TM22IOB	GND (10k)	O	Not used
265	VDD2	AL_3VSYS	I	Power for digital
266	PP5/ADM13/A13	ADM13	I/O	Interface with IC103
267	PP3/ADM11/A11	ADM11	I/O	Interface with IC103
268	PP4/ADM12/A12	ADM12	I/O	Interface with IC103
269	VSS	D_GND	-	GND for digital
270	VSS	D_GND	-	GND for digital
271	ND	OPEN	-	Not used
272	VDD	VOUT_25	I	Power for digital
273	VSS	D_GND	-	GND for digital
274	P70/AN24	GND (10k)	-	Not used
275	PI6/AN22	GND (10k)	-	Not used
276	PI0/AN16	GND (10k)	-	Not used
277	PH0/AN8	THERM_MSD	I	Temperature sensor
278	PG0/AN0	START_SENSOR	I	START_SENSOR

Pin No.	Port Name	Reference	I/O	Description
279	ND	OPEN	-	Not used
280	TRST	VSS (10k)	-	Not used
281	PF0/TM24IOA	OPEN	O	Not used
282	PE2/TM21IOA	DRUM_FG	O	DRUM_FG
283	PE0/TM20IOA	GND (10k)	O	Not used
284	PF1/TM24IOB	OPEN	O	Not used
285	PP1/ADM9/A9	ADM9	I/O	Interface with 3.5LSI
286	PJ0/EXMOD0	GND (10k)	I	Memory mode selection
287	PO4/ADM4/A4	ADM4	I/O	Interface with IC103
288	PO7/ADM7/A7	ADM7	I/O	Interface with IC103
289	PO1/ADM1/A1	ADM1	I/O	Interface with IC103
290	PN5/AS	DALE	O	Interface with IC103
291	PN4/DK	DV_WAIT	I	Interface with IC103
292	PM4/CS4	OPEN	O	Not used
293	VDDB	AL_3VSYS	I	Power for digital
294	PI4/AN20	GND (10k)	-	Not used
295	PI1/AN17	GND (10k)	-	Not used
296	PH1/AN9	REEL_CURENT	I	Reel motor current
297	PG1/AN1	END_SENSOR	I	E_SENSOR
298	VREFH	AL_3VSYS (for analog)	I	A/D GND (H)
299	VDD	VOUT_25	I	Power for digital
300	TMS	VDD2 (10k)	-	Not used
301	PE6/TM23IOA	GND (10k)	O	Not used
302	PF2/TM25IOA	OPEN	O	Not used
303	PF3/TM25IOB	GND (10k)	O	Not used
304	PP0/ADM8/A8	ADM8	I/O	Interface with IC103
305	PP6/ADM14/A14	ADM14	I/O	Interface with IC103
306	PP2/ADM10/A10	ADM10	I/O	Interface with IC103
307	PN3/RE	DRE	O	Interface with IC103
308	PN1/WE1/SDQM1	OPEN	O	Not used
309	PM2/CS2	DV_CS	O	Interface with IC103
310	PM5/RWSEL	RWSEL	O	Interface with IC103
311	PM0/CS0	OPEN	O	Not used
312	PI2/AN18	GND (10k)	-	Not used
313	PH6/AN14	EJECT_MSD	-	EJECT brings up
314	PH7/AN15	GND (10k)	-	Not used
315	PH4/AN12	GND (10k)	-	Not used
316	PH2/AN10	REEL_ECR	I	Reference value for reel torque control
317	PG4/AN4	MIC_2	I	AD for MIC IDBOARD detection
318	PG2/AN2	DEW_SENSOR	I	DEW_SENSOR
319	VREFL	A_GND	I	A/D GND (L)
320	PV1/SBOA	DAC_DATA	O	D/A control
321	TCK	VDD2 (10k)	-	Not used
322	TDI	VDD2 (10k)	-	Not used
323	ND	OPEN	-	Not used
324	ND	OPEN	-	Not used
325	VDDB	AL_3VSYS	I	Power for digital
326	PO2/ADM2/A2	ADM2	I/O	Interface with IC103
327	PO5/ADM5/A5	ADM5	I/O	Interface with IC103
328	VDD	VOUT_25	I	Power for digital

Pin No.	Port Name	Reference	I/O	Description
329	VSS	D_GND	-	GND for digital
330	PN0/WE0/SDQM0	DWE	O	Interface with IC103
331	PM1/CS1	OPEN	O	Not used
332	PI7/AN23	GND (10k)	-	Not used
333	PI3/AN19	GND (10k)	-	Not used
334	PH3/AN11	HOUS_CURRENT	I	Tension sensor
335	PG5/AN5	MIC_1	I	AD for MIC IDBOARD detection
336	AVDD	AL_3VSYS	I	Power for analog
337	VSS	D_GND	-	GND for digital
338	PG6/AN6	GND (10k)	-	Not used
339	PV2/SBTA	DAC_CLK	O	D/A control
340 — 343	ND	OPEN	-	Not used
344	PO6/ADM6/A6	ADM6	I/O	Interface with IC103
345	PO3/ADM3/A3	ADM3	I/O	Interface with IC103
346	VDDB	AL_3VSYS	I	Power for digital
347	PO0/ADM0/A0	ADM0	I/O	Interface with IC103
348	PN2/SYSCLK	OPEN	O	Not used
349	PM3/CS3	OPEN	O	Not used
350	VSS	D_GND	-	GND for digital
351	AVSS	A_GND	I	GND for analog
352	PI5/AN21	GND (10k)	-	Not used
353	PH5/AN13	GND (10k)	-	Not used
354	PG7/AN7	MODE_SENS	I	Mode sensor (mecha position)
355	PG3/AN3	MIC_3	I	AD for MIC IDBOARD detection
356	PV3/ADTRG	AL_3VSYS	-	Not used
357	PV0/SBIA	DAC_CS	O	D/A control
358	TDO	OPEN	-	Not used
359 — 360	ND	OPEN	-	Not used

Table 4.3.3 MSD Terminal Function

4.3.6 RS-422A command list

COMMAND FROM CONTROLLER					RETURN FROM			
CMD -1	Data Count	CMD -2	DATA -1	NAME	CMD -1	Data Count	CMD -2	NAME
0	0	0C	-	Local Disable	1	0	01	ACK
0	0	11	-	Device Type Request	1	2	11	Device Type
0	0	1D	-	Local Enable	1	0	01	ACK
2	0	00	-	Stop	1	0	01	ACK
2	0	01	-	Play	1	0	01	ACK
2	0	02	-	Rec	1	0	01	ACK
2	0	03	-	StillÄiJVC OnlyÄj	1	0	01	ACK
2	0	04	-	Standby Off	1	0	01	ACK
2	0	05	-	Standby On	1	0	01	ACK
2	0	0F	-	Eject	1	0	01	ACK
2	0	10	-	Fast Fwd	1	0	01	ACK
2	X	11	-	Jog Fwd	1	0	01	ACK (Switch to shuttle)
2	X	12	-	Var Fwd	1	0	01	ACK (Switch to shuttle)
2	X	13	-	Shuttle Fwd	1	0	01	ACK
2	0	20	-	Rewind	1	0	01	ACK
2	X	21	-	Jog Rev	1	0	01	ACK (Switch to shuttle)
2	X	22	-	Var Rev	1	0	01	ACK (Switch to shuttle)
2	X	23	-	Shuttle Rev	1	0	01	ACK
2	0	30	-	Preroll	1	0	01	ACK
2	4	31	-	Cue Up With Data	1	0	01	ACK
2	0	54	-	Anti-clog Timer Disable	1	0	01	ACK
2	0	55	-	Anti-clog Timer Enable	1	0	01	ACK
4	4	04	-	Time Code Preset	1	0	01	ACK
4	0	10	-	In Entry	1	0	01	ACK
4	4	14	-	In Data Preset	1	0	01	ACK
4	0	18	-	In + Shift	1	0	01	ACK
4	0	19	-	In - Shift	1	0	01	ACK
4	0	20	-	In Reset	1	0	01	ACK
4	0	24	-	In Recall	1	0	01	ACK
4	4	31	-	Preroll Time Preset	1	0	01	ACK
4	X	3E	-	Rec Inhibit Preset	1	0	01	ACK
6	1	0A	01	TC Gen Data Sense	7	4	08	Gen Time Data
6	1	0A	10	TC Gen Data Sense	7	4	09	Gen UB Data (UB: Fix to 0)
6	1	0A	11	TC Gen Data Sense	7	8	08	Gen TC & UB Data (UB: Fix to 0)
6	1	0C	01	Current Time Sense	7	4	04	TC (main) Data
6	1	0C	02	Current Time Sense	7	4	06	TC (main) Data
6	1	0C	03	Current Time Sense	7	4	04	TC (main) Data
6	1	0C	10	Current Time Sense	7	4	05	UB (main) Data (UB: Fix to 0)
6	1	0C	11	Current Time Sense	7	8	04	TC & UB (main) Data (UB: Fix to 0)
6	1	0C	20	Current Time Sense	7	4	07	UB (main) Data (UB: Fix to 0)
6	1	0C	22	Current Time Sense	7	8	06	TC & UB (main) Data (UB: Fix to 0)
6	1	0C	30	Current Time Sense	7	4	05	UB (main) Data (UB: Fix to 0)
6	1	0C	33	Current Time Sense	7	8	04	TC & UB (main) Data (UB: Fix to 0)
6	0	10	-	In Data Sense	7	4	10	In Data
6	1	20	-	Status Sense	7	X	20	Status Data
6	0	2B	-	Remain Time Sense	7	6	2B	Remain Data
6	0	31	-	Preroll Time Sense	7	3	31	Preroll Time Data
6	0	36	-	Timer Mode Sense	7	1	36	Timer Mode Data
6	0	3E	-	Rec Inhibit Sense	7	2	3E	Rec Inhibit Status

Table 4.3.4 RS-422A Command List