

SECTION 5

BLOCK DIAGRAMS SCHEMATIC DIAGRAMS CIRCUIT BOARD DIAGRAMS

NOTE:

BE SURE TO MAKE YOUR ORDERS OF REPLACEMENT PARTS ACCORDING TO PARTS LIST, SECTION 6

CAUTION

THE  MARK INDICATES THE PRIMARY CIRCUIT TO DISTINGUISH THE PRIMARY FROM THE SECONDARY CIRCUIT.

PAY ATTENTION NOT TO RECEIVE AN ELECTRIC SHOCK DURING REPAIR AND SERVICE OF THE PRODUCTS.

IMPORTANT SAFETY NOTICE:

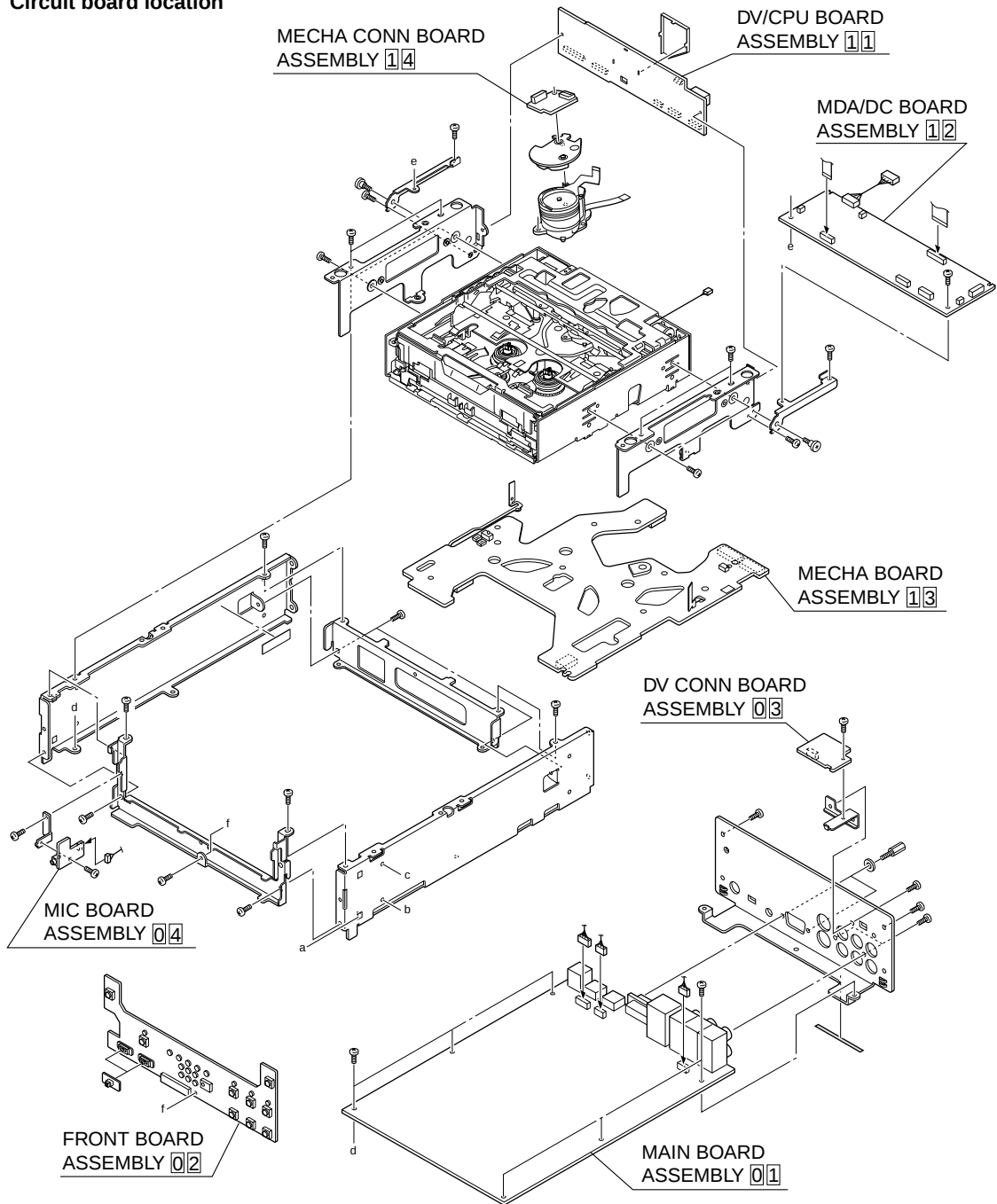
COMPONENTS IDENTIFIED WITH THE MARK  HAVE THE SPECIAL CHARACTERISTICS FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS, USE ONLY THE SAME TYPE.

CONTENTS

5.1	INDEX TO PAGES OF MAIN BOARDS AND CIRCUIT BOARD LOCATION	5-1
5.1.1	Circuit board location	5-1
5.2	SYSTEM CONTROL BLOCK DIAGRAM	5-2
5.3	VIDEO BLOCK DIAGRAM	5-3
5.4	AUDIO BLOCK DIAGRAM	5-4
5.5	OVERALL WIRING DIAGRAM	5-5
5.6	DV UNIT OVERALL WIRING DIAGRAM	5-6
5.7	MAIN SCHEMATIC DIAGRAM.....	5-7
5.8	MAIN CIRCUIT BOARD	5-13
5.9	DV/CPU SCHEMATIC DIAGRAM	5-15
5.10	DV/CPU CIRCUIT BOARD.....	5-19
5.11	MDA/DC CIRCUIT BOARD	5-20
5.12	MDA/DC SCHEMATIC DIAGRAM	5-21
5.13	FDM (FRONT, DV CONN & MIC) SCHEMATIC DIAGRAMS.....	5-25
5.14	FDM (FRONT, DV CONN & MIC) CIRCUIT BOARDS	5-26
5.15	MECHA & MECHA CONN SCHEMATIC DIAGRAMS	5-27
5.16	MECHA & MECHA CONN CIRCUIT BOARDS.....	5-28
5.17	IC BLOCK DIAGRAMS.....	5-30

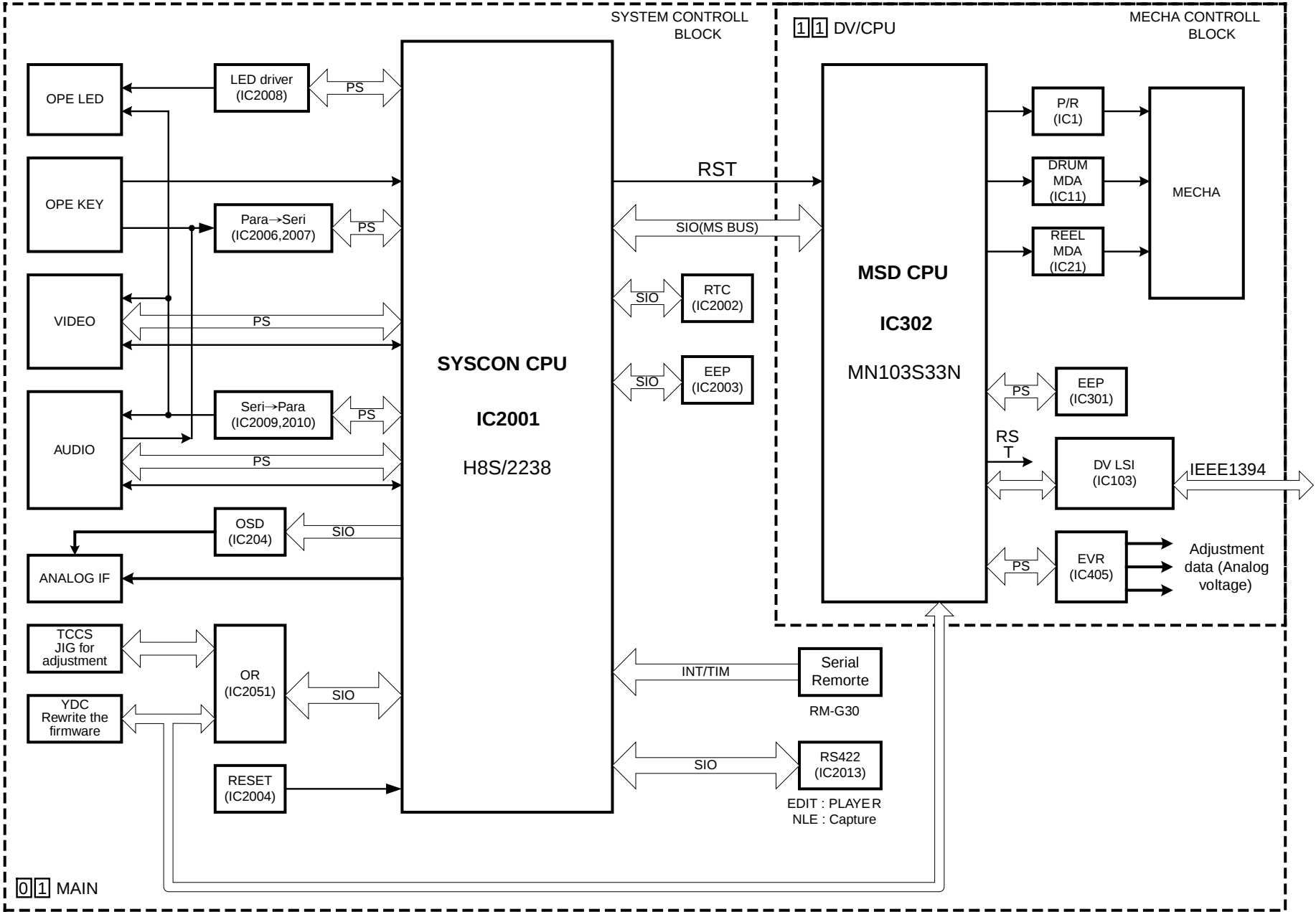
5.1 INDEX TO PAGES OF MAIN BOARDS AND CIRCUIT BOARD LOCATION

5.1.1 Circuit board location

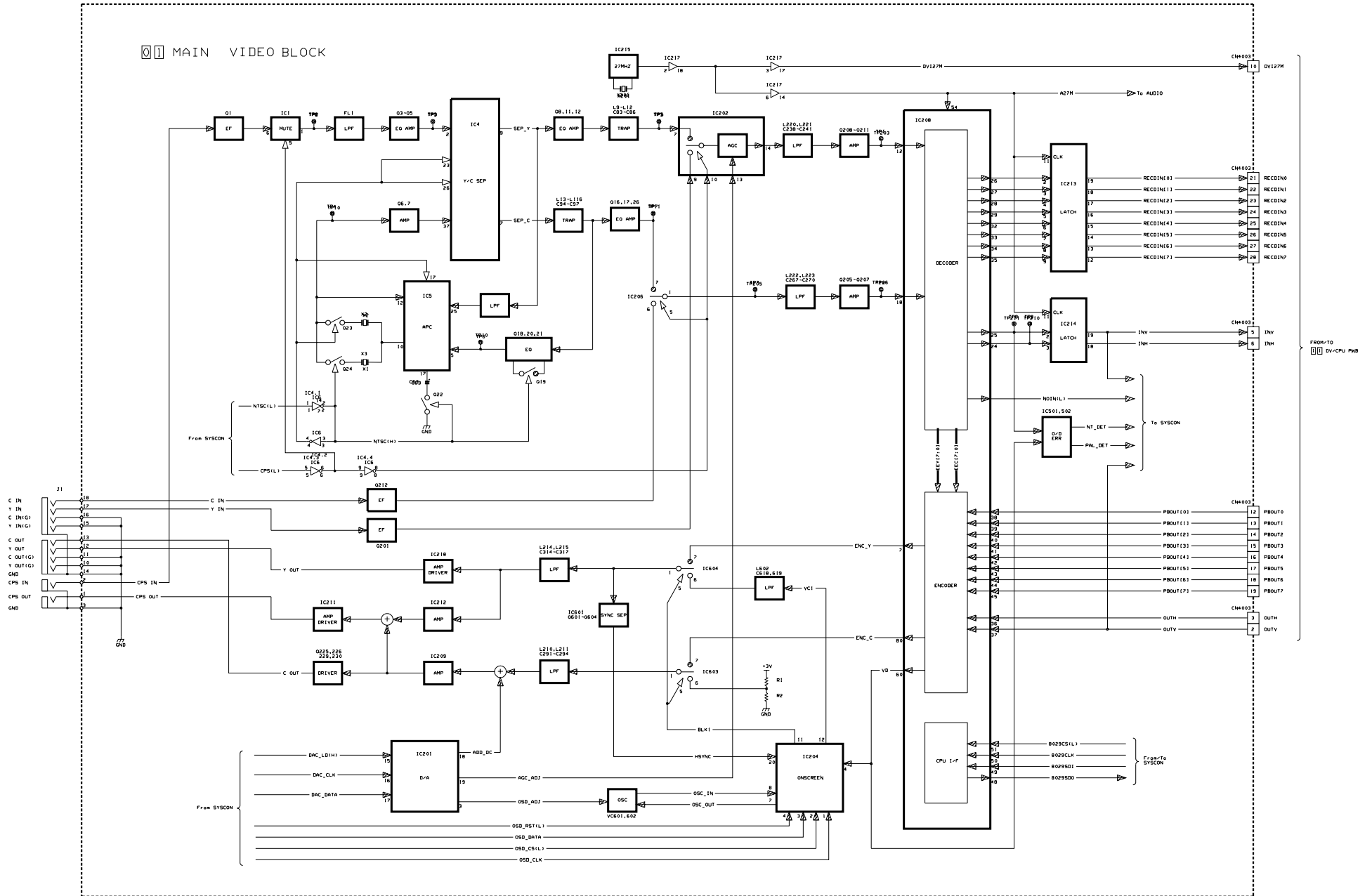


Board No.	Board Name	Page of diagram		
		Block diagram	Schematic diagram	Circuit board
01	MAIN	5-2, 5-3, 5-4	5-7 to 5-12	5-13, 5-14
02	FRONT	—	5-25	5-26
03	DV CONN	—	5-25	5-26
04	MIC	5-4	5-25	5-26
11	DV/CPU	5-2, 5-4	5-15 to 5-18	5-19
12	MDA/DC	—	5-21 to 5-24	5-20
13	MECHA	—	5-27	5-28, 5-29
14	MECHA CONN	—	5-27	5-29

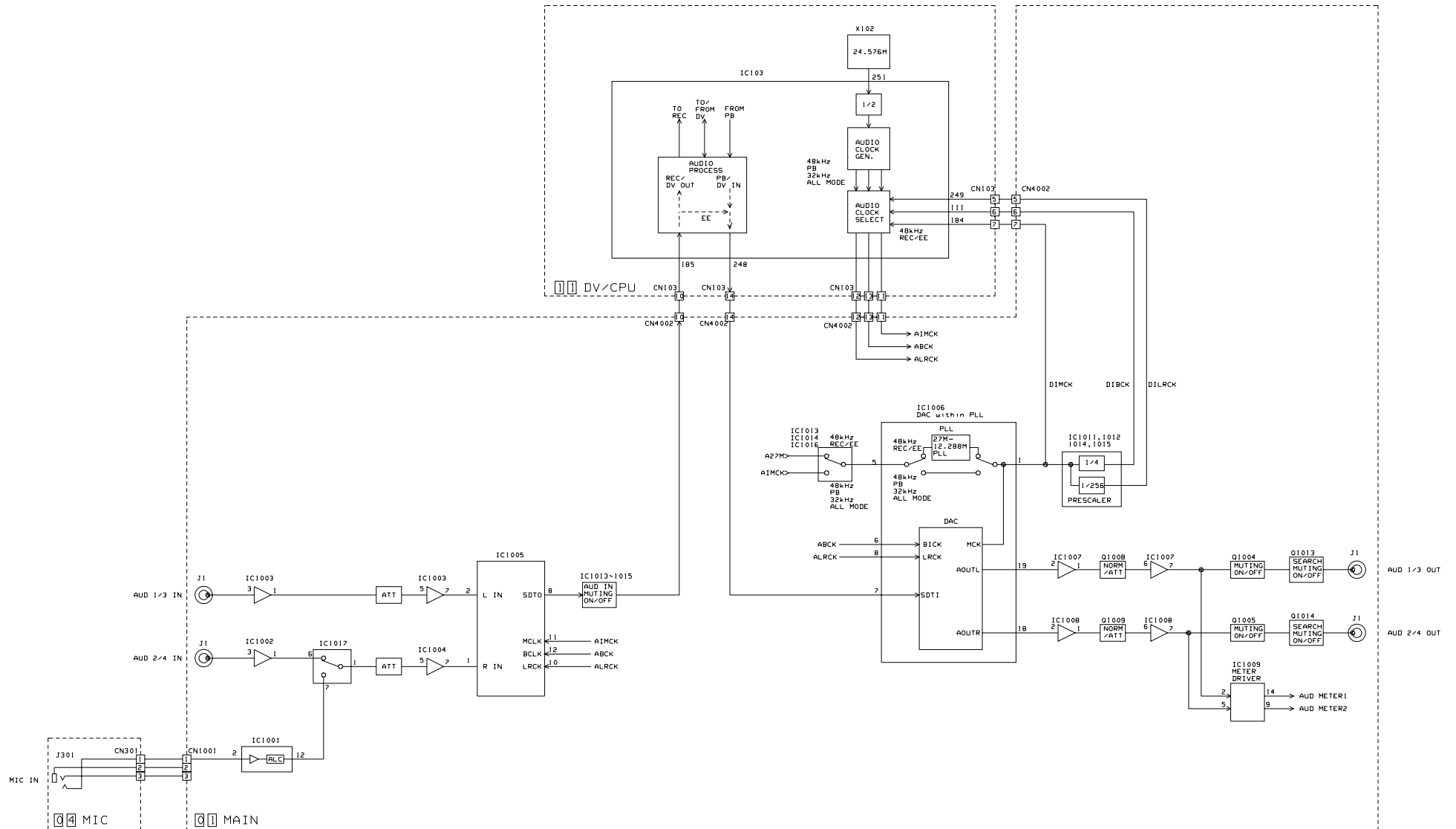
5.2 SYSTEM CONTROL BLOCK DIAGRAM



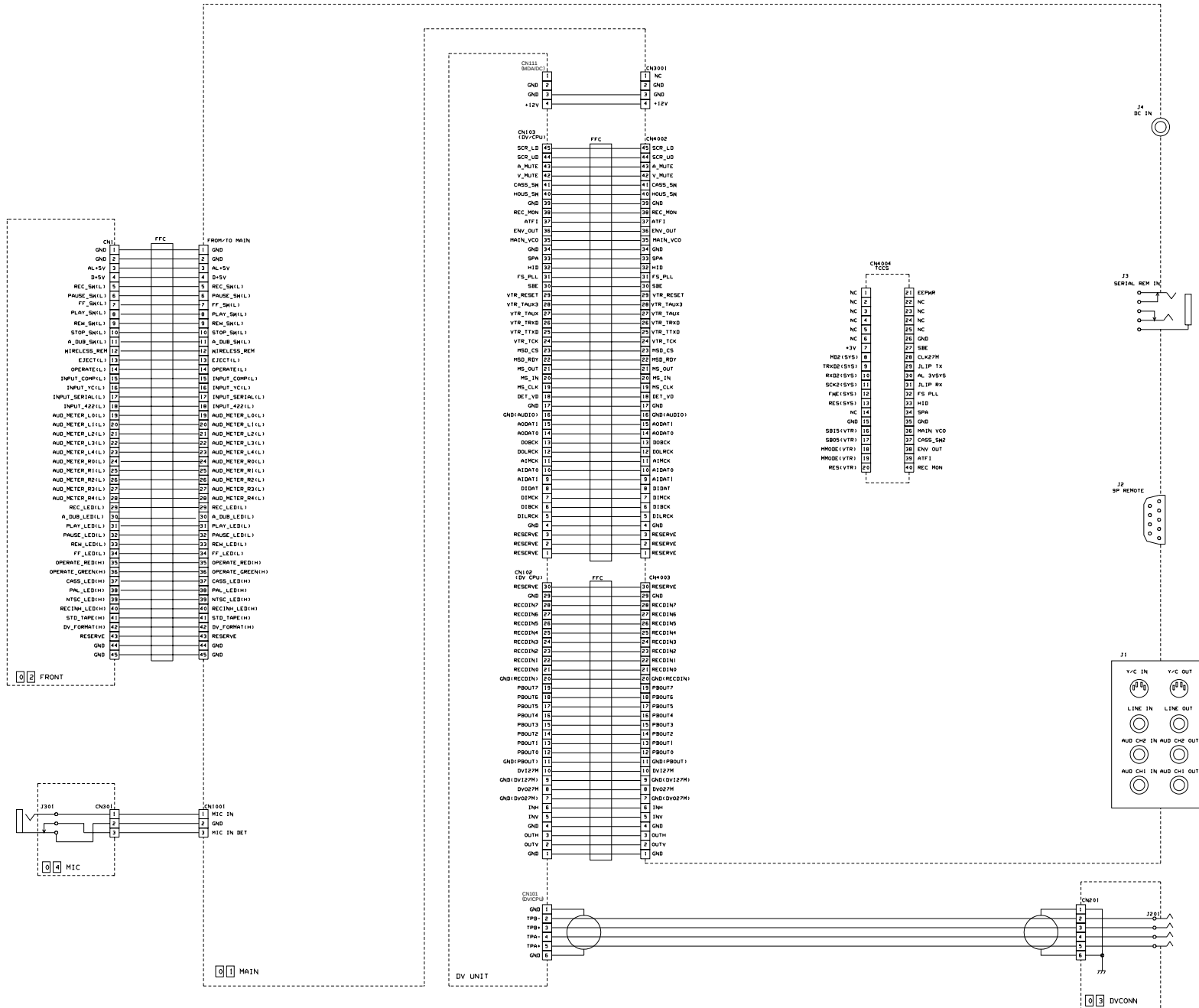
5.3 VIDEO BLOCK DIAGRAM



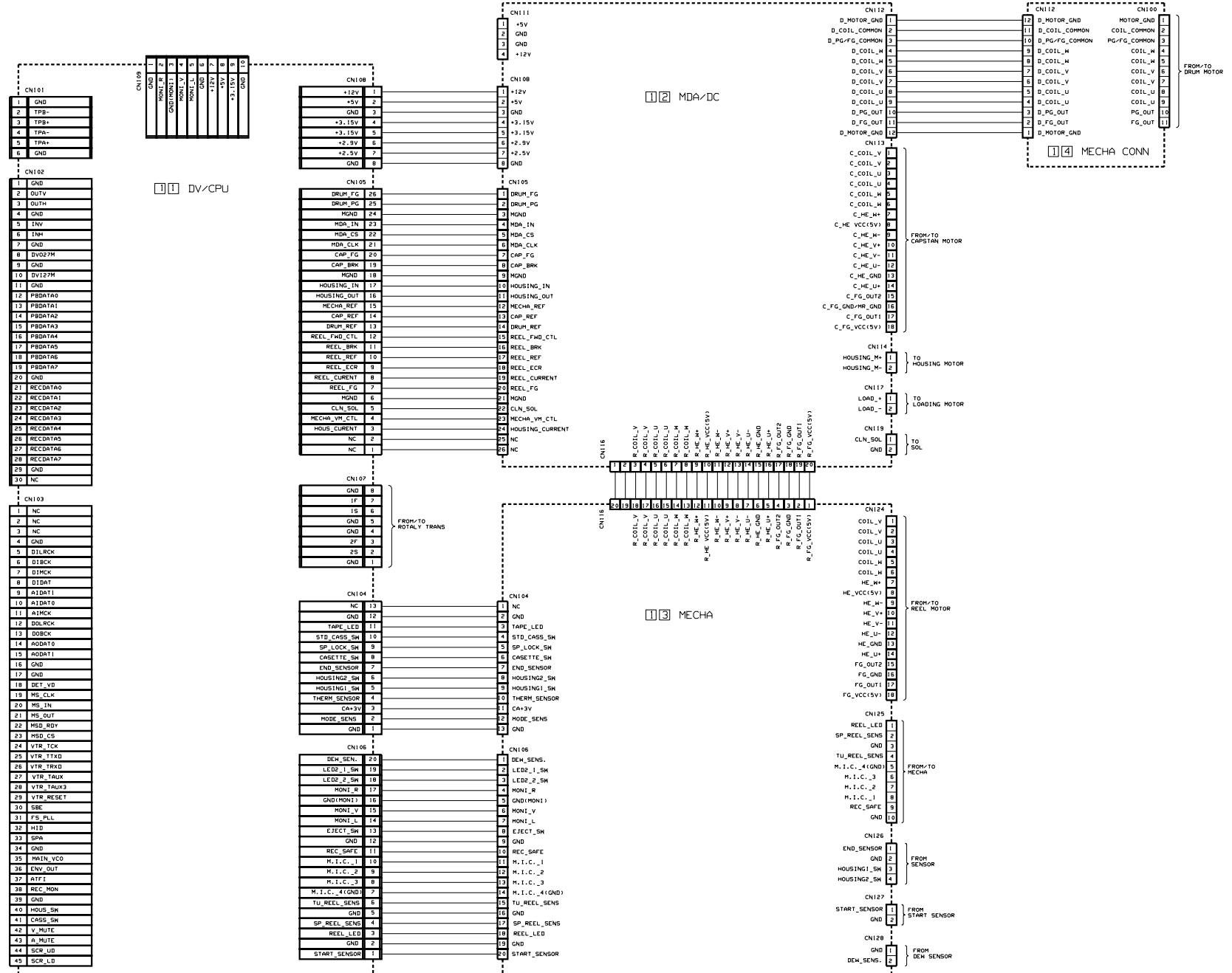
5.4 AUDIO BLOCK DIAGRAM



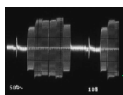
5.5 OVERALL WIRING DIAGRAM



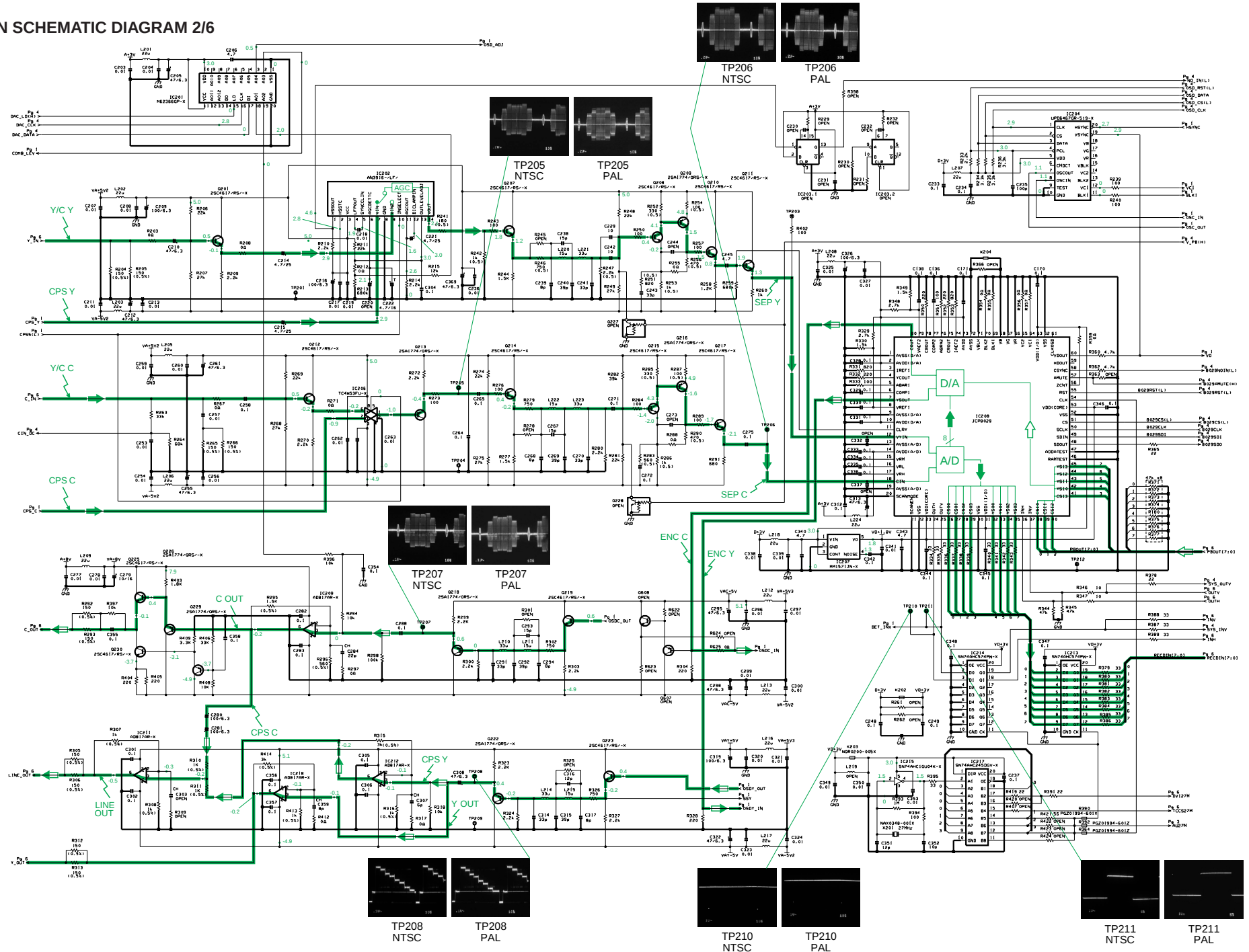
5.6 DV UNIT OVERALL WIRING DIAGRAM

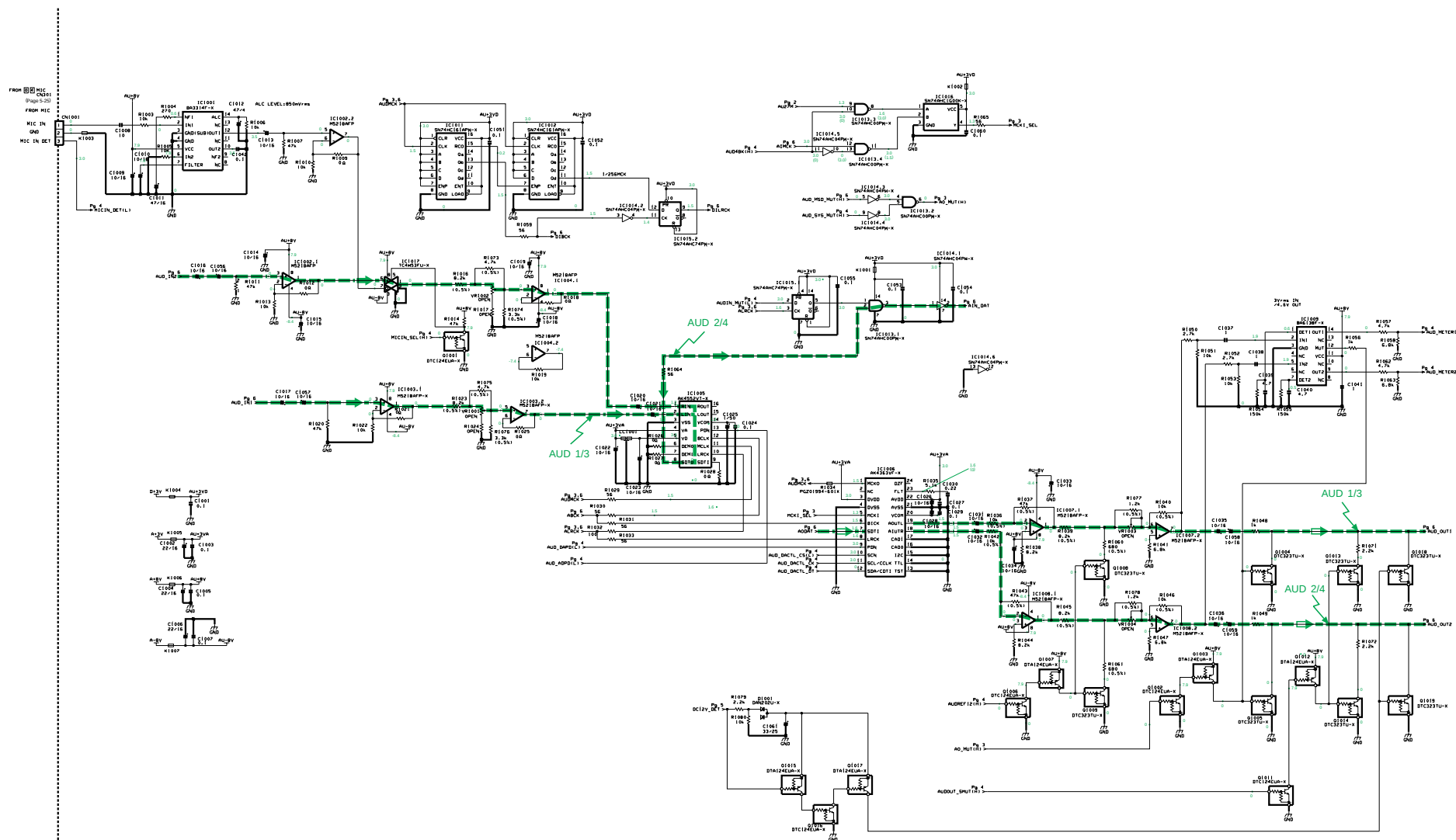


5.7 MAIN SCHEMATIC DIAGRAM 1/6

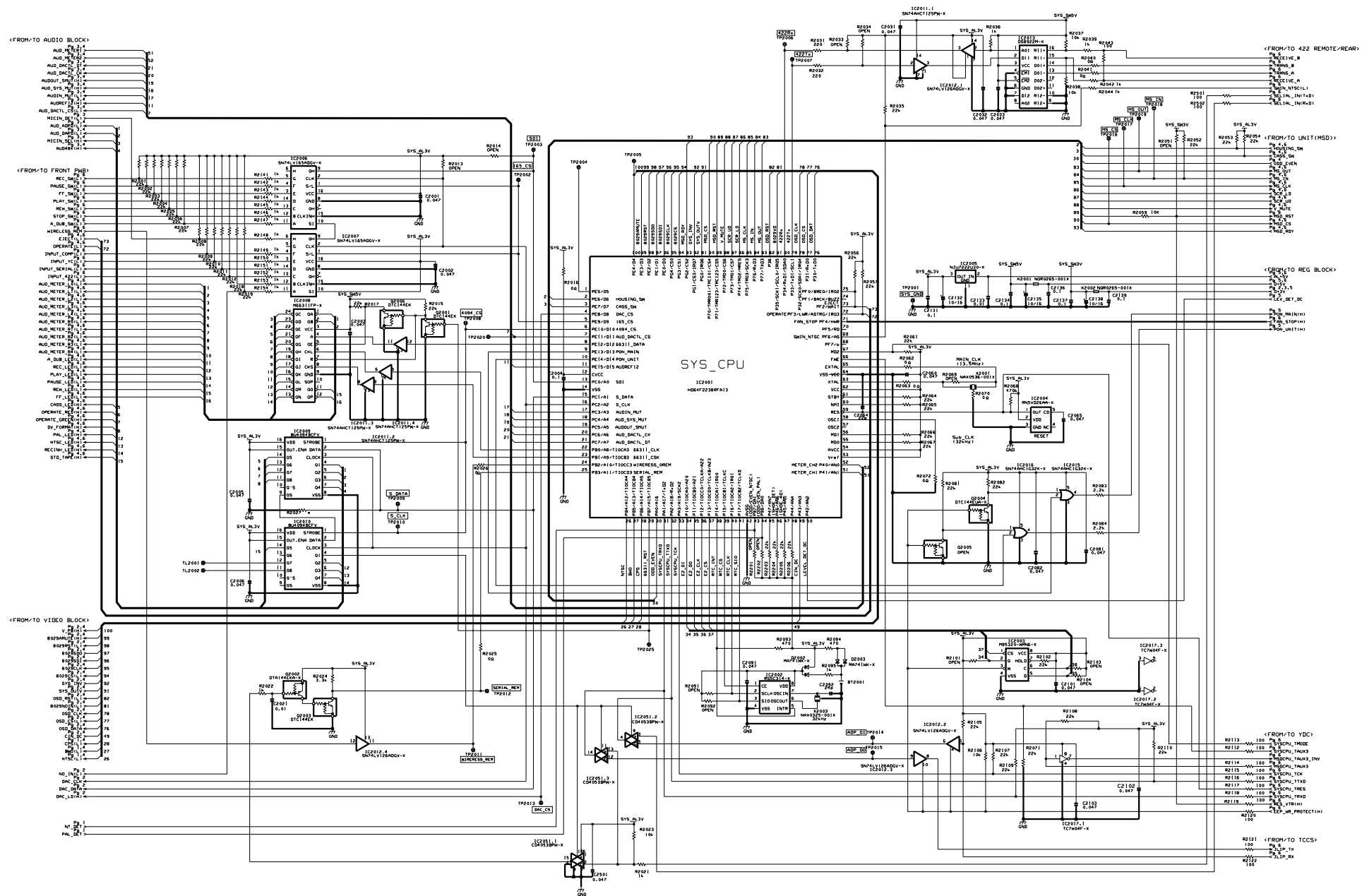


MAIN SCHEMATIC DIAGRAM 2/6





MAIN SCHEMATIC DIAGRAM 4/6



MAIN SCHEMATIC DIAGRAM 5/6

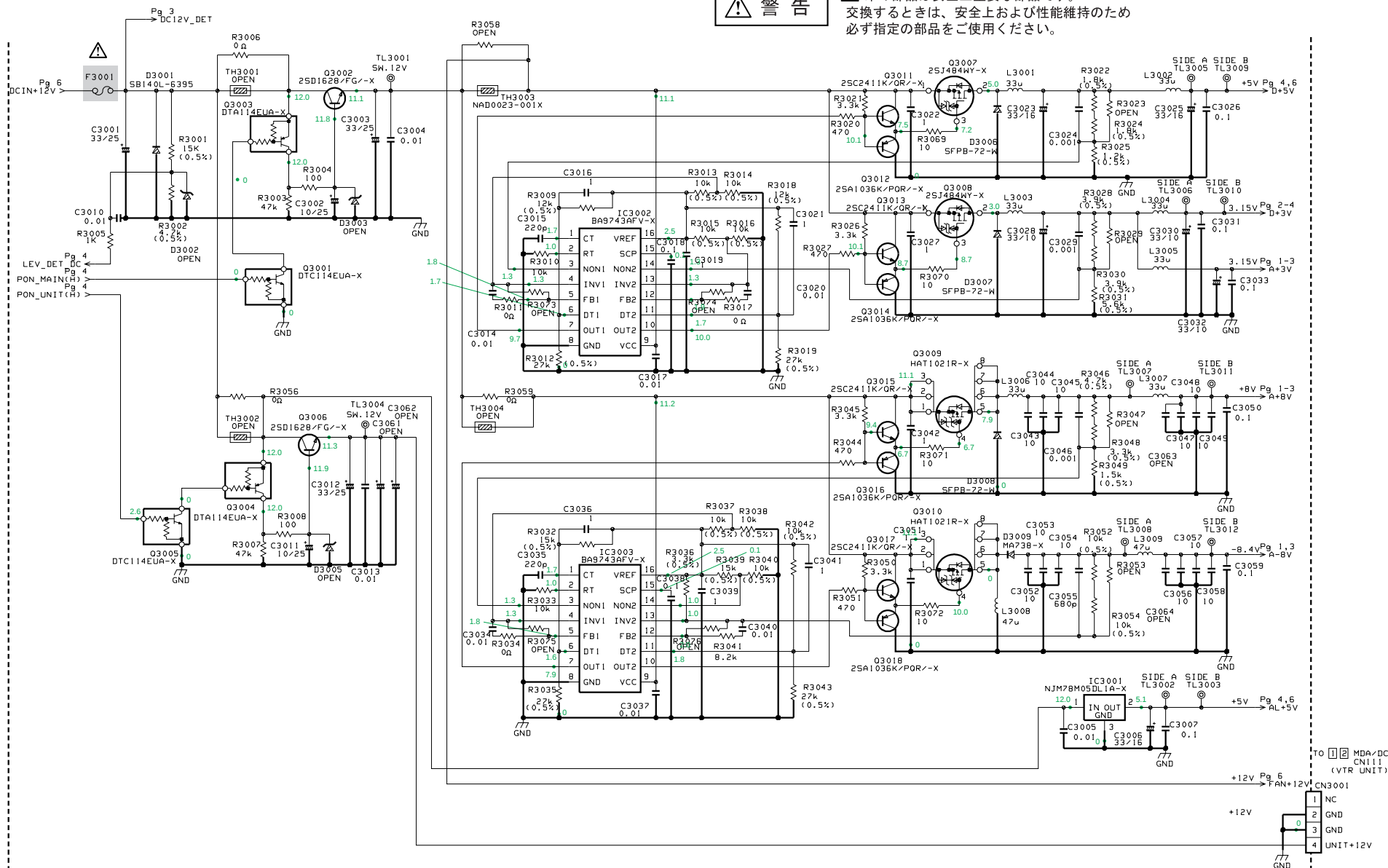
IMPORTANT SAFETY NOTICE:

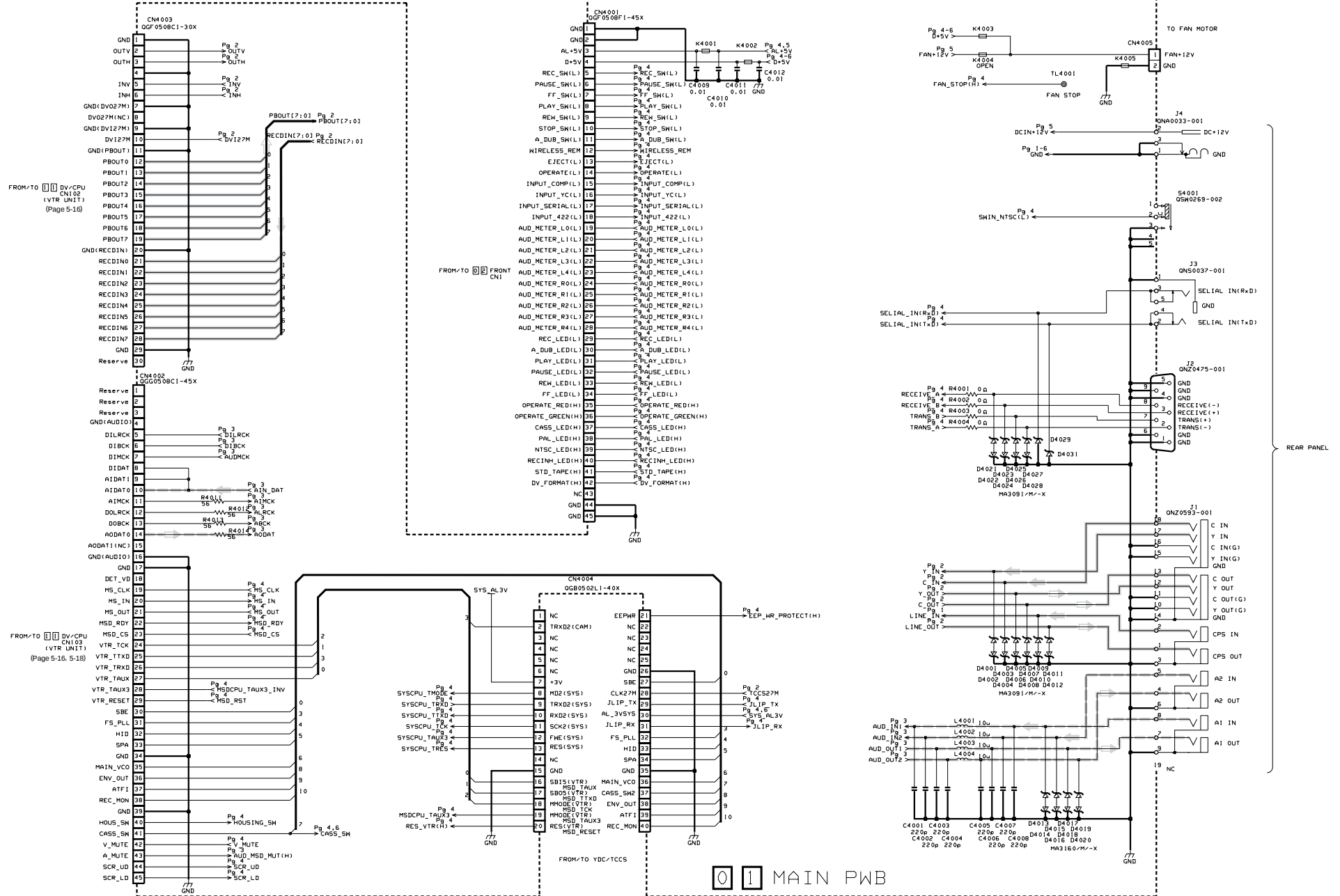
COMPONENTS IDENTIFIED WITH THE MARK  HAVE THE SPECIAL CHARACTERISTICS FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS, USE ONLY THE SAME TYPE.

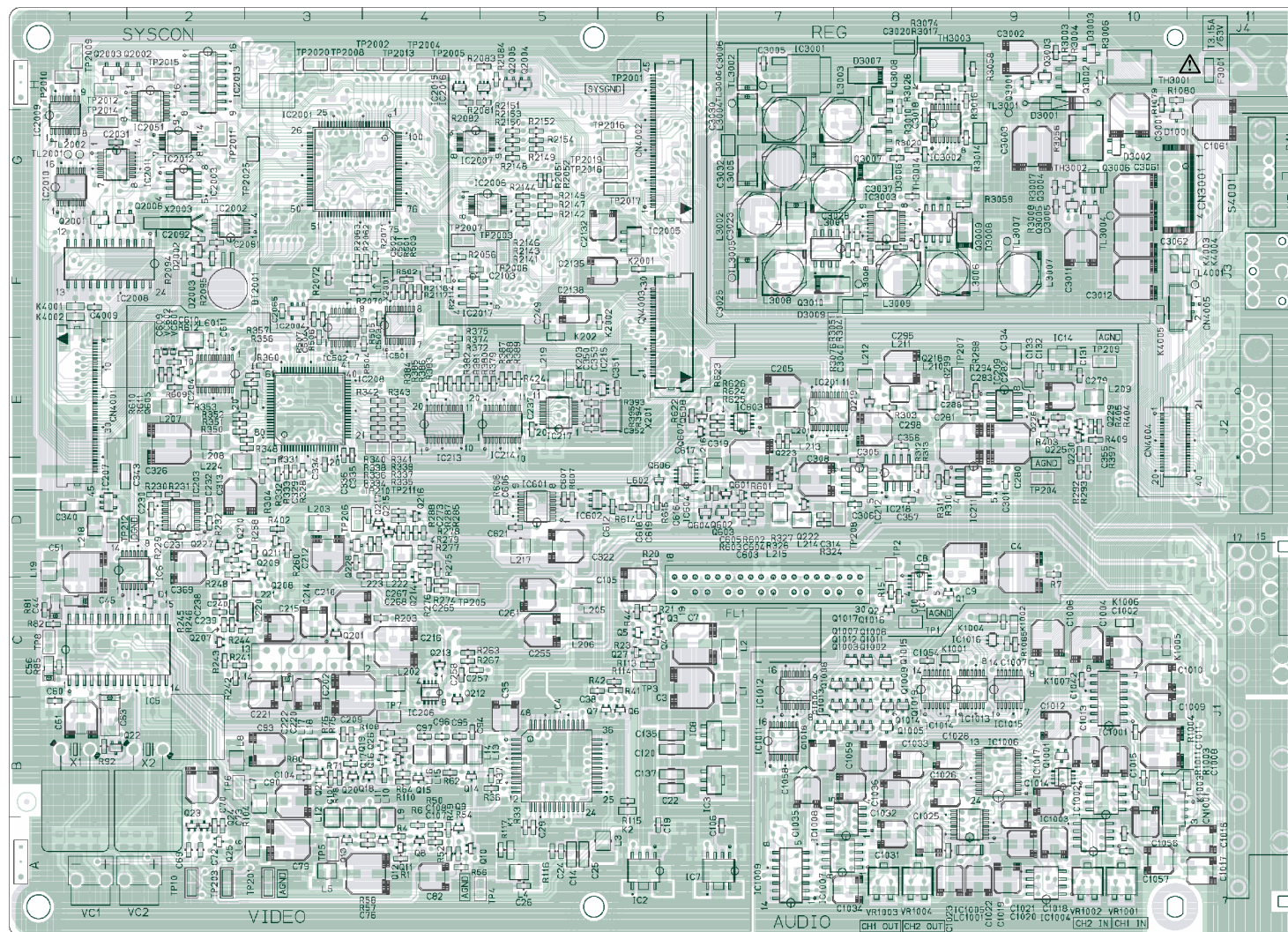


⚠ 印の部品は安全上重要な部品です。

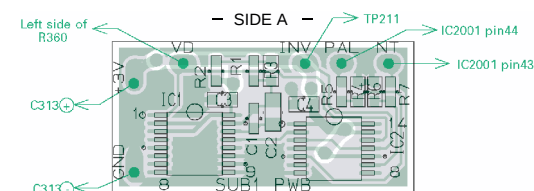
交換するときは、安全上および性能維持のため必ず指定の部品をご使用ください。







— SUB1 CIRCUIT BOARD —



IMPORTANT SAFETY NOTICE:

COMPONENTS IDENTIFIED WITH THE MARK  HAVE THE SPECIAL CHARACTERISTICS FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS, USE ONLY THE SAME TYPE.

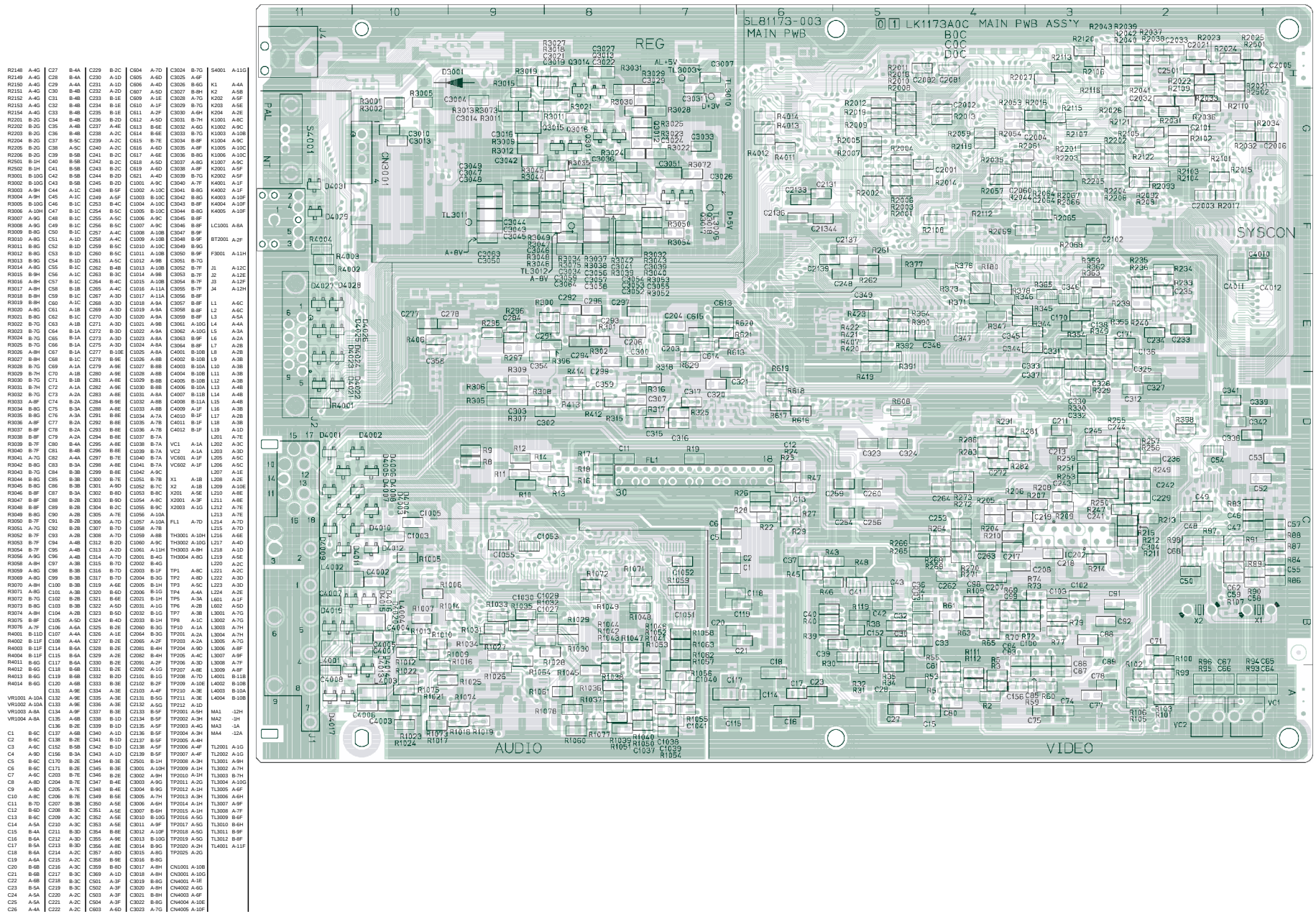


 印の部品は安全上重要な部品です。交換するときは、安全上および性能維持のため必ず指定の部品をご使用ください。

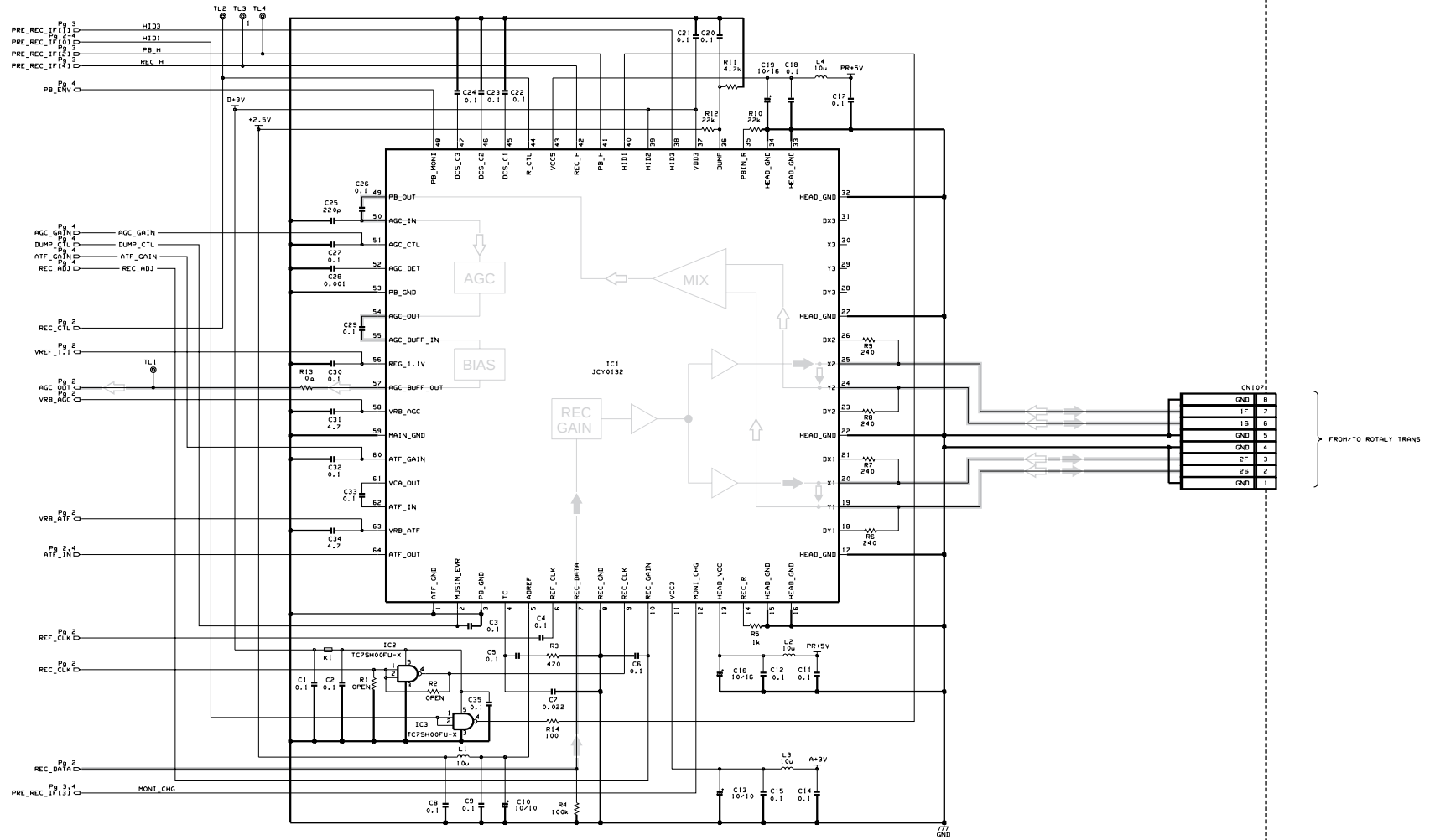
● ADDRESS TABLE OF BOARD PARTS
Each address may have an address error by one interval.

Side	A-1C	Y axis	X axis
IC1	A8D	Q005	A-1E
IC2	A5A	Q006	A-1D
IC3	A4B	Q007	A-1C
IC4	A5B	Q008	A-1B
IC5	A1C	Q009	A-1A
IC6	A1D	Q010	A-1A
IC7	A6A	Q013	A-7B
IC8	A4B	Q014	A-7B
IC9	A4B	Q015	A-7B
IC10	A4B	Q016	A-7B
IC11	A7E	Q016	A-7C
IC12	A3C	Q017	A-7C
IC13	A1D	Q018	A-7C
IC14	A5E	Q019	A-7C
IC15	A7E	Q021	A-3G
IC16	A7E	Q021	A-3G
IC17	A3C	Q022	A-3H
IC18	A3D	Q023	A-3H
IC19	A3D	Q024	A-3H
IC20	A3D	Q025	A-3H
IC21	A3D	Q026	A-3H
IC22	A3D	Q027	A-3H
IC23	A3D	Q028	A-3H
IC24	A3D	Q029	A-3H
IC25	A3D	Q030	A-3H
IC26	A3D	Q031	A-3H
IC27	A3D	Q032	A-3H
IC28	A3D	Q033	A-3H
IC29	A3D	Q034	A-3H
IC30	A3D	Q035	A-3H
IC31	A3D	Q036	A-3H
IC32	A3D	Q037	A-3H
IC33	A3D	Q038	A-3H
IC34	A3D	Q039	A-3H
IC35	A3D	Q040	A-3H
IC36	A3D	Q041	A-3H
IC37	A3D	Q042	A-3H
IC38	A3D	Q043	A-3H
IC39	A3D	Q044	A-3H
IC40	A3D	Q045	A-3H
IC41	A3D	Q046	A-3H
IC42	A3D	Q047	A-3H
IC43	A3D	Q048	A-3H
IC44	A3D	Q049	A-3H
IC45	A3D	Q050	A-3H
IC46	A3D	Q051	A-3H
IC47	A3D	Q052	A-3H
IC48	A3D	Q053	A-3H
IC49	A3D	Q054	A-3H
IC50	A3D	Q055	A-3H
IC51	A3D	Q056	A-3H
IC52	A3D	Q057	A-3H
IC53	A3D	Q058	A-3H
IC54	A3D	Q059	A-3H
IC55	A3D	Q060	A-3H
IC56	A3D	Q061	A-3H
IC57	A3D	Q062	A-3H
IC58	A3D	Q063	A-3H
IC59	A3D	Q064	A-3H
IC60	A3D	Q065	A-3H
IC61	A3D	Q066	A-3H
IC62	A3D	Q067	A-3H
IC63	A3D	Q068	A-3H
IC64	A3D	Q069	A-3H
IC65	A3D	Q070	A-3H
IC66	A3D	Q071	A-3H
IC67	A3D	Q072	A-3H
IC68	A3D	Q073	A-3H
IC69	A3D	Q074	A-3H
IC70	A3D	Q075	A-3H
IC71	A3D	Q076	A-3H
IC72	A3D	Q077	A-3H
IC73	A3D	Q078	A-3H
IC74	A3D	Q079	A-3H
IC75	A3D	Q080	A-3H
IC76	A3D	Q081	A-3H
IC77	A3D	Q082	A-3H
IC78	A3D	Q083	A-3H
IC79	A3D	Q084	A-3H
IC80	A3D	Q085	A-3H
IC81	A3D	Q086	A-3H
IC82	A3D	Q087	A-3H
IC83	A3D	Q088	A-3H
IC84	A3D	Q089	A-3H
IC85	A3D	Q090	A-3H
IC86	A3D	Q091	A-3H
IC87	A3D	Q092	A-3H
IC88	A3D	Q093	A-3H
IC89	A3D	Q094	A-3H
IC90	A3D	Q095	A-3H
IC91	A3D	Q096	A-3H
IC92	A3D	Q097	A-3H
IC93	A3D	Q098	A-3H
IC94	A3D	Q099	A-3H
IC95	A3D	Q100	A-3H
IC96	A3D	Q101	A-3H
IC97	A3D	Q102	A-3H
IC98	A3D	Q103	A-3H
IC99	A3D	Q104	A-3H
IC100	A3D	Q105	A-3H
IC101	A3D	Q106	A-3H
IC102	A3D	Q107	A-3H
IC103	A3D	Q108	A-3H
IC104	A3D	Q109	A-3H
IC105	A3D	Q110	A-3H
IC106	A3D	Q111	A-3H
IC107	A3D	Q112	A-3H
IC108	A3D	Q113	A-3H
IC109	A3D	Q114	A-3H
IC110	A3D	Q115	A-3H
IC111	A3D	Q116	A-3H
IC112	A3D	Q117	A-3H
IC113	A3D	Q118	A-3H
IC114	A3D	Q119	A-3H
IC115	A3D	Q120	A-3H
IC116	A3D	Q121	A-3H
IC117	A3D	Q122	A-3H
IC118	A3D	Q123	A-3H
IC119	A3D	Q124	A-3H
IC120	A3D	Q125	A-3H
IC121	A3D	Q126	A-3H
IC122	A3D	Q127	A-3H
IC123	A3D	Q128	A-3H
IC124	A3D	Q129	A-3H
IC125	A3D	Q130	A-3H
IC126	A3D	Q131	A-3H
IC127	A3D	Q132	A-3H
IC128	A3D	Q133	A-3H
IC129	A3D	Q134	A-3H
IC130	A3D	Q135	A-3H
IC131	A3D	Q136	A-3H
IC132	A3D	Q137	A-3H
IC133	A3D	Q138	A-3H
IC134	A3D	Q139	A-3H
IC135	A3D	Q140	A-3H
IC136	A3D	Q141	A-3H
IC137	A3D	Q142	A-3H
IC138	A3D	Q143	A-3H
IC139	A3D	Q144	A-3H
IC140	A3D	Q145	A-3H
IC141	A3D	Q146	A-3H
IC142	A3D	Q147	A-3H
IC143	A3D	Q148	A-3H
IC144	A3D	Q149	A-3H
IC145	A3D	Q150	A-3H
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IC148	A3D	Q153	A-3H
IC149	A3D	Q154	A-3H
IC150	A3D	Q155	A-3H
IC151	A3D	Q156	A-3H
IC152	A3D	Q157	A-3H
IC153	A3D	Q158	A-3H
IC154	A3D	Q159	A-3H
IC155	A3D	Q160	A-3H
IC156	A3D	Q161	A-3H
IC157	A3D	Q162	A-3H
IC158	A3D	Q163	A-3H
IC159	A3D	Q164	A-3H
IC160	A3D	Q165	A-3H
IC161	A3D	Q166	A-3H
IC162	A3D	Q167	A-3H
IC163	A3D	Q168	A-3H
IC164	A3D	Q169	A-3H
IC165	A3D	Q170	A-3H
IC166	A3D	Q171	A-3H
IC167	A3D	Q172	A-3H
IC168	A3D	Q173	A-3H
IC169	A3D	Q174	A-3H
IC170	A3D	Q175	A-3H
IC171	A3D	Q176	A-3H
IC172	A3D	Q177	A-3H
IC173	A3D	Q178	A-3H
IC174	A3D	Q179	A-3H
IC175	A3D	Q180	A-3H
IC176	A3D	Q181	A-3H
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IC181	A3D	Q186	A-3H
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IC185	A3D	Q190	A-3H
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IC191	A3D	Q196	A-3H
IC192	A3D	Q197	A-3H
IC193	A3D	Q198	A-3H
IC194	A3D	Q199	A-3H
IC195	A3D	Q200	A-3H
IC196	A3D	Q201	A-3H
IC197	A3D	Q202	A-3H
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IC199	A3D	Q204	A-3H
IC200	A3D	Q205	A-3H
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IC202	A3D	Q207	A-3H
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IC206	A3D	Q211	A-3H
IC207	A3D	Q212	A-3H
IC208	A3D	Q213	A-3H
IC209	A3D	Q214	A-3H
IC210	A3D	Q215	A-3H
IC211	A3D	Q216	A-3H
IC212	A3D	Q217	A-3H
IC213	A3D	Q218	A-3H
IC214	A3D	Q219	A-3H
IC215	A3D	Q220	A-3H
IC216	A3D	Q221	A-3H
IC217	A3D	Q222	A-3H
IC218	A3D	Q223	A-3H
IC219	A3D	Q224	A-3H
IC220	A3D	Q225	A-3H
IC221	A3D	Q226	A-3H
IC222	A3D	Q227	A-3H
IC223	A3D	Q228	A-3H
IC224	A3D	Q229	A-3H
IC225	A3D	Q230	A-3H
IC226	A3D	Q231	A-3H
IC227	A3D	Q232	A-3H
IC228	A3D	Q233	A-3H
IC229	A3D	Q234	A-3H
IC230	A3D	Q235	A-3H
IC231	A3D	Q236	A-3H
IC232	A3D	Q237	A-3H
IC233	A3D	Q238	A-3H
IC234	A3D	Q239	A-3H
IC235	A3D	Q240	A-3H
IC236	A3D	Q241	A-3H
IC237	A3D	Q242	A-3H
IC238	A3D	Q243	A-3H
IC239	A3D	Q244	A-3H
IC240	A3D	Q245	A-3H
IC241	A3D	Q246	A-3H
IC242	A3D	Q247	A-3H
IC243	A3D	Q248	A-3H
IC244	A3D	Q249	A-3H
IC245	A3D	Q250	A-3H
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IC252	A3D	Q257	A-3H
IC253	A3D	Q258	A-3H
IC254	A3D	Q259	A-3H
IC255	A3D	Q260	A-3H
IC256	A3D	Q261	A-3H
IC257	A3D	Q262	A-3H
IC258	A3D	Q263	A-3H
IC259	A3D	Q264	A-3H
IC260	A3D	Q265	A-3H
IC261	A3D	Q266	A-3H
IC262	A3D	Q267	A-3H
IC263	A3D	Q268	A-3H
IC264	A3D	Q269	A-3H
IC265	A3D	Q270	A-3H
IC266	A3D	Q271	A-3H
IC267	A3D	Q272	A-3H
IC268	A3D	Q273	A-3H
IC269	A3D	Q274	A-3H
IC270	A3D	Q275	A-3H
IC271	A3D	Q276	A-3H
IC272	A3D	Q277	A-3H
IC273	A3D	Q278	A-3H
IC274	A3D	Q279	A-3H
IC275	A3D	Q280	A-3H
IC276	A3D	Q281	A-3H
IC277	A3D	Q282	A-3H
IC278	A3D	Q283	A-3H
IC279	A3D	Q284	A-3H
IC280	A3D	Q285	A-3H
IC281	A3D	Q286	A-3H
IC282	A3D	Q287	A-3H
IC283	A3D	Q288	A-3H
IC284	A3D	Q289	A-3H
IC285	A3D	Q290	A-3H
IC286	A3D	Q291	A-3H
IC287	A3D	Q292	A-3H
IC288	A3D	Q293	A-3H
IC289	A3D	Q294	A-3H
IC290	A3D	Q295	A-3H
IC291	A3D	Q296	A-3H
IC292	A3D	Q297	A-3H
IC293	A3D	Q298	A-3H
IC294	A3D	Q299	A-3H
IC295	A3D	Q300	A-3H
IC296	A3D	Q301	A-3H
IC297	A3D	Q302	A-3H
IC298	A3D	Q303	A-3H
IC299	A3D	Q304	A-3H
IC300	A3D	Q305	A-3H
IC301	A3D	Q306	

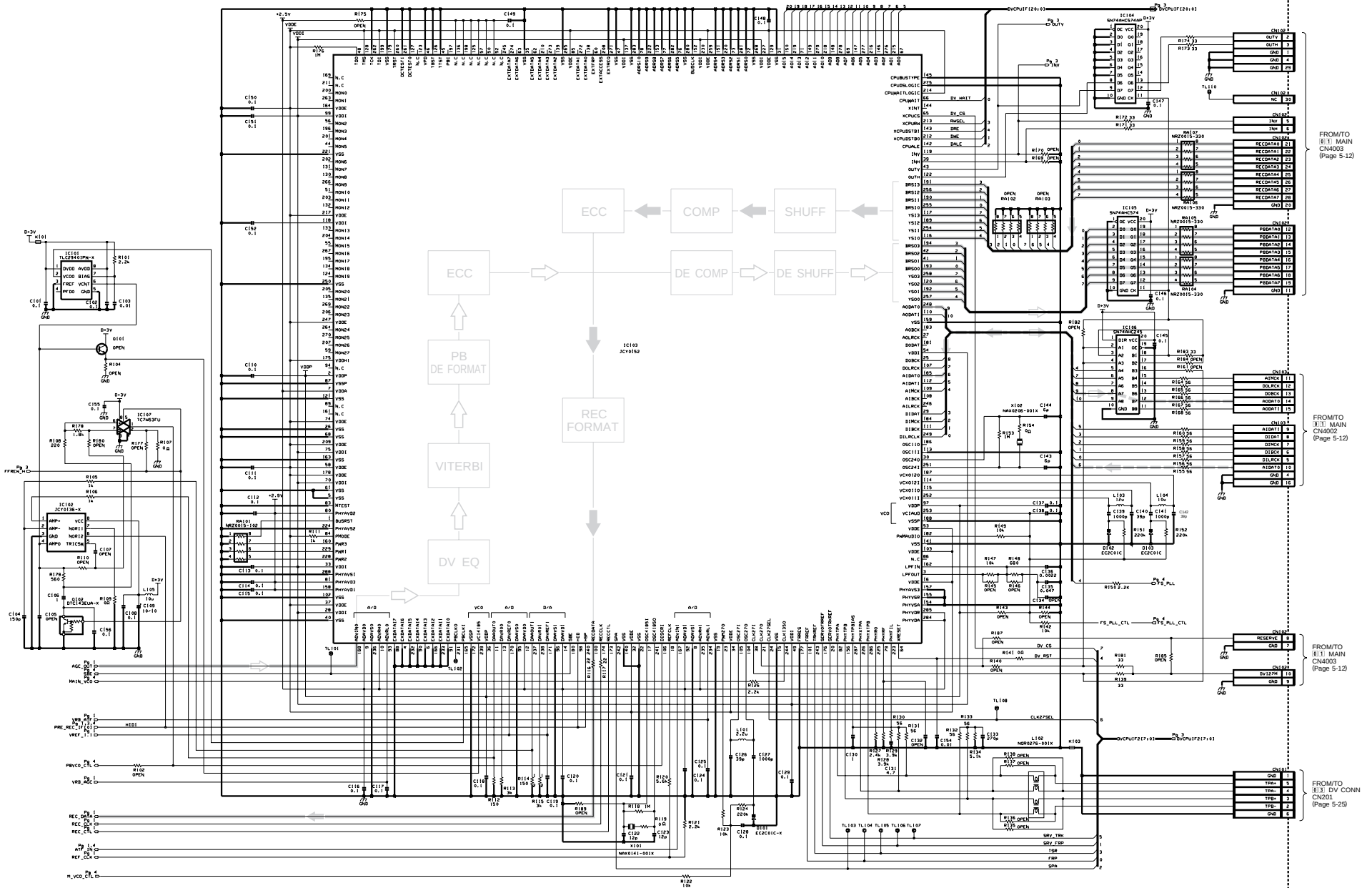
- SIDE B -

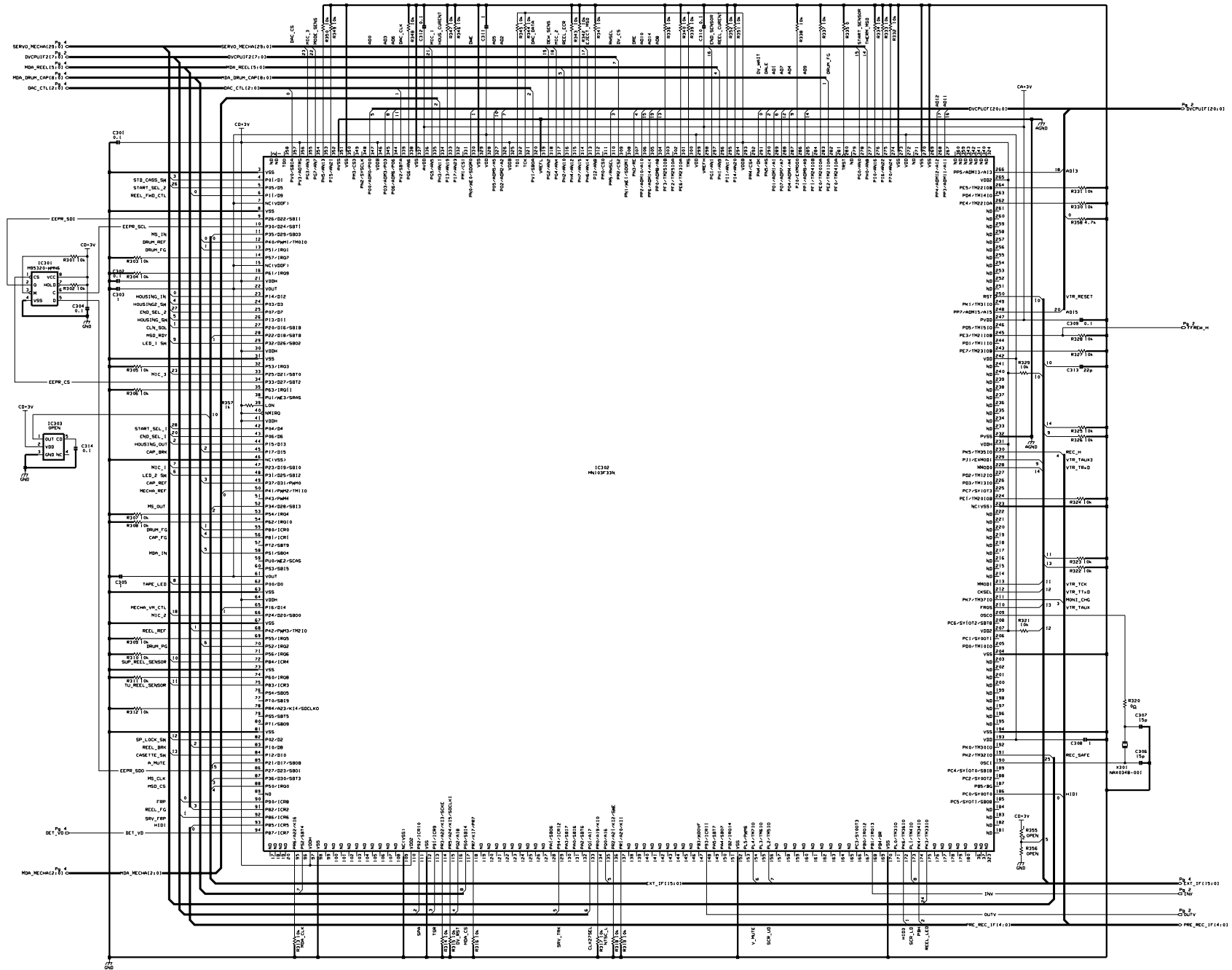


DV/CPU

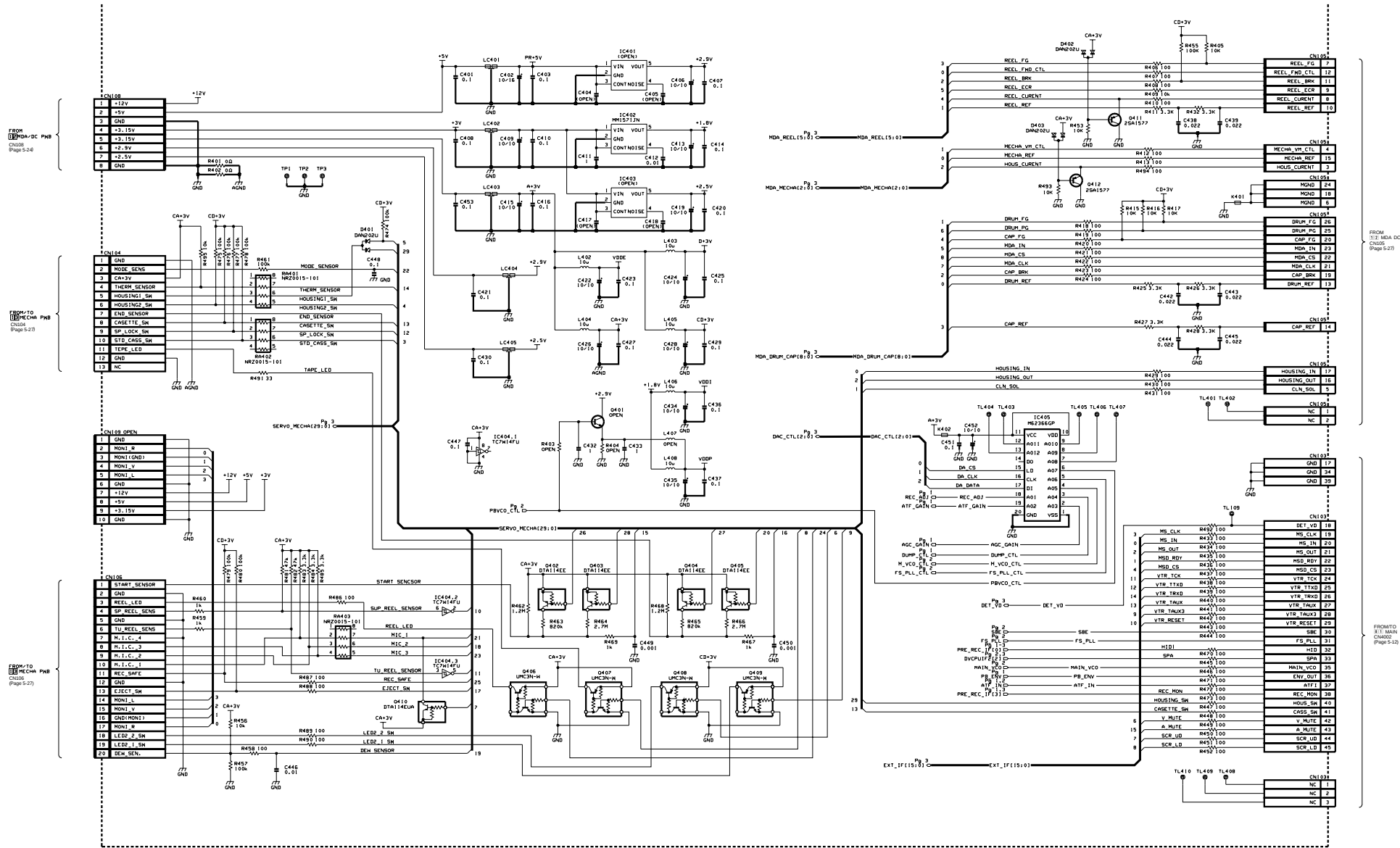


DV/CPU SCHEMATIC DIAGRAM 2/4





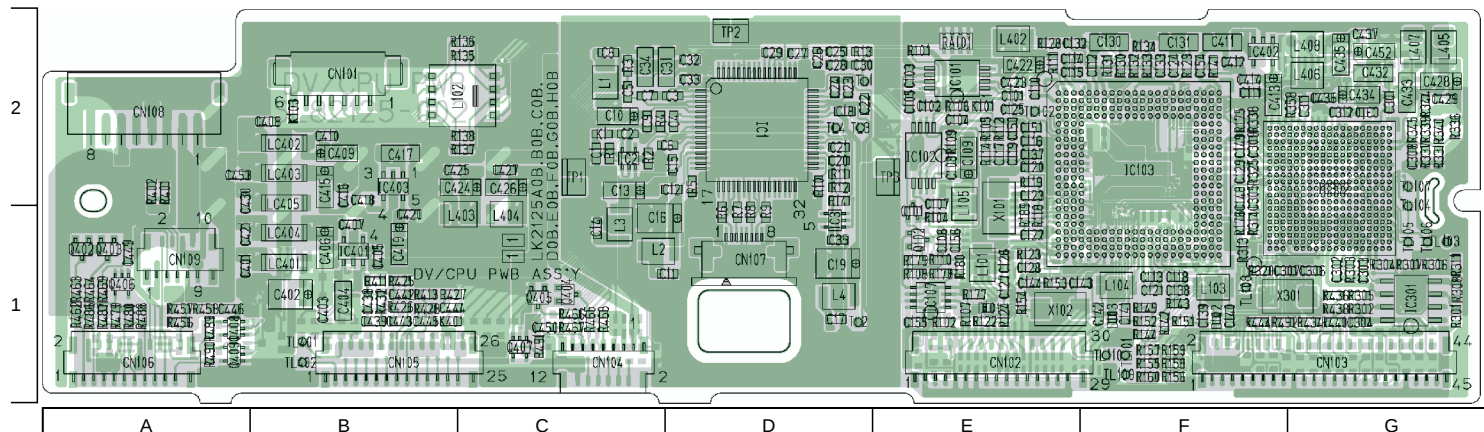
DV/CPU SCHEMATIC DIAGRAM 4/4



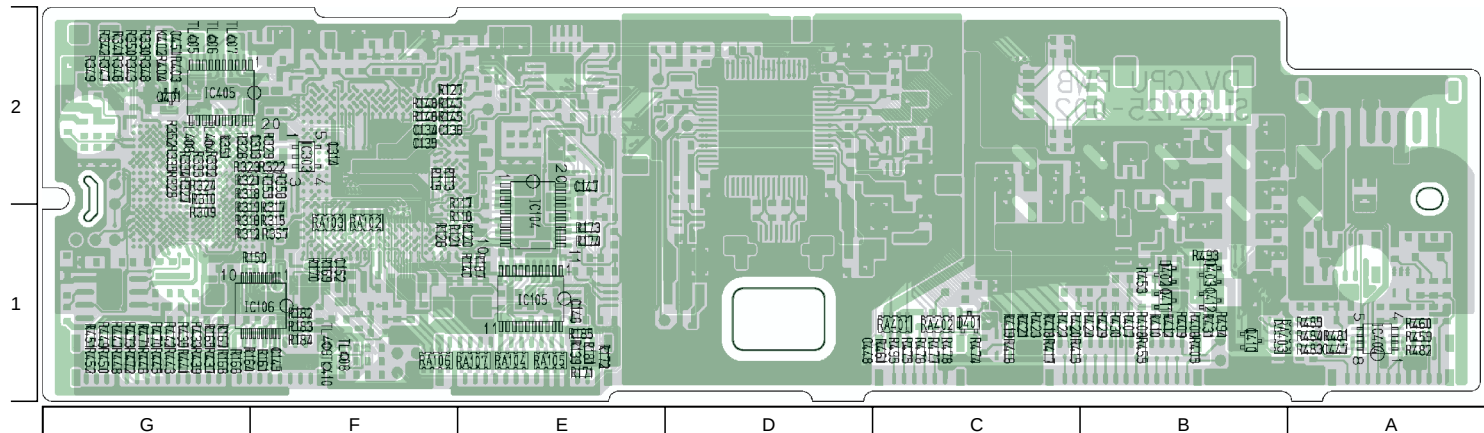
5.10 DV/CPU CIRCUIT BOARD

5-19

— SIDE A —



— SIDE B —



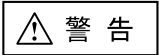
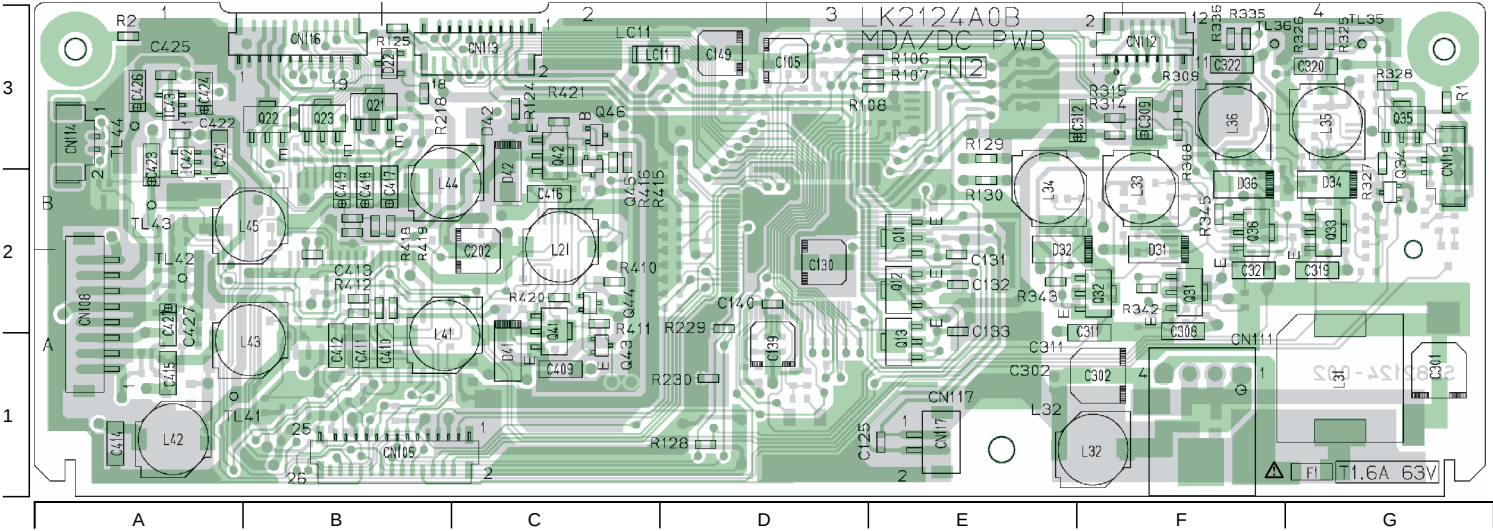
● ADDRESS TABLE OF BOARD PARTS
Each address may have an address error by one interval.

Side A-1C
Y axis
X axis

IC1	A-2D	R136	A-2C	R339	A-2G	R473	B-1G	C119	A-2E	C439	A-1B
IC2	A-2C	R137	A-2C	R340	A-2G	R474	B-1C	C120	A-2E	C442	A-1B
IC3	A-1D	R138	A-2C	R341	B-2G	R475	B-1C	C121	A-1F	C443	A-1B
IC101	A-2E	R139	B-1E	R342	B-2G	R476	B-1C	C122	A-1E	C444	A-1B
IC102	A-2E	R140	B-1E	R343	B-2G	R477	B-1C	C123	A-2E	C445	A-1B
IC103	A-2F	R141	A-2F	R344	A-2G	R478	B-1C	C124	A-2F	C446	A-1A
IC104	B-1E	R142	B-1E	R345	B-2G	R479	B-1C	C125	A-2F	C447	B-1A
IC105	B-1E	R143	A-1F	R346	B-2G	R480	A-1A	C126	A-1E	C448	B-1C
IC106	B-1F	R144	A-1F	R347	B-2G	R481	B-1A	C127	A-1E	C449	A-1A
IC107	A-1E	R145	B-2F	R348	B-2G	R482	B-1A	C128	A-1E	C450	A-1C
IC301	A-1G	R146	B-2F	R349	B-2G	R483	B-1A	C129	A-2F	C451	B-2G
IC302	A-2G	R147	B-2F	R350	B-2G	R484	B-1A	C130	A-2F	C452	A-2G
IC303	B-2F	R148	B-2F	R351	B-2G	R485	B-1A	C131	A-2F	C453	A-2A
IC401	B-1E	R149	A-1F	R352	B-2G	R486	A-1A	C132	A-2F		
IC402	A-2F	R150	B-1F	R353	B-2F	R487	A-1A	C133	A-2F	X101	A-1E
IC403	A-2B	R151	A-1F	R354	B-2F	R488	A-1A	C134	B-2F	X102	A-1E
IC404	B-1A	R152	A-1F	R355	B-1F	R489	A-1A	C135	B-2F	X301	A-1G
IC405	B-2G	R153	A-1E	R356	A-2G	R490	A-1A	C136	B-2F		
		R154	A-1E	R401	A-2A	R491	A-1C	C137	A-2E	TP1	A-2C
Q101	A-1E	R155	A-1F	R402	A-2A	R492	A-1G	C138	A-1F	TP2	A-2D
Q102	A-1E	R156	A-1F	R403	B-2G	R493	B-1B	C139	A-1F	TP3	A-2E
Q401	B-1E	R157	A-1F	R404	B-2G	R494	B-1F	C140	A-1F		
Q402	A-1A	R158	A-1F	R405	B-1B	R495	B-1C	C141	A-1F	CN101	A-2B
Q403	A-1A	R159	A-1F	R406	B-1B			C142	A-1F	CN102	A-1E
Q404	A-1C	R160	A-1F	R407	B-1B	RA101	A-2E	C143	A-1F	CN103	A-1G
Q405	A-1C	R161	B-1F	R408	B-1B	RA102	B-1F	C144	A-1F	CN104	A-1C
Q406	A-1A	R164	B-1F	R409	B-1B	RA103	B-1F	C145	B-1F	CN105	A-1B
Q407	A-1C	R165	B-1G	R410	B-1B	RA104	B-1E	C146	B-1E	CN106	A-1A
Q408	A-1A	R166	B-1G	R411	A-1B	RA105	B-1E	C147	A-1F	CN107	A-1D
Q409	A-1A	R167	B-1G	R412	B-1B	RA106	B-1F	C148	A-2F	CN108	A-2A
Q410	B-1B	R168	B-1G	R413	A-1B	RA107	B-1E	C149	A-2F	CN109	A-1A
Q411	B-1B	R169	B-1F	R415	B-1B	RA401	B-1C	C150	A-2E		
Q412	B-1B	R170	B-1F	R416	B-1C	RA402	B-1C	C151	A-2E	K1	A-2C
		R171	B-1E	R417	B-1C	RA403	B-1A	C152	B-1F	K101	A-2E
D101	A-1E	R172	B-1E	R418	B-1C			C154	A-2F	K103	A-2B
D102	A-1F	R173	B-1E	R419	B-1C	C1	A-2C	C155	A-1E	K401	A-1B
D103	A-1F	R174	B-1E	R420	B-1B	C2	A-2C	C156	A-1E	K402	B-2G
D401	B-1C	R175	A-2F	R421	B-1C	C3	A-2D	C157	A-2G		
D402	B-1B	R176	A-1F	R422	B-1C	C4	A-2D	C302	A-1G	LC401	A-1B
D403	B-1B	R177	A-1E	R423	B-1C	C5	A-2C	C303	A-1G	LC402	A-2B
		R178	A-1E	R424	B-1B	C6	A-2D	C304	A-1G	LC403	A-2B
R1	A-2C	R179	A-1E	R425	A-1B	C7	A-2C	C305	A-2F	LC404	A-1B
R2	A-2C	R180	A-1E	R426	A-1B	C8	A-2C	C306	A-1G	LC405	A-2B
R3	A-2C	R181	B-1E	R427	A-1B	C9	A-2C	C307	A-1G		
R4	A-2D	R182	B-1F	R428	A-1B	C10	A-2C	C308		L1	A-2C
R5	A-2D	R183	B-1F	R429	B-1B	C11	A-1D	C309	A-2F	L2	A-1C
R6	A-1D	R184	B-1F	R430	B-1B	C12	A-2D	C310	A-2G	L3	A-1C
R7	A-1D	R185	B-1E	R431	B-1B	C13	A-2C	C311	A-2G	L4	A-1D
R8	A-1D	R187	B-1E	R432	A-1B	C14	A-1C	C312	A-2G	L101	A-1E
R9	A-1D	R189	A-1E	R433	B-1G	C15	A-2D	C313	B-2F	L102	A-2C
R10	A-2D	R301	A-1G	R434	A-1G	C16	A-1D	C314	B-2F	L103	A-1F
R11	A-2D	R302	A-2F	R435	B-1G	C17	A-1D	C315	A-1F	L104	A-1F
R12	A-2D	R303	A-1G	R436	A-1G	C18	A-2D	C402	A-1B	L105	A-2E
R13	A-2D	R304	A-1G	R437	B-1G	C19	A-1D	C403	A-1B	L402	A-2E
R14	A-2D	R305	A-1G	R438	A-1G	C20	A-2D	C404	A-1B	L403	A-1C
R101	A-2E	R306	A-1G	R439	B-1G	C21	A-2D	C405	A-1B	L404	A-1C
R102	A-1E	R307	A-1G	R440	A-1G	C22	A-2E	C406	A-1B	L405	A-2G
R104	A-1E	R308	A-1G	R441	B-1G	C23	A-2D	C407	A-1B	L406	A-2G
R105	A-2E	R309	B-1G	R442	B-1G	C24	A-2D	C408	A-2B	L407	A-2G
R106	A-2E	R310	B-2G	R443	B-1G	C25	A-2D	C409	A-2B	L408	A-2G
R107	A-1E	R311	A-1G	R444	A-1F	C26	A-2D	C410	A-2B		
R108	A-1E	R312	B-1F	R445	B-1G	C27	A-2D	C411	A-2F	TL1	A-2E
R109	A-2E	R313	A-1F	R446	B-1G	C28	A-2D	C412	A-2F	TL2	A-1D
R110	A-1E	R314	A-1F	R447	B-1G	C29	A-2D	C413	A-2F	TL3	A-2D
R111	A-2E	R315	B-1F	R448	B-1G	C30	A-2D	C414	A-2F	TL4	A-2D
R112	A-2E	R316	B-1F	R449	B-1G	C31	A-2D	C415	A-2B	TL101	A-1F
R113	A-2E	R317	B-2F	R450	B-1G	C32	A-2D	C416	A-2B	TL102	A-1F
R114	A-2E	R318	B-2F	R451	B-1G	C33	A-2D	C417	A-2B	TL103	A-1G
R115	B-2F	R319	B-1F	R452	B-1G	C34	A-2C	C418	A-2B	TL104	A-2G
R116	B-1E	R320	A-1F	R453	B-1B	C35	A-1D	C419	A-1B	TL105	A-1G
R117	B-2E	R321	B-2F	R455	B-1B	C101	A-2E	C420	A-1B	TL106	A-1G
R118	A-1E	R322	B-2F	R456	A-1A	C102	A-2E	C421	A-1A	TL107	A-2G
R119	A-2E	R323	B-2F	R457	A-1A	C103	A-2E	C422	A-2E	TL108	A-1F
R120	B-1E	R324	B-2G	R458	A-1A	C104	A-2E	C423	A-2E	TL109	A-1F
R121	B-1E	R325	A-2F	R459	B-1A	C105	A-2E	C424	A-2C	TL110	A-1F
R122	A-1E	R326	B-2G	R460	B-1A	C106	A-1E	C425	A-2C	TL401	A-1B
R123	A-1E	R327	B-2G	R461	B-1C	C107	A-2E	C426	A-2C	TL402	A-1B
R124	A-1E	R328	B-2G	R462	A-1A	C108	A-2E	C427	A-2C	TL403	B-2G
R126	B-1F	R329	B-2F	R463	A-1A	C109	A-2E	C428	A-2G	TL404	B-2G
R127	B-2F	R330	B-2G	R464	A-1A	C110	A-2E	C429	A-2G	TL405	B-2G
R128	A-2E	R331	A-2G	R465	A-1C	C111	A-2F	C430	A-2A	TL406	B-2G
R129	A-2F	R332	B-2G	R466	A-1C	C112	A-2F	C431	A-2G	TL407	B-2G
R130	A-2F	R333	B-2G	R467	A-1C	C113	A-1F	C432	A-2G	TL408	B-1F
R131	A-2F	R334	B-2G	R468	A-1C	C114	A-2F	C433	A-2G	TL409	B-1F
R132	A-2F	R335	B-2G	R469	A-1A	C115	A-2F	C434	A-2G	TL410	B-1F
R133	A-2F	R336	A-2G	R470	B-1G	C116	A-2E	C435	A-2G		
R134	A-2F	R337	A-2G	R471	B-1G	C117	A-2E	C436	A-2G		
R135	A-2C	R338	A-2F	R472	B-1G	C118	A-1F	C437	A-2E		
								C438	A-1B		

5.11 MDA/DC CIRCUIT BOARD

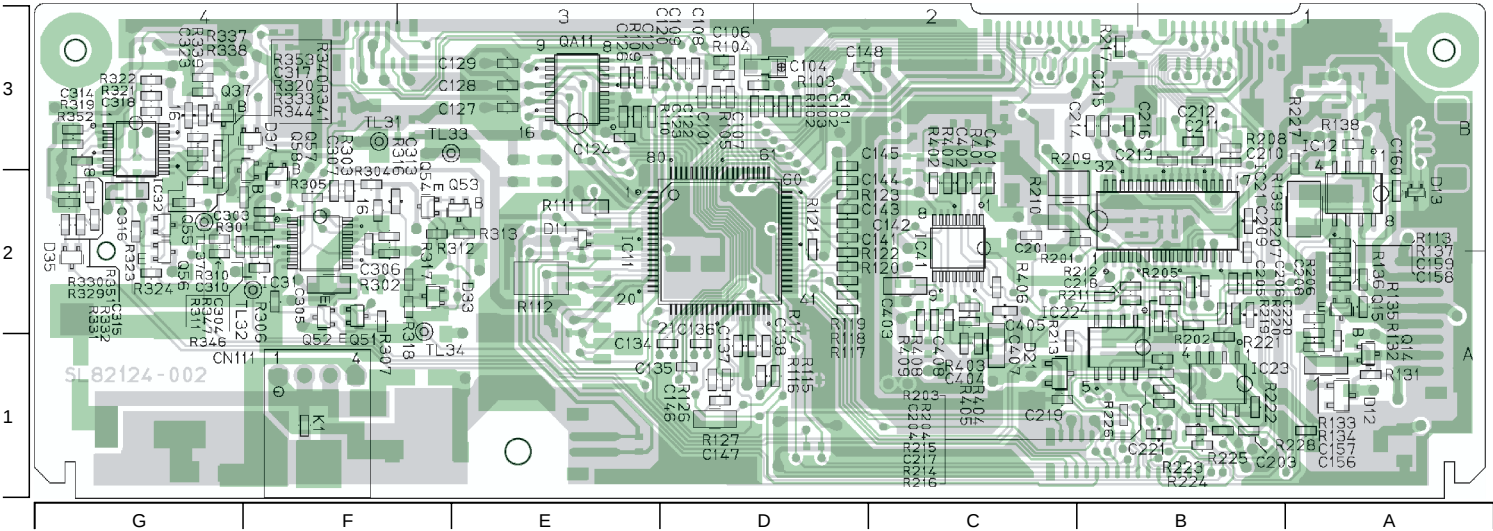
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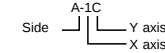
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— SIDE B —

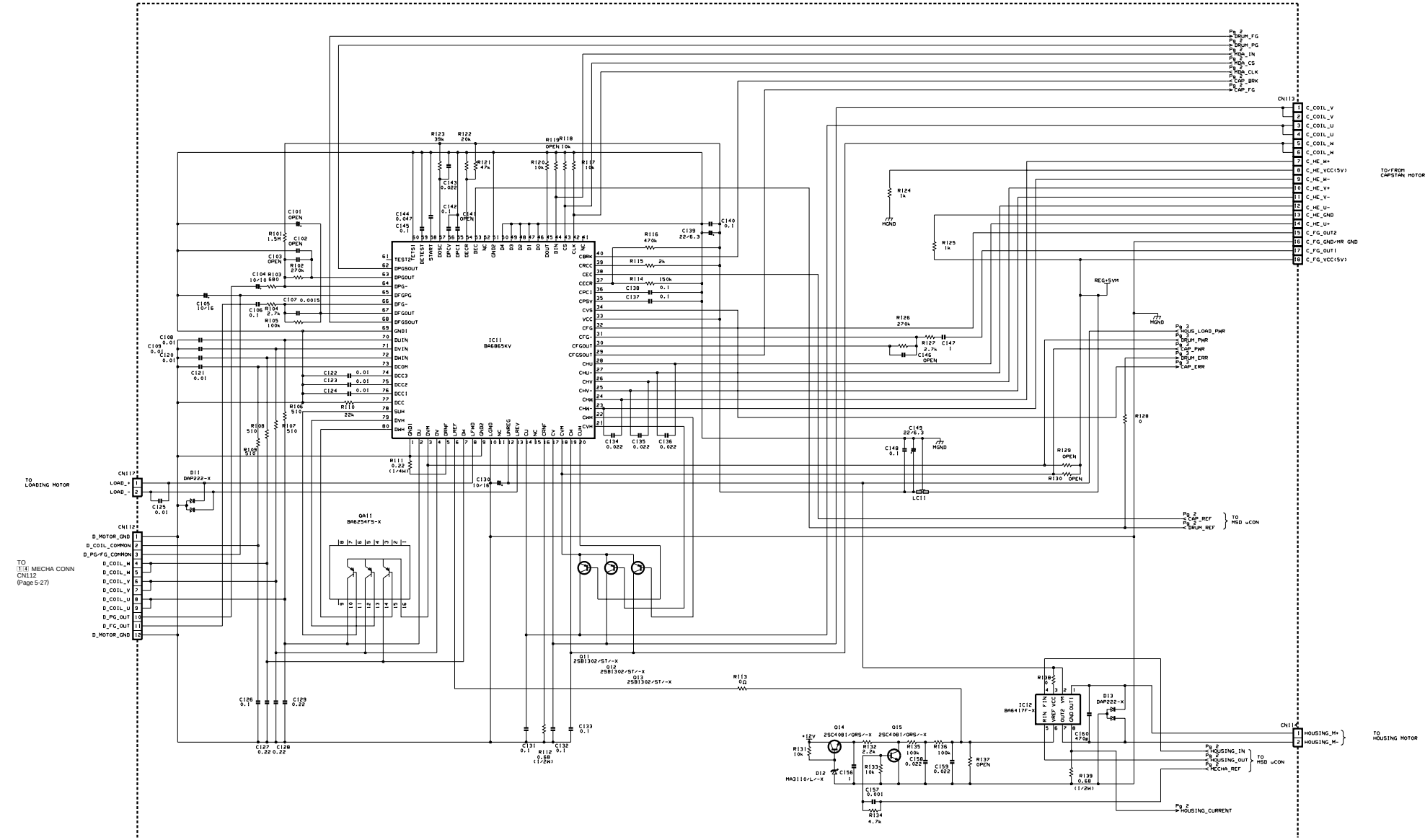


● ADDRESS TABLE OF BOARD PARTS
Each address may have an address error by one interval.

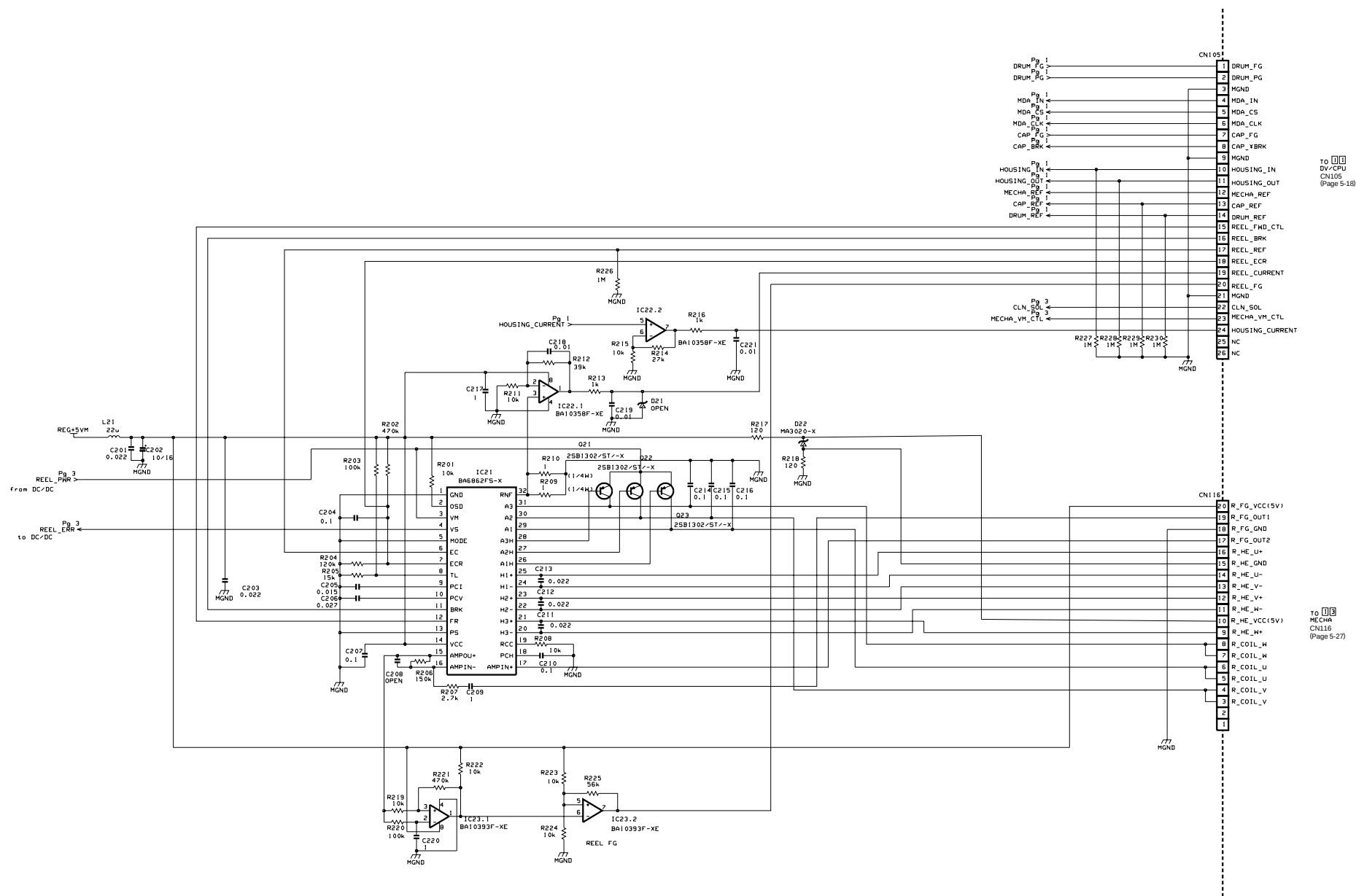


IC11	B-2D	R120	B-2D	R328	A-3G	C142	B-2D	C422	A-3A
IC12	B-2A	R121	B-2D	R329	B-2G	C143	B-2D	C423	A-2A
IC21	B-2B	R122	B-2D	R330	B-2G	C144	B-2D	C424	A-3A
IC22	B-1B	R123	B-2D	R331	B-2G	C145	B-2D	C425	A-3A
IC23	B-1B	R124	A-3C	R332	B-2G	C146	B-1D	C426	A-3A
IC31	B-2F	R125	A-3B	R333	B-2G	C147	B-1D	C427	A-2A
IC32	B-3G	R126	B-1D	R334	B-2F	C148	B-3C		
IC41	B-2C	R127	B-1D	R335	A-3F	C149	A-3D	CN105	A-1B
IC42	A-2A	R128	A-1D	R336	A-3F	C156	B-1A	CN108	A-2A
IC43	A-3A	R129	A-3E	R337	B-3G	C157	B-1A	CN111	A-1F
		R130	A-2E	R338	B-3G	C158	B-2A	CN112	A-3F
Q11	A-2E	R131	B-1A	R339	B-3G	C159	B-2A	CN113	A-3C
Q12	A-2E	R132	B-1A	R340	B-3G	C160	B-2A	CN114	A-3A
Q13	A-1E	R133	B-2A	R341	B-2G	C201	B-2C	CN116	A-3B
Q14	B-1A	R134	B-1A	R342	A-2F	C202	A-2C	CN117	A-1E
Q15	B-2A	R135	B-2A	R343	A-2E	C203	B-1B	CN119	A-2G
Q21	A-3B	R136	B-2A	R344	B-2G	C204	B-2B		
Q22	A-3B	R137	B-2A	R345	A-2F	C205	B-2B	K1	B-1F
Q23	A-3B	R138	B-3A	R346	B-2F	C206	B-2B		
Q31	A-2F	R139	B-2A	R347	B-2F	C207	A-2B	LC11	A-3C
Q32	A-2F	R201	B-2B	R348	B-2F	C208	B-2B		
Q33	A-2G	R202	B-2B	R351	B-2G	C209	B-2B	F1	A-1G
Q34	A-2G	R203	B-2B	R352	B-3G	C210	B-2B		
Q35	A-3G	R204	B-2B	R353	B-3G	C211	B-3B	L21	A-2C
Q36	A-2F	R205	B-2B	R401	B-2C	C212	B-3B	L31	A-1G
Q37	B-3G	R206	B-2B	R402	B-2C	C213	B-3B	L32	A-1F
Q41	A-1C	R207	B-2B	R403	B-2C	C214	B-3B	L33	A-2F
Q42	A-3C	R208	B-3B	R404	B-1C	C215	B-3B	L34	A-2E
Q43	A-1C	R209	B-2C	R405	B-1C	C216	B-3B	L35	A-3G
Q44	A-2C	R210	B-2C	R406	B-2C	C217	B-1B	L36	A-3F
Q45	A-2C	R211	B-2B	R407	B-2C	C218	B-2B	L41	A-1B
Q46	A-3C	R212	B-2B	R408	B-2C	C219	B-1C	L42	A-1A
Q51	B-2F	R213	B-1C	R409	B-2C	C220	B-2B	L43	A-1B
Q52	B-2F	R214	B-1B	R410	A-2C	C221	B-1B	L44	A-2B
Q53	B-2E	R215	B-1B	R411	A-2C	C301	A-1G	L45	A-2B
Q54	B-2F	R216	B-1B	R412	A-2B	C302	A-1F		
Q55	B-2G	R217	B-3B	R413	A-2B	C303	B-2F	QA11	B-3E
Q56	B-2G	R218	A-3B	R414	A-2B	C304	B-2F		
Q57	B-2F	R219	B-2B	R415	A-2C	C305	B-2F	TL31	B-3F
Q58	B-2F	R220	B-2B	R416	A-2C	C306	B-2F	TL32	B-2F
		R221	B-1B	R417	A-2B	C307	B-2F	TL33	B-3E
D11	B-2E	R222	B-1B	R418	A-2B	C308	A-1F	TL34	B-1F
D12	B-1A	R223	B-1B	R419	A-2B	C309	A-3F	TL35	A-3G
D13	B-2A	R224	B-1B	R420	A-2C	C310	B-2G	TL36	A-3F
D21	B-1C	R225	B-1B	R421	A-3C	C311	A-1F	TL37	B-2G
D22	A-3B	R226	B-1B			C312	A-3F	TL41	A-1A
D31	A-2F	R227	B-2A	C101	B-3D	C313	B-2F	TL42	A-2A
D32	A-2E	R228	B-1A	C102	B-3D	C314	B-3G	TL43	A-2A
D33	B-2F	R229	A-1D	C103	B-3D	C315	B-2G	TL44	A-3A
D34	A-2G	R230	A-1D	C104	B-3D	C316	B-2G		
D35	B-2G	R301	B-2F	C105	A-3D	C317	B-3G		
D36	A-2F	R302	B-2F	C106	B-3D	C318	B-3G		
D37	B-3F	R303	B-2F	C107	B-3D	C319	A-2G		
D41	A-1C	R304	B-2F	C108	B-3D	C320	A-3G		
D42	A-2C	R305	B-2F	C109	B-3D	C321	A-2F		
		R306	B-2F	C120	B-3D	C322	A-3F		
R1	A-3G	R307	B-2F	C121	B-3E	C323	B-3G		
R2	A-3A	R308	A-3F	C122	B-3E	C401	B-2C		
R101	B-3D	R309	A-3F	C123	B-3E	C402	B-2C		
R102	B-3D	R310	B-2G	C124	B-3E	C403	B-2C		
R103	B-3D	R311	B-2G	C125	A-1E	C404	B-2C		
R104	B-3D	R312	B-2F	C126	B-3E	C405	B-2C		
R105	B-3D	R313	B-2E	C127	B-3E	C407	B-1C		
R106	A-3E	R314	A-3F	C128	B-3E	C408	B-2C		
R107	A-3E	R315	A-3F	C129	B-3E	C409	A-1C		
R108	A-3E	R316	B-2F	C130	A-2D	C410	A-1B		
R109	B-3E	R317	B-2F	C131	A-2E	C411	A-1B		
R110	B-3E	R318	B-2F	C132	A-2E	C412	A-1B		
R111	B-2E	R319	B-3G	C133	A-1E	C413	A-2B		
R112	B-2E	R320	B-2G	C134	B-1D	C414	A-1A		
R113	B-2A	R321	B-3G	C135	B-1D	C415	A-1A		
R114	B-1D	R322	B-3G	C136	B-1D	C416	A-2C		
R115	B-1D	R323	B-2G	C137	B-1D	C417	A-2B		
R116	B-1D	R324	B-2G	C138	B-1D	C418	A-2B		
R117	B-2D	R325	A-3G	C139	A-1D	C419	A-2B		
R118	B-2D	R326	A-3G	C140	A-2D	C420	A-2B		
R119	B-2D	R327	A-2G	C141	B-2D	C421	A-3A		

5-21 5.12 MDA/DC SCHEMATIC DIAGRAM 1/4



MDA/DC SCHEMATIC DIAGRAM 2/4



TO [Symbol]
DV/CPU
CN105
(Page 5-18)

TO [Symbol]
MECHA
CN116
(Page 5-27)

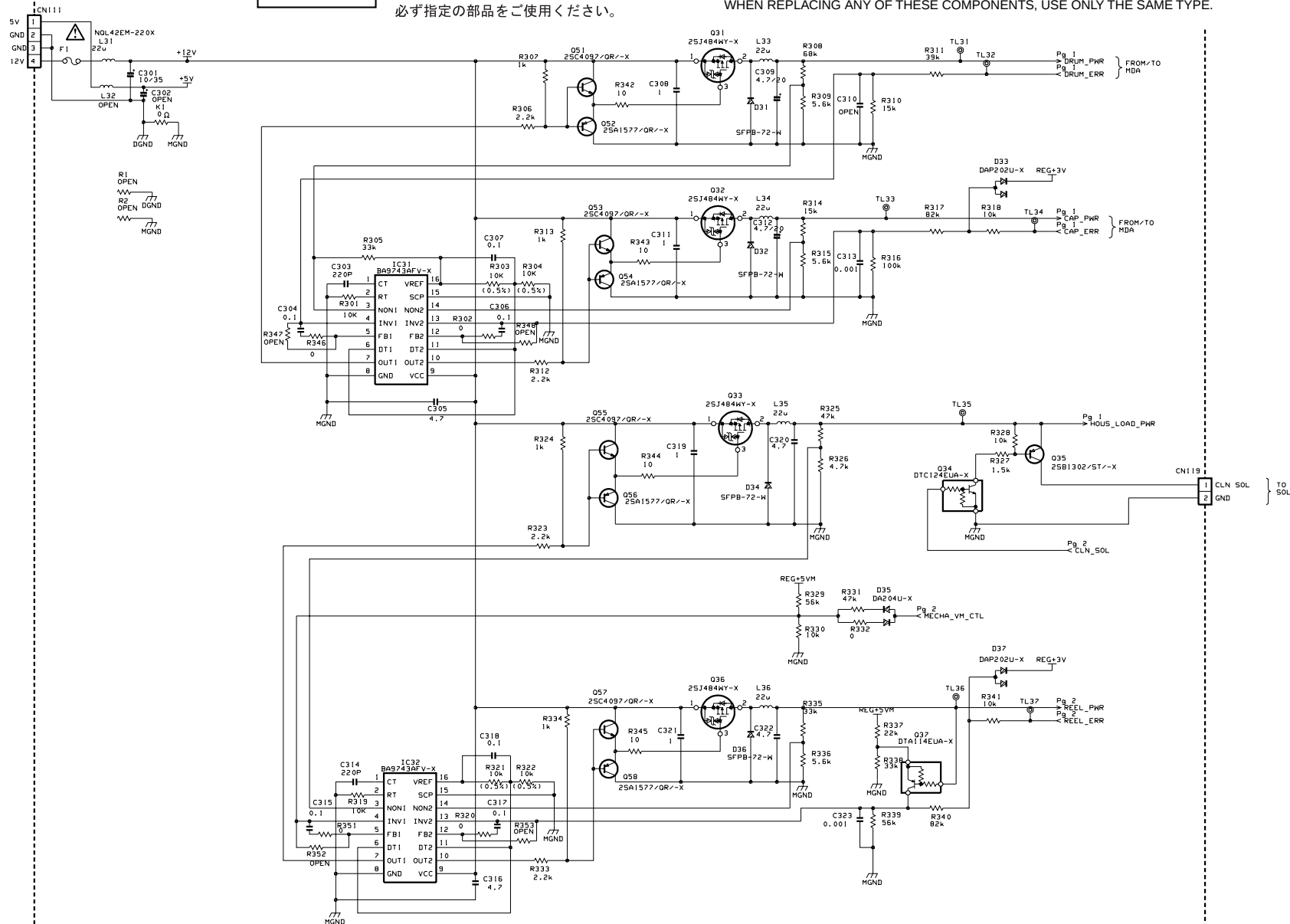
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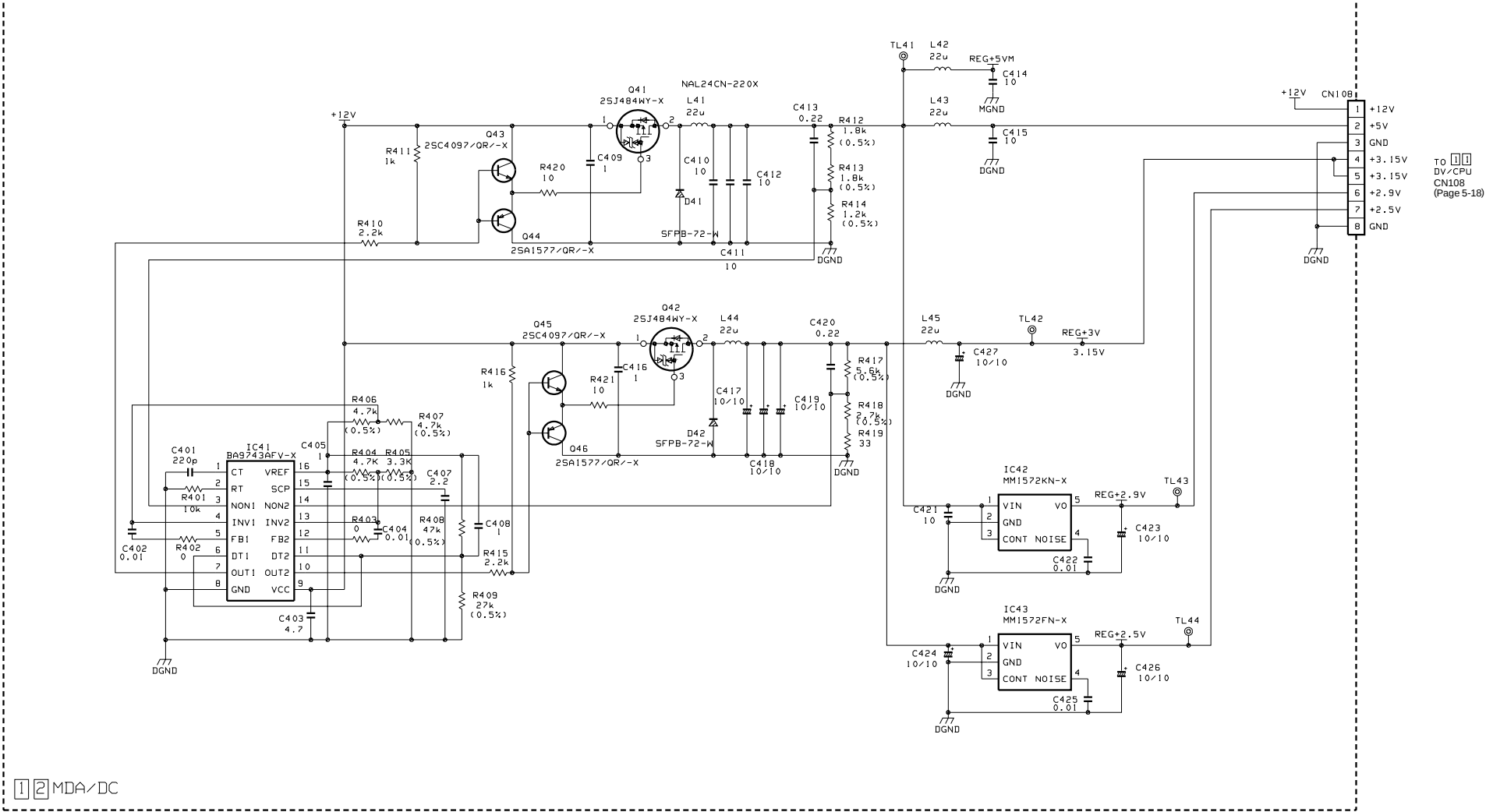
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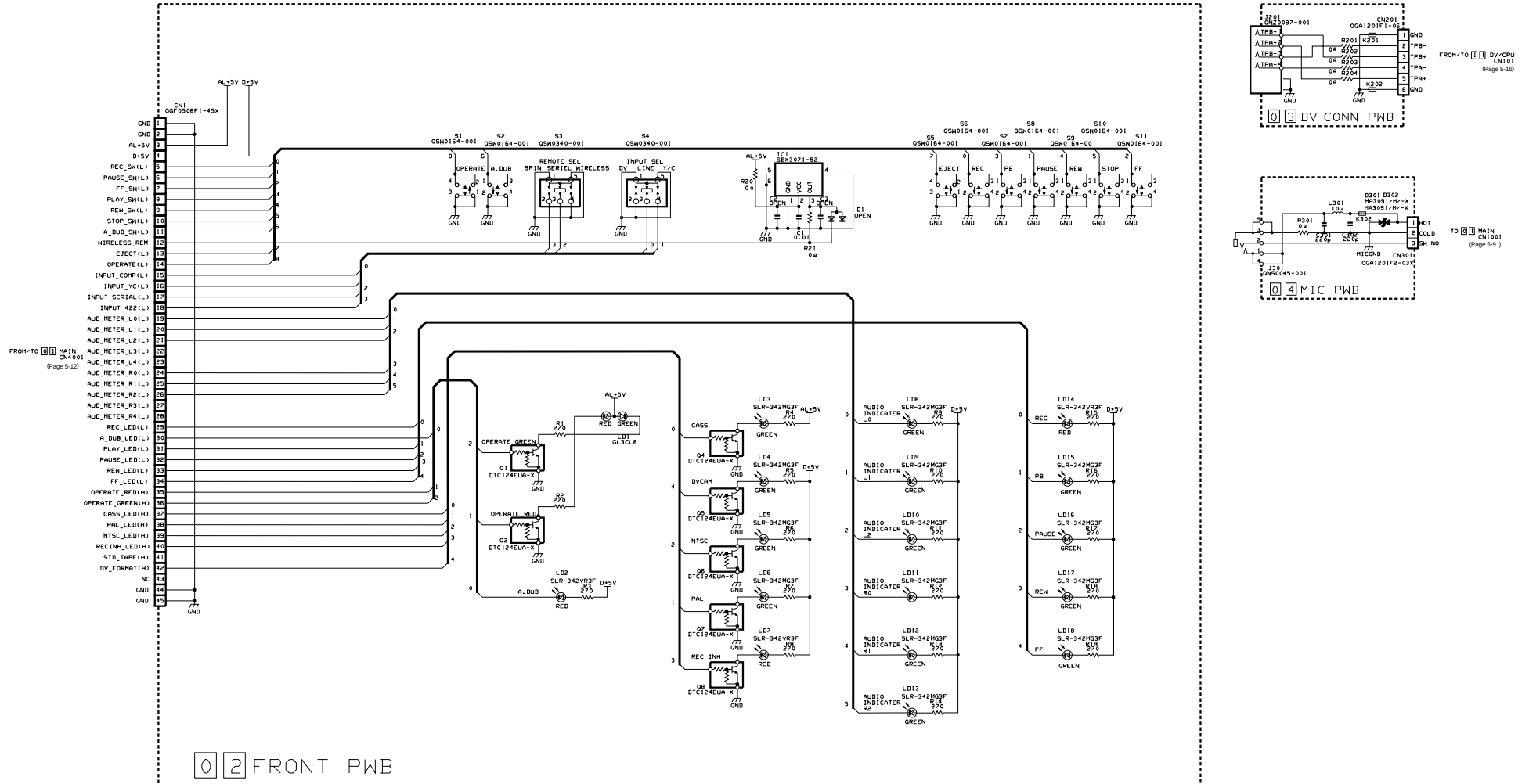
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(Page 5-11)



MDA/DC SCHEMATIC DIAGRAM 4/4

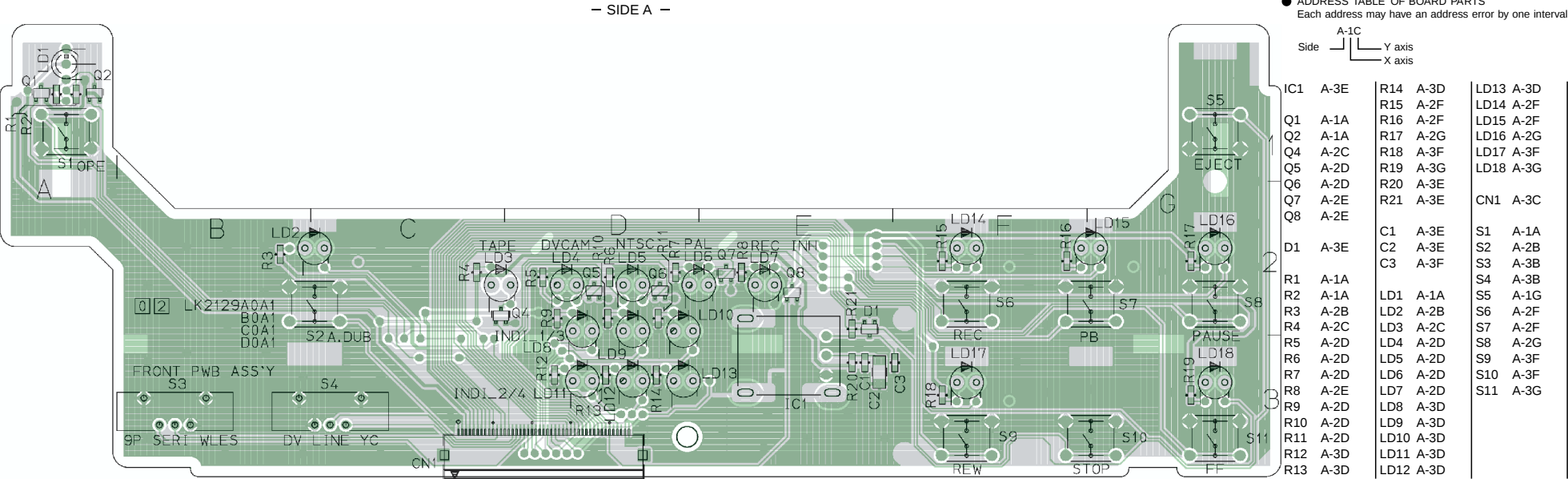


5-25 5.13 FDM (FRONT, DV CONN & MIC) SCHEMATIC DIAGRAMS



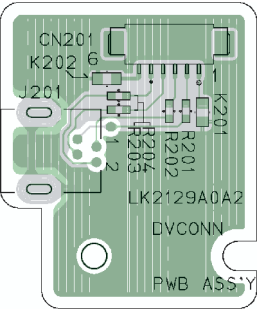
5.14 FDM (FRONT, DV CONN & MIC) CIRCUIT BOARDS

— FRONT CIRCUIT BOARD —



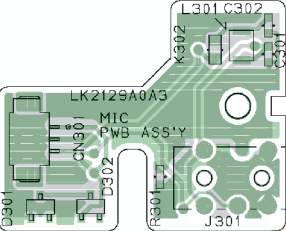
— DV CONN CIRCUIT BOARD —

— SIDE A —

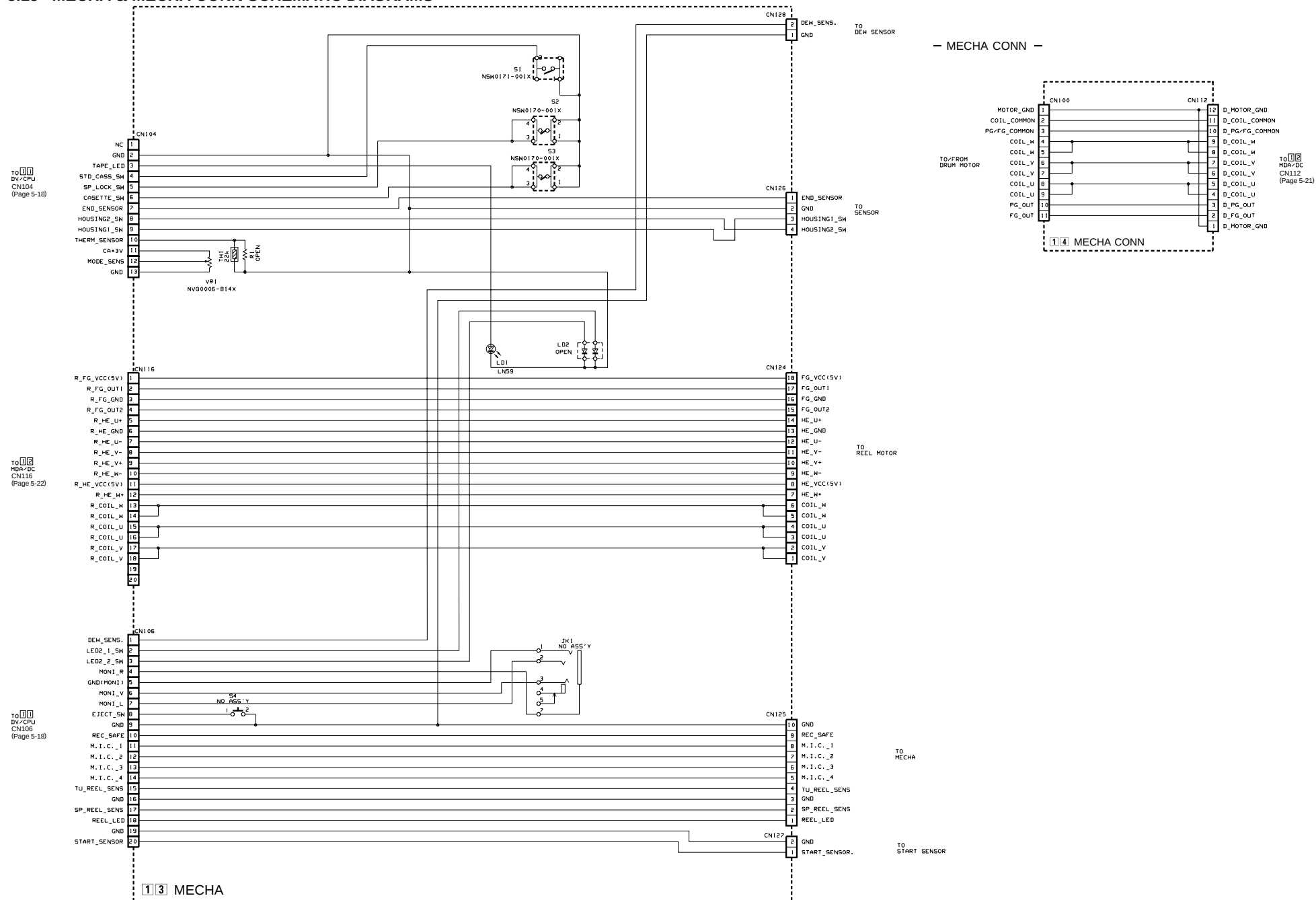


— MIC CIRCUIT BOARD —

— SIDE A —



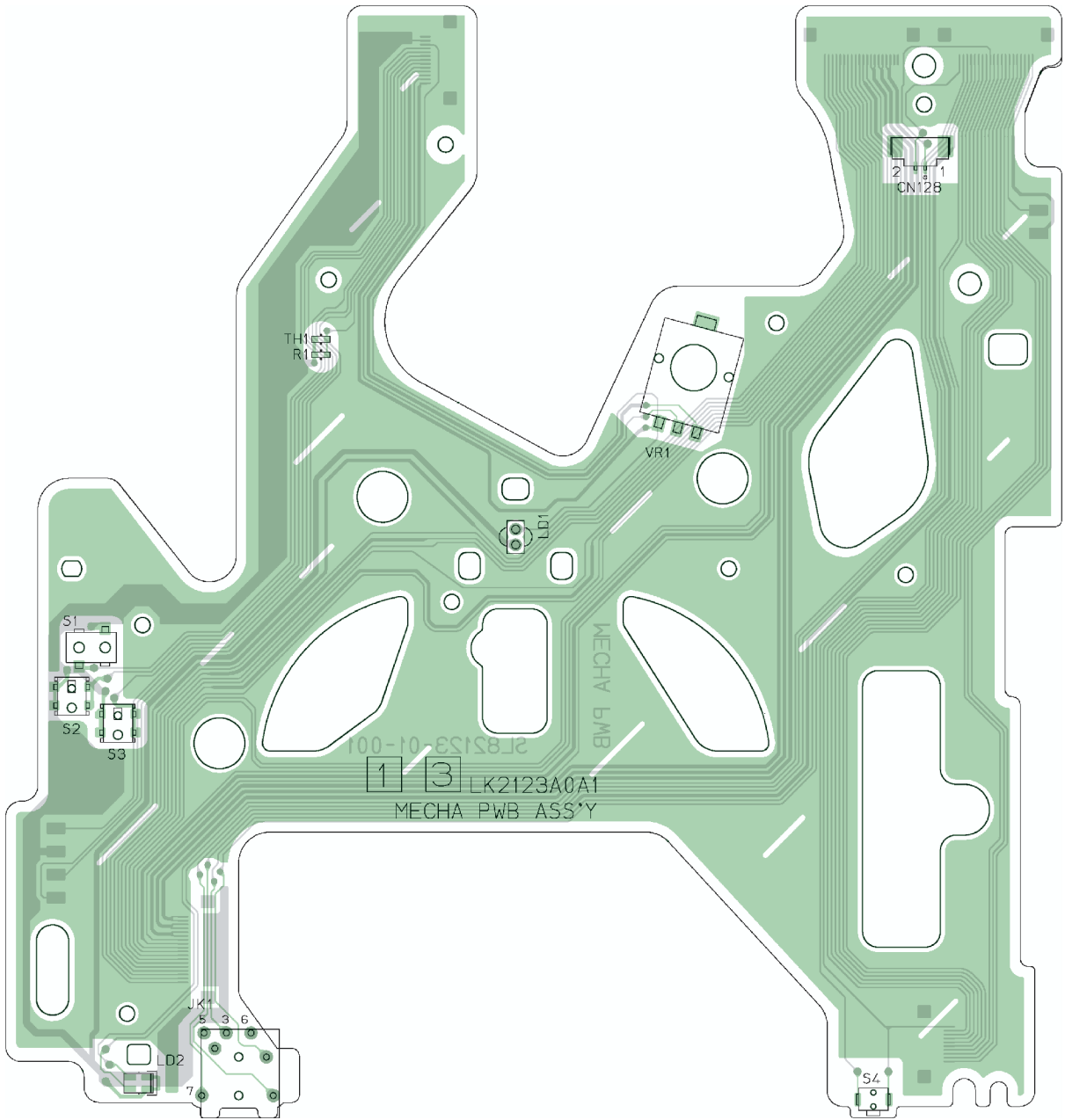
5.15 MECHA & MECHA CONN SCHEMATIC DIAGRAMS



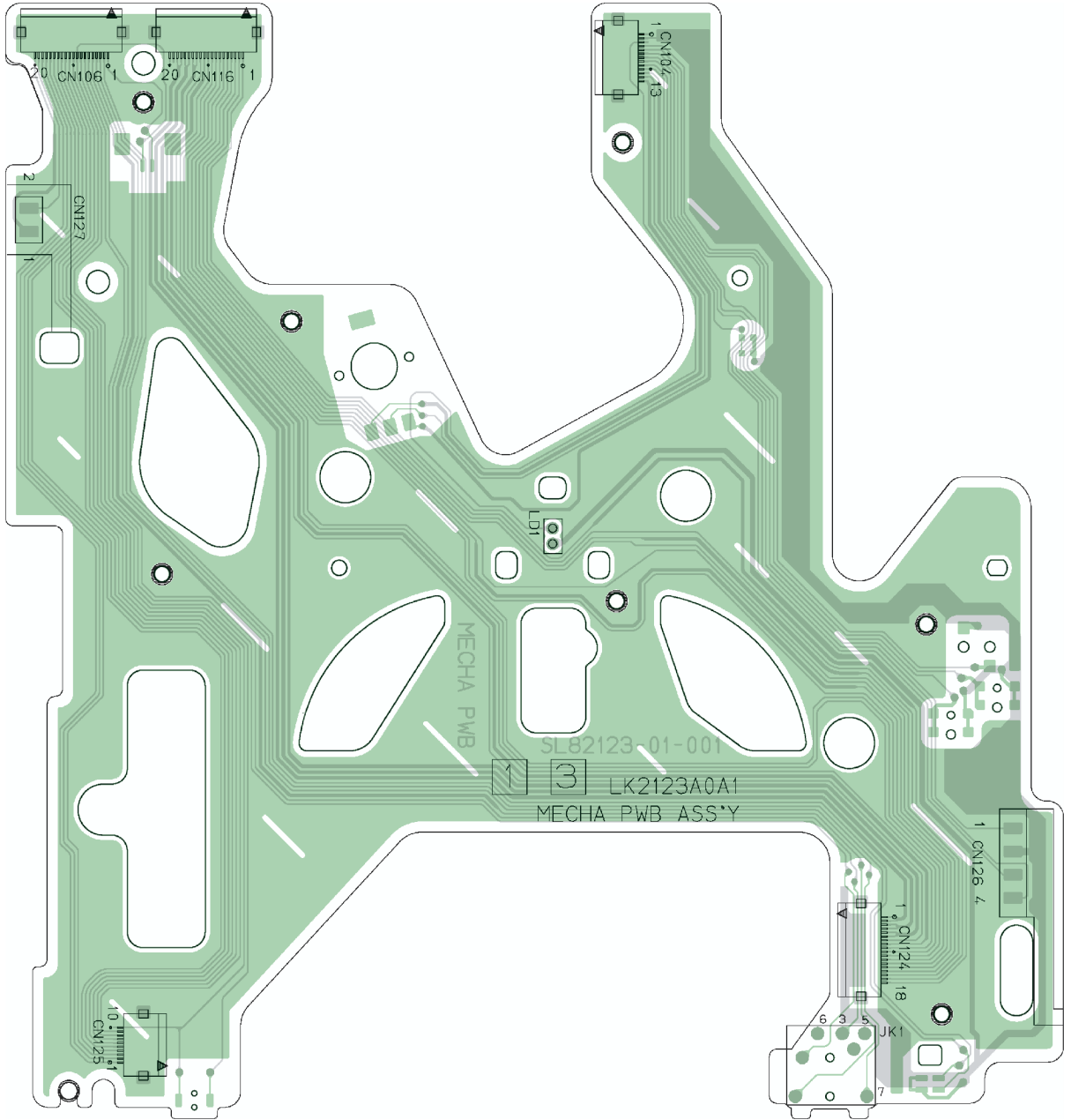
5.16 MECHA & MECHA CONN CIRCUIT BOARDS

— MECHA CIRCUIT BOARD —

— SIDE A —

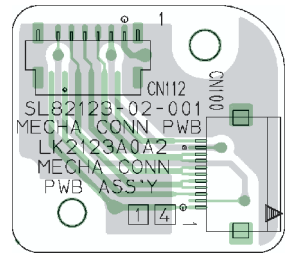


— SIDE B —



— MECHA CONN CIRCUIT BOARD —

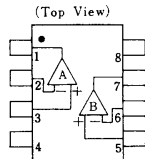
— SIDE A —



5-30

■ **AD817AR-X [ANALOG DEVICES]**
(Hi-Speed Low Power Op.Amp)

■ BA10393F-XE [ROHM]
(Dual Comparator)

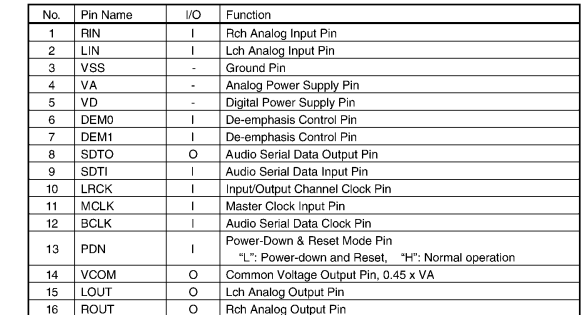
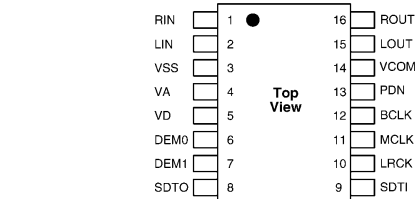


■ BA6138F-X [ROHM]
(1/2 square-law compression amplifiers)

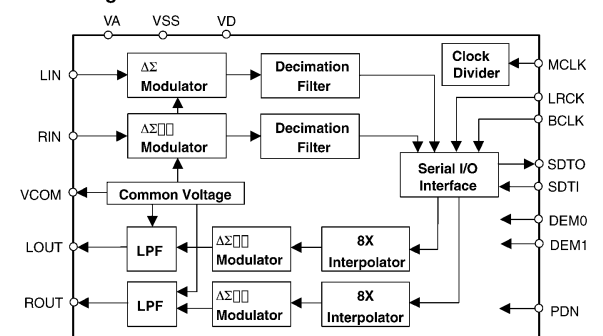
Pin

1. A OUTPUT
2. A-INPUT
3. A+INPUT
4. V^-
5. B+INPUT
6. B-INPUT
7. B OUTPUT
8. V^+

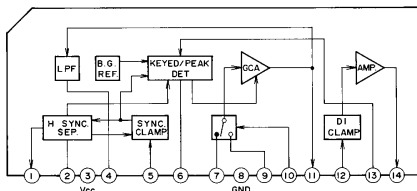
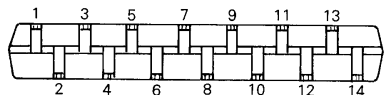
Pin/Function



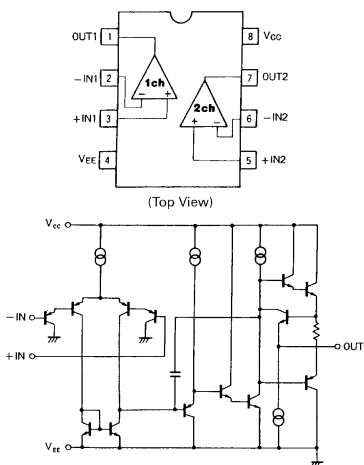
The block diagram illustrates the system architecture of the AD7792. It features two input channels, LIN and RIN, each connected to a differential input pair (VA, VSS and VD, VSS). The LIN channel includes a $\Delta\Sigma$ Modulator and a Decimation Filter. The RIN channel includes a $\Delta\Sigma$ Modulator and a Decimation Filter. A Common Voltage block provides a reference voltage to the RIN channel's $\Delta\Sigma$ Modulator. The outputs of the Decimation Filters are connected to the Serial I/O Interface. The Serial I/O Interface is also connected to a Clock Divider, which provides MCLK, LRCK, and BCLK signals. The Serial I/O Interface has SDTO and SDTI pins. The system also includes LOUT and ROUT outputs, each connected to a Low Pass Filter (LPF) and a $\Delta\Sigma$ Modulator. These modulators are connected to 8X Interpolators, which are then connected to the Serial I/O Interface. The Serial I/O Interface also has DEM0 and DEM1 pins. The system is powered by VCOM, LOUT, ROUT, and PDN pins.



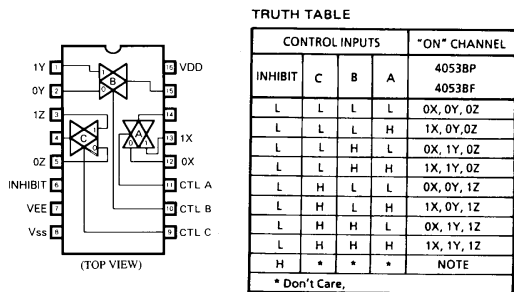
■ AN3916-/LF/ [MATSUSHITA]
(Video AGC)



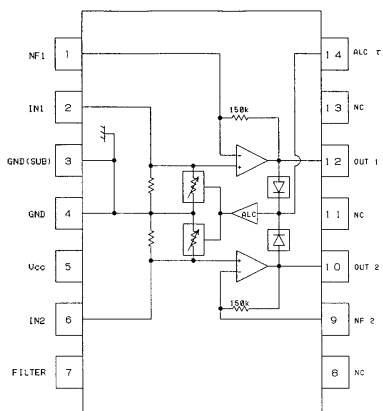
■ BA10358F-XE [ROHM]
(Dual Ground Sense Op.Amp)



■ **CD4053BPW-X [RCA]**
(Triple 2 Channel Analog Multiplexers/Demultiplexers)

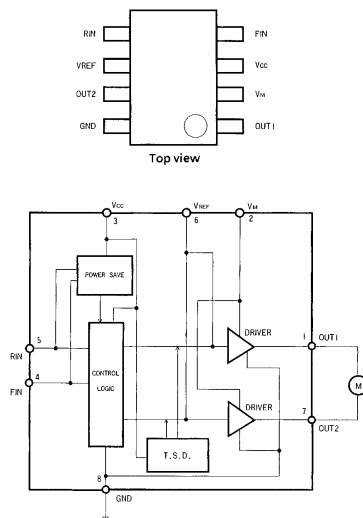


■ BA3314F-X [ROHM]
(Dual Pre-Amp. for Audio Signal)

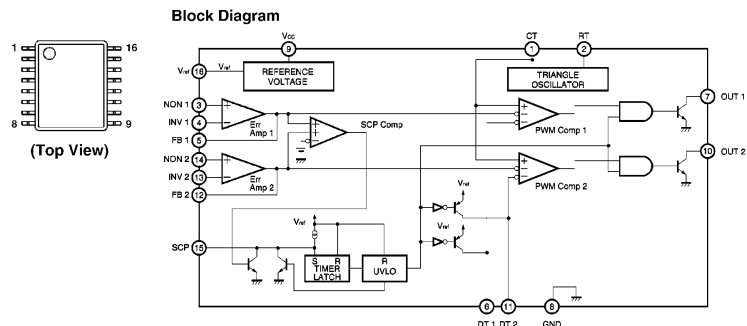


(Top View)

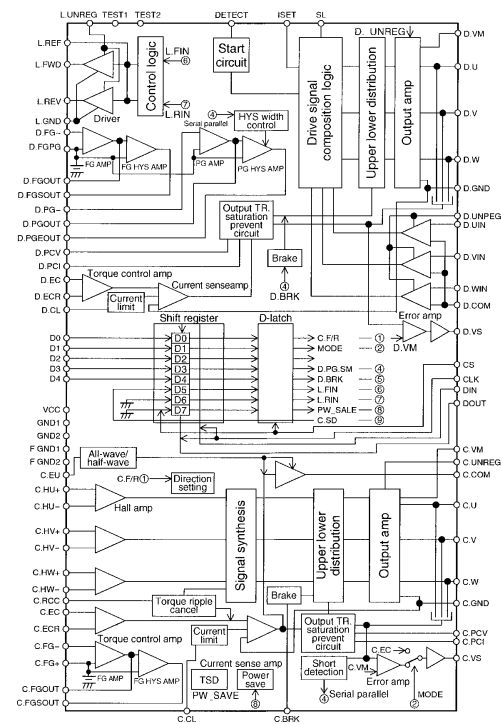
■ BA6417F-X [ROHM]
(Reversible Motor Driver)



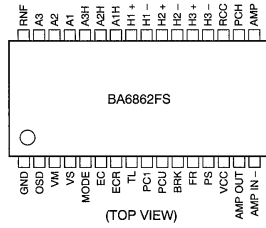
■ **BA9743AFV-X [ROHM]**
(2-channel Switching Regulator Controller)



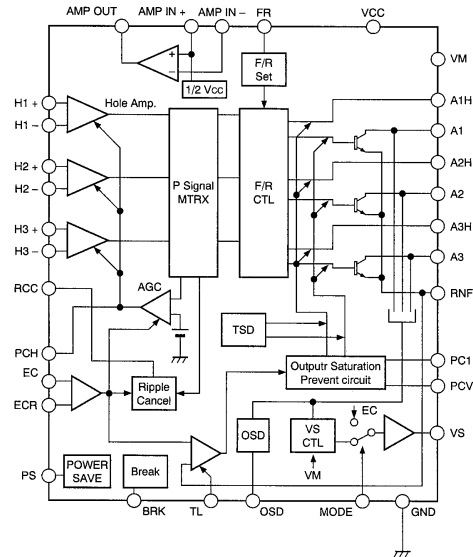
■ BA6865KV [ROHM]
(Motor Driver Controller)



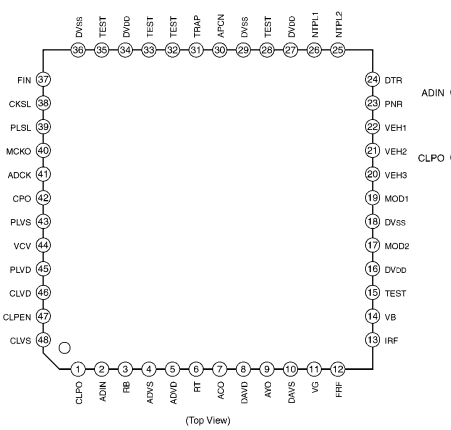
■ BA6862FS-X [ROHM]
(Motor Driver)



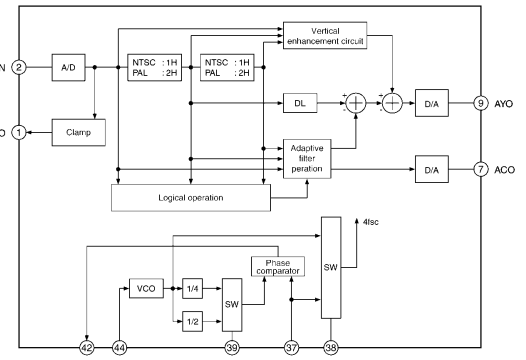
Pin No.	Symbol	Function
1	GND	GND
2	OSD	Output detect for short circuit
3	VM	Power source for motor drive
4	VS	Control for motor drive
5	MODE	Current/Voltage switching
6	ECR	Torque control
7	TL	Torque reference
8	PC1	Output saturation prevent level (low level)
9	PCV	Output saturation prevent level (high level)
10	BRK	Break input H: Break L: Movement
11	FR	Forward/Reverse CTL input
12	PS	Power save H: Stand-by L: Movement
13	VCC	
14	AMP OUT	Amplifier output
15	AMP IN -	Amplifier input (-)
16	AMP IN +	Amplifier input (+)
17	RCC	Ripple cancel
18	PCH	Hole amp, AGC phase comparator
19	H3 -	Hole signal input
20	H3 +	Hole signal input
21	H2 -	Hole signal input
22	H2 +	Hole signal input
23	H1 -	Hole signal input
24	H1 +	Hole signal input
25	A1H	Pre motor drive output
26	A2H	Pre motor drive output
27	A3H	Pre motor drive output
28	A1	Motor drive output
29	A2	Motor drive output
30	A3	Motor drive output
31	RNF	GND for motor drive
32		



■ CXD2064Q [SONY]
(DIGITAL COM FILTER (NTSC/PAL))

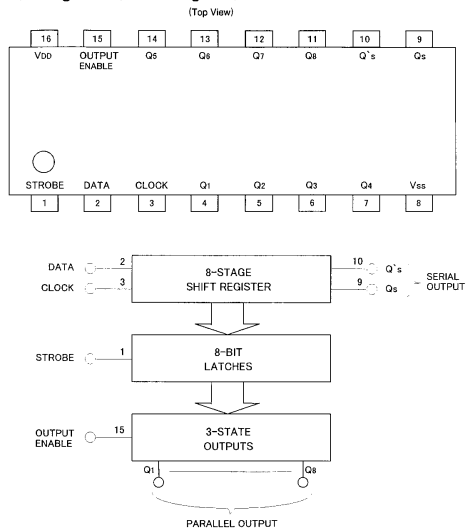


Pin No.	Symbol	I/O	Description
1	CLPO	O	Internal clamp circuit current output. Connect to ADIN when using the internal clamp. Leave this pin open when not in use.
2	ADIN	I	Comb filter analog input (A/D converter input).
3	RB	O	Reference bottom voltage for the A/D converter (0.52V typ.).
4	ADVS	—	A/D converter analog ground.
5	ADVD	—	A/D converter analog power supply. (5.0V)
6	RT	O	Reference top voltage for the A/D converter (2.60V typ.).
7	ACO	O	Analog chroma signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
8	DAVD	—	D/A converter analog power supply. (5.0V)
9	AYO	O	Analog luminance signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
10	DAVS	—	D/A converter analog ground.
11	VG	O	D/A converter related pin. Connect a capacitor of approximately 0.1μF between this pin and the analog power supply (DAVD).
12	VRF	I	Sets the full-scale value of the Y and C-channel D/A converter output signal.
13	IRF	O	Connect a resistor of "16R" (16 times the output resistor "R" of the D/A converter).
14	VB	O	D/A converter related pin. Connect to the analog ground (DAVS) via a capacitor of approximately 0.1μF.
15	TEST	I	Test pin. Normally fix to "Low".
16	DVDD	—	Digital power supply. (5.0V)
17	DVSS	—	Digital ground.
18	MOD2	I	Y/C separation mode setting. MOD2 L L Adaptive processing mode
19	MOD1	I	MOD1 H L BPF separation mode
20	VEH3	I	VEH3 H H Through mode
21	VEH2	I	Vertical enhancement setting. Can be set in 8 stages from VEH3 VEH2 VEH1: LLL (off) to HHH (max.)
22	VEH1	I	
23	PNR	I	L: NTSC/N-PAL, M-PAL, N-PAL
24	DTR	I	Normally fix to "Low".
25	NTP2	I	NTSC/PAL/M-PAL/N-PAL mode setting. NTP2 L L NTSC
26	NTP1	I	NTP1 L L PAL
27	DVDD	—	Digital power supply. (5.0V)



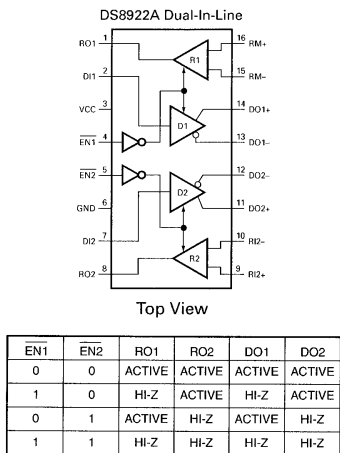
Pin No.	Symbol	I/O	Description
28	TEST	I	Test pin. Normally fix to "Low".
29	DVSS	—	Digital ground.
30	APCN	I	Horizontal aperture correction circuit setting. Low: Off, High: On.
31	TRAP	I	Trap filter setting. Low: Off, High: On.
32	TEST	I	Test pin. Normally open or fix to "Low".
33	TEST	I	Test pin. Normally open or fix to "Low".
34	DVDD	—	Digital power supply. (5.0V)
35	TEST	I	Test pin. Normally open or fix to "Low".
36	DVSS	—	Digital ground.
37	FIN	I	Clock input. Input the burst-locked fsc (2fsc) when using the internal PLL. Input the burst-locked 4fsc when not using the internal PLL.
38	CKSL	I	PLL control. Low: The internal PLL is not used. The clock (4fsc) which is input to FIN is supplied internally. High: The internal PLL is used. VCO oscillation output 4fsc clock is supplied internally.
39	PLSL	I	Selects the clock input to FIN. Low: fsc, High: 2fsc. When inputting 4fsc to FIN (when not using the internal PLL), this pin may be set to either "Low" or "High".
40	MCKO	O	Clock (4fsc) output.
41	ADCK	I	Clock input for A/D converter. Normally connect to MCKO.
42	CPO	O	PLL phase comparator output. Leave open when not using the PLL.
43	PLVS	—	PLL analog ground.
44	VCV	I	VCO control voltage input. Connect to PLVS when not using the PLL.
45	PLVD	—	PLL analog power supply. (5.0V)
46	CLVD	—	Clamp D/A converter analog power supply. (5.0V)
47	CLPEN	I	Clamp circuit enable pin. Low: Clamp on, High: Clamp off.
48	CLVS	—	Clamp D/A converter analog ground.

■ **BU4094BCFV-X [ROHM]**
(8-Stage Shift/Store Register)

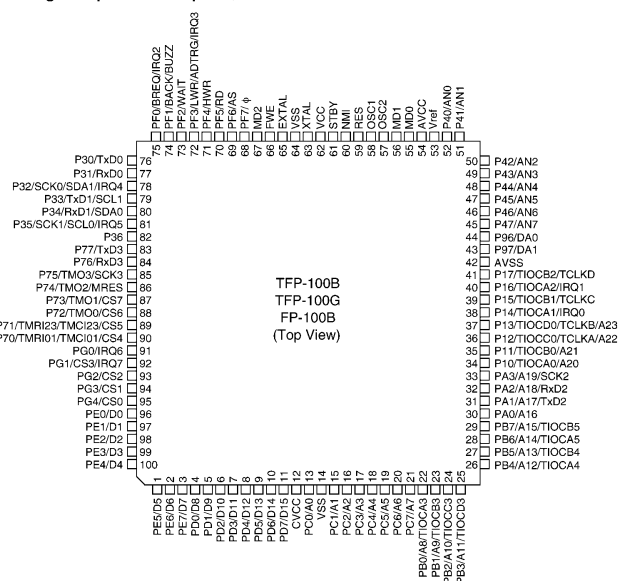


■ **DS8922M-X [NATIONAL SEMICONDUCTOR]**
(RS-422 Dual Differential Line Driver and Receiver Pairs)

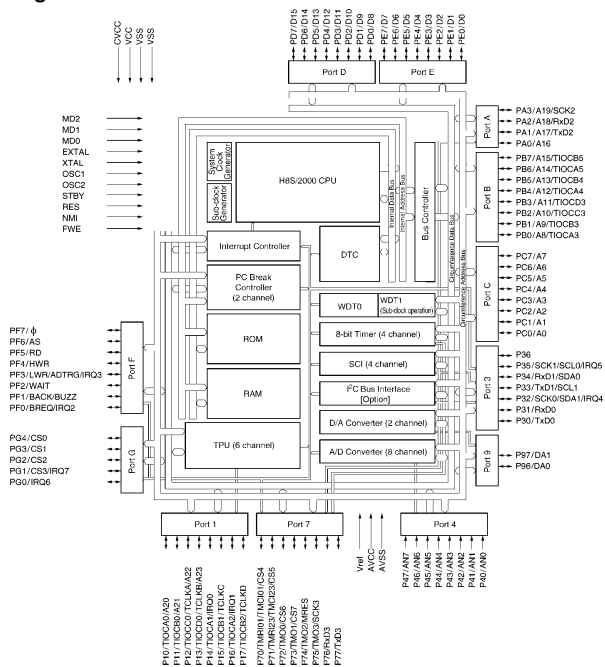
Connection Diagrams



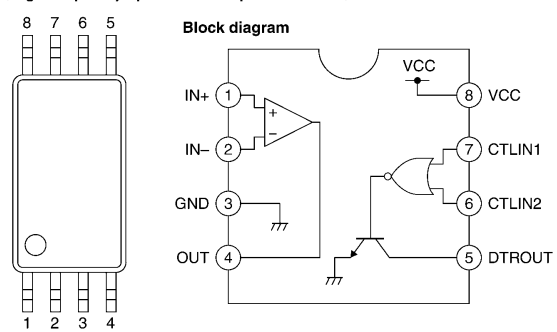
■ HD64F2238RFA13 [HITACHI]
(16-Bit Single Chip Micro Computer)



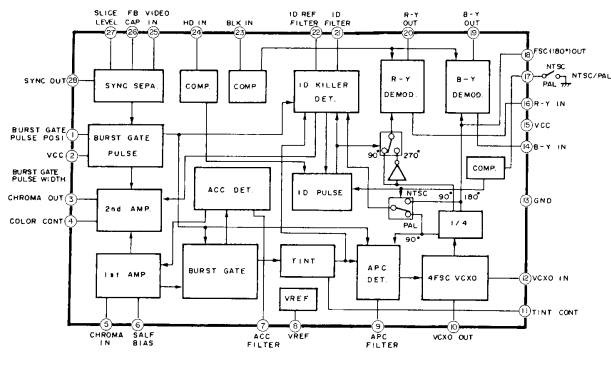
Block diagram



■ JCY0136-X [ROHM]
(High frequency operational amplifier for DVC)

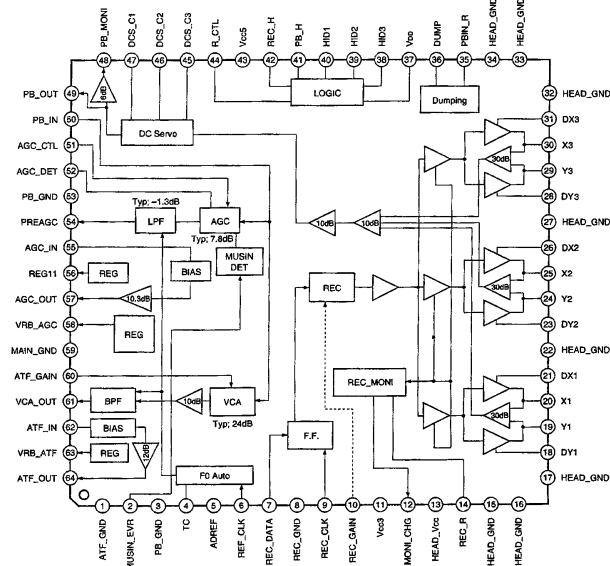


■ M51271FP-X [MITSUBISHI]
(Component Decoder)



■ JCY0132 [SONY]
(REC/PLAY amplifier for digital VCR)

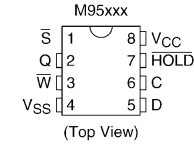
Block diagram



Pin description

Pin No.	Pin name	Description	Pin No.	Pin name	Description
1	ATF_GND	Ground terminal	36	DUMP	HEAD resonance control terminal at playback mode
2	MUSIN_EVR	EVR terminal for non-signal detection level adjustment of AGC circuit	37	VDD	VDD power supply terminal
3	PB_GND	Ground terminal	38	HID3	Mode control terminal, channel select of playback amplifier and control of recording current measurement circuit
4	TC	Time constant terminal for F0 auto PLL circuit	39	HID2	Mode control terminal, channel select of recording/playback amplifier
5	ADREF	ADREF power supply terminal ADREF	40	HID1	Mode control terminal, channel select of recording/playback amplifier
6	REF_CLK	Reference clock input terminal for F0 auto PLL	41	PB_H	Mode control terminal, ON/OFF of playback circuit
7	REC_DATA	REC DATA input terminal	42	REC_H	Mode control terminal, ON/OFF of recording circuit
8	REC_GND	Ground terminal	43	Vcc5	Vcc5 power supply terminal
9	REC_CLK	REC CLOCK input terminal	44	R_CTL	Mode control terminal, ON/OFF of recording current output
10	REC_GAIN	Adjusting terminal for recoding current	45	DCS_C3	Time constant terminal for DC servo circuit
11	Vcc3	Vcc3 power supply terminal	46	DCS_C2	Time constant terminal for DC servo circuit
12	MONI_CHG	Monitor terminal for recording current output level : REC mode, Quick charge pulse input terminal of TC terminal : PB mode	47	DCS_C1	Time constant terminal for DC servo circuit
13	HEAD_Vcc	Power supply terminal of R/P amplifier section	48	PB_MONI	PB amplifier monitor terminal
14	REC_R	External resistor connecting terminal for recording current output level monitor	49	PB_OUT	PB amplifier output terminal
15	HEAD_GND	Ground terminal	50	PB_IN	PB MAIN/ATF input terminal
16	HEAD_GND	Ground terminal	51	AGC_CTL	AGC control terminal for MAIN family
17	HEAD_GND	Ground terminal	52	AGC_DET	Time constant terminal for MAIN family
18	DY1	Damping resistor connecting terminal	53	PB_GND	Ground terminal
19	Y1	HEAD terminal	54	PREAGC	AGC+LPF output terminal for MAIN family
20	X1	HEAD terminal	55	AGC_IN	10.3dB amplifier input terminal for MAIN family
21	DX1	Damping resistor connecting terminal	56	REG11	Regulator 1.1V output terminal
22	HEAD_GND	Ground terminal	57	AGC_OUT	Output terminal for MAIN family
23	DY2	Damping resistor connecting terminal	58	VRB_AGC	Bottom reference voltage output terminal for A/D converter of MAIN family
24	Y2	HEAD terminal	59	MAIN_GND	Ground terminal
25	X2	HEAD terminal	60	ATF_GAIN	VCA control terminal for ATF family
26	DX2	Damping resistor connecting terminal	61	VCA_OUT	VCA+BPF output terminal for ATF family
27	HEAD_GND	Ground terminal	62	ATF_IN	12dB amplifier input terminal for ATF family
28	DY3	Damping resistor connecting terminal	63	VRB_ATF	Bottom reference voltage output terminal for A/D converter of ATF family
29	Y3	HEAD terminal	64	ATF_OUT	Output terminal for ATF family
30	X3	HEAD terminal			
31	DX3	Damping resistor connecting terminal			
32	HEAD_GND	Ground terminal			
33	HEAD_GND	Ground terminal			
34	HEAD_GND	Ground terminal			
35	PBIN_R	External resistor connecting terminal for playback reference current			

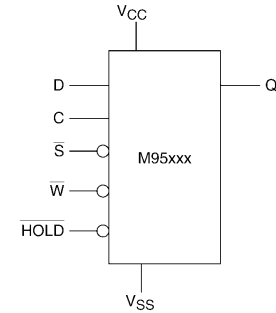
■ M95320-WMN6-X [ST MICROELECTRONICS]
(64/32 Kbit Serial SPI Bus EEPROM)



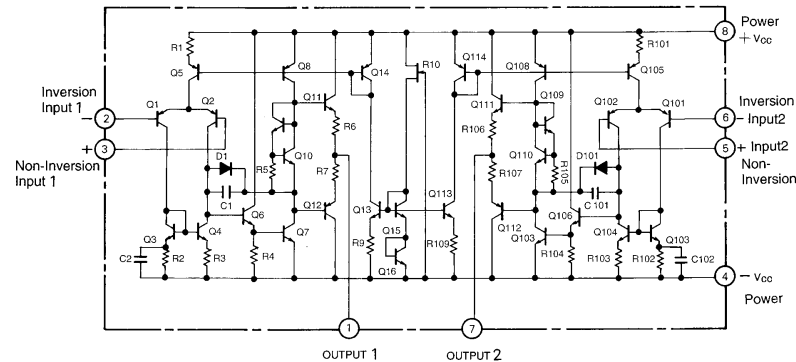
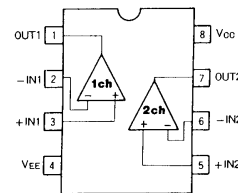
Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
S	Chip Select
W	Write Protect
HOLD	Hold
VCC	Supply Voltage
VSS	Ground

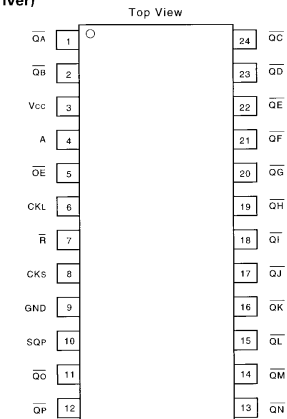
Logic Diagram



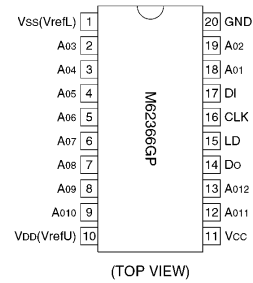
■ M5218AFP-X [MITSUBISHI]
(Dual Op.Amp.)



■ M66311FP-X [MITSUBISHI]
(LED Driver)

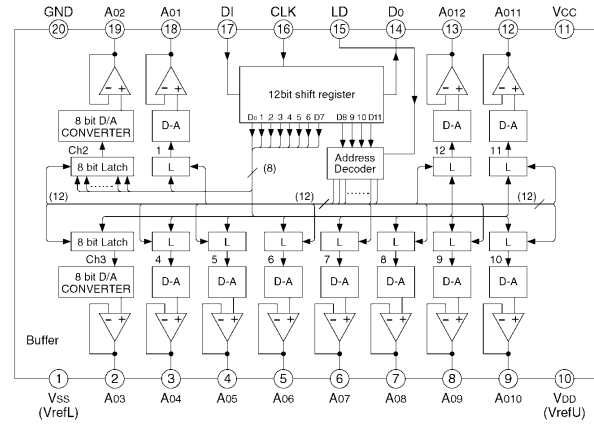


■ M62366GP-X [MITSUBISHI] (8bit 12channel D/A converter)

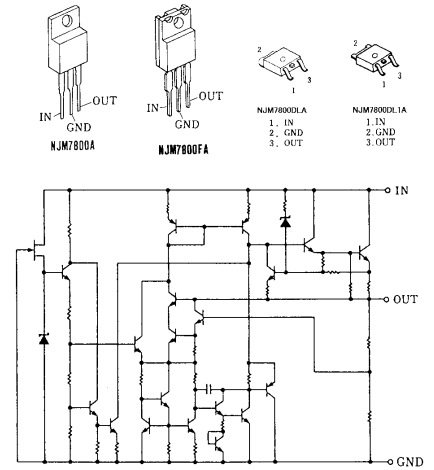


Pin No.	Symbol	Function
17	DI	Serial data input terminal to input 12-bit long serial data
14	Do	Terminal to output MSB data of 12-bit shift register
16	CLK	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
15	LD	When H-level signal is input to this terminal, the value stored in 12-bit shift register is loaded in decoder and D-A converter output register
18, 19, 20, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	A01, A02, A03, A04, A05, A06, A07, A08, A09, A010, A011, A012	8-bit D-A converter output terminal
11	VCC	Power supply terminal
20	GND	GND terminal
10	VDD	D-A converter upper reference voltage input terminal
1	VSS	D-A converter lower reference voltage input terminal

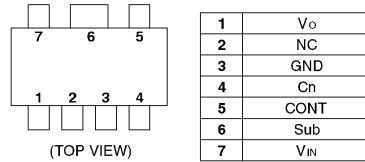
Block Diagram



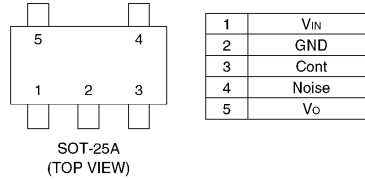
■ NJM78M05DL1A-X [JRC] (3-Terminal Positive Voltage Regulator (+5V))



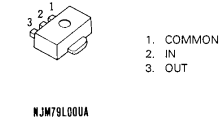
■ MM1565AF-X [MITSUMI] (500mA Regulator (5V))



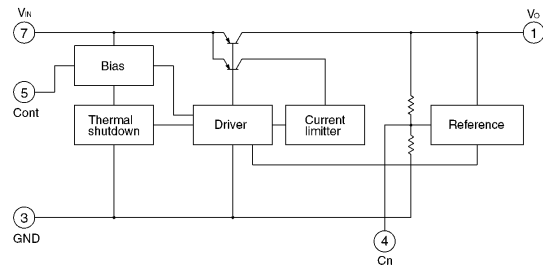
■ MM1571JN-X [MITSUMI] (1.8V Regulator)



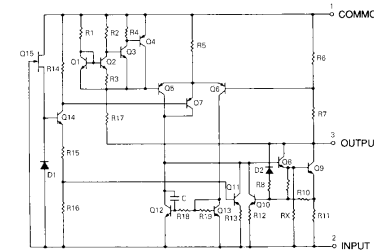
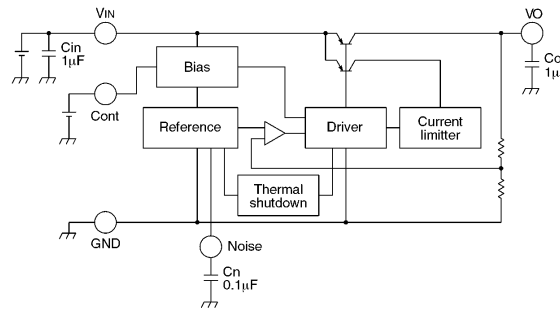
■ NJM79L05UA-X [JRC] (3-Terminal Negative Voltage Regulator (-5V))



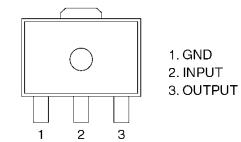
Block Diagram



Block Diagram



■ NJU722U30-X [JRC] (3-Terminal Positive Voltage Regulator)

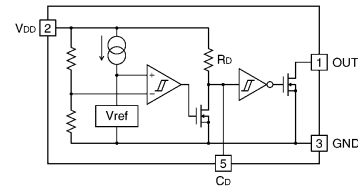


■ MM1572FN-X [MITSUMI] (Refer to MM1571JN-X.)

■ MM1572KN-X [MITSUMI] (Refer to MM1571JN-X.)

■ RN5VD26AA-X [RICOH]
(Voltage detector)

Block diagram

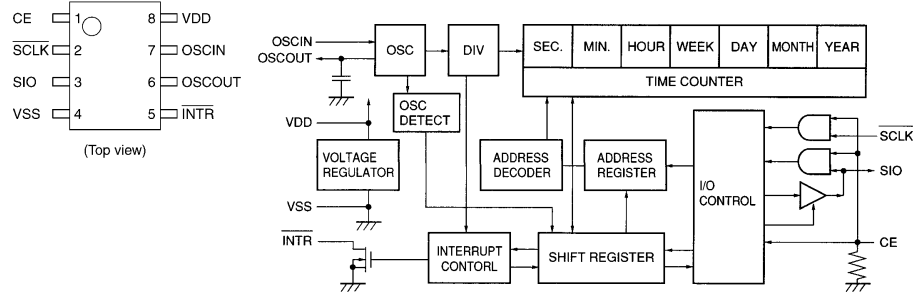


Pin descriptions

Pin Number	Pin Name	Pin Description
1	OUT	Output terminal
2	VDD	Power supply terminal
3	GND	Ground terminal
4	NC	Not connect
5	CD	External capacitor connecting terminal for delay

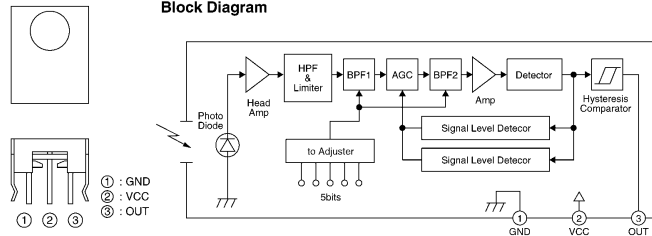
■ RS5C314-X [RICOH]
(CMOS Realtime Clock)

Block diagram

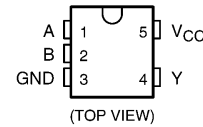


■ SBX3071-52 [SONY]
(Remote Control Receiver)

Block Diagram



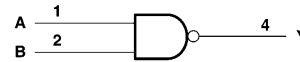
■ SN74AHC1G00K-X [TEXAS INSTRUMENTS]
(Single 2-Input Positive NAND Gate)



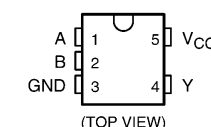
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Logic diagram (positive logic)



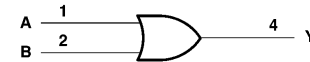
■ SN74AHC1G32K-X [TEXAS INSTRUMENTS]
(Single 2-Input Positive OR Gate)



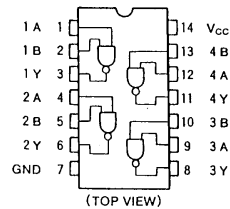
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

Logic diagram (positive logic)



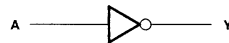
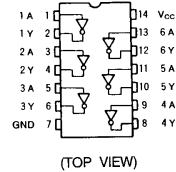
■ SN74AHC00PW-X [TEXAS INSTRUMENTS]
(Quad 2-Input NAND Gates)



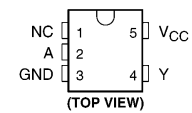
TRUE Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

■ SN74AHC04PW-X [TEXAS INSTRUMENTS]
(Hex Inverters)



■ SN74AHC1G04K-X [TEXAS INSTRUMENTS]
(Single Inverter Gate)

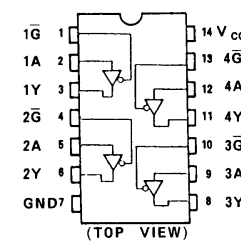


FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	L
L	H



■ SN74AHC125PW-X [TEXAS INSTRUMENTS]
(Quad Bus Buffer Gates With 3-State Outputs)

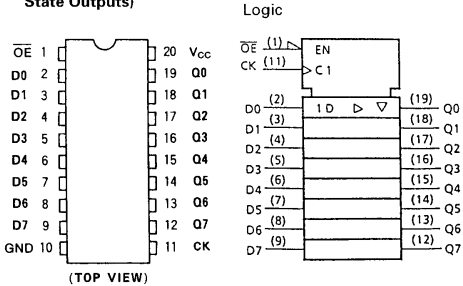


TC74HC125A TRUE Table

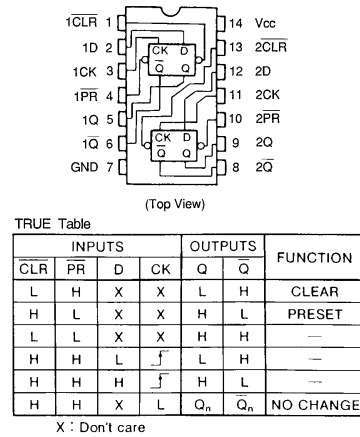
INPUTS		OUTPUTS
G	A	Y
H	X	Z
L	L	L
L	H	H

X : Don't Care
Z : High Impedance

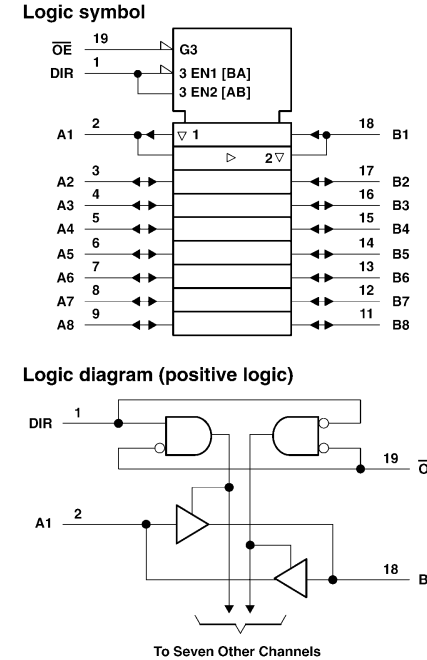
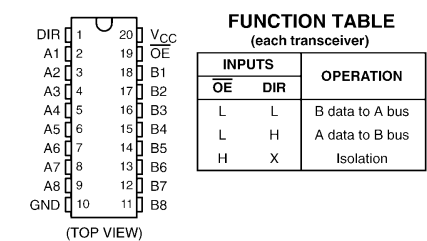
■ SN74AHC574PW-X [TEXAS INSTRUMENTS]
(Octal D-Type EDGE-Trigger Flip-Flop With NON Inverted 3-State Outputs)



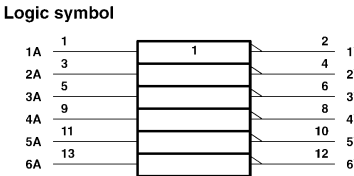
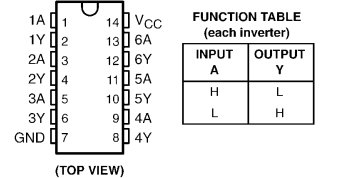
■ SN74AHC74PW-X [TEXAS INSTRUMENTS]
(Dual D-Type Flip-Flop with Preset and Clear)



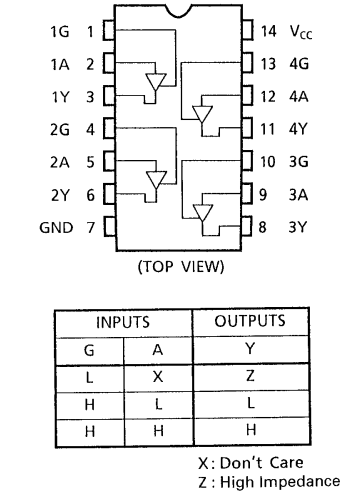
■ SN74AHC245DGV-X [TEXAS INSTRUMENTS]
(Octal Bus Transceivers with 3-State Outputs)



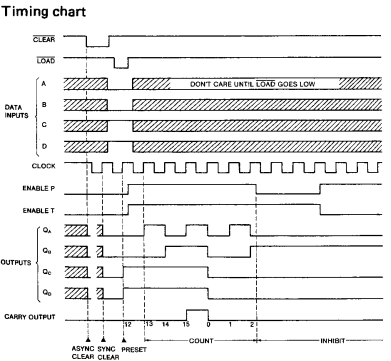
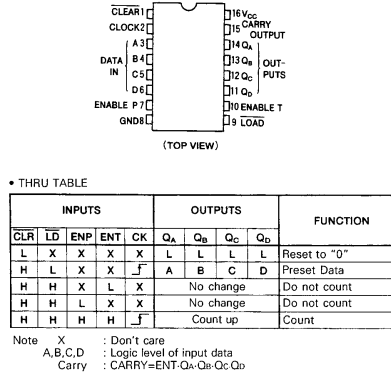
■ SN74AHC04PW-X [TEXAS INSTRUMENTS]
(Hex Inverters)



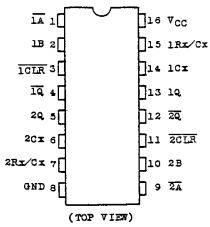
■ SN74LV126ADGV-X [TEXAS INSTRUMENTS]
(Bus Buffer Gates with 3-State Output)



■ SN74HC161APW-X [TEXAS INSTRUMENTS]
(Synchronous 4-Bit Counters Binary, Direct Clear)



TC74VHC221AFT-X [TOSHIBA]
(Dual Monostable Multivibrators (With Schmitt Trigger Input))

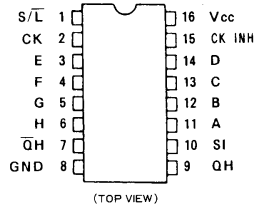


True Table

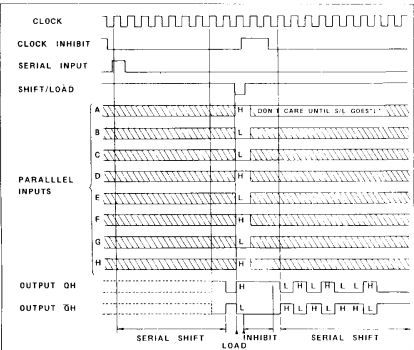
INPUTS			OUTPUTS		NOTE
A	B	CL	Q	Q	
L	H	H	L	H	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	L	H	L	H	OUTPUT ENABLE
L	H	L	L	H	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

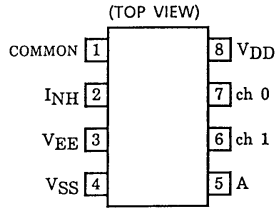
SN74LV165ADGV-X [TEXAS INSTRUMENTS]
(8-Bit Serial or Parallel-In/Serial Out Shift Registers)



Timing chart



TC4W53FU-X [TOSHIBA]
(2-Channel Multiplexer)



Truth table

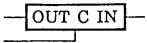
CONTROL C	IMPEDANCE BETWEEN IN-OUT *
H	$0.5 \sim 5 \times 10^4 \Omega$
L	$> 10^9 \Omega$

* Don't Care

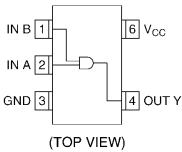
Truth table

CONTROL INPUT		ON CHANNEL
INH	A	
L	L	ch 0
L	H	ch 1
H	*	NONE

* Don't Care



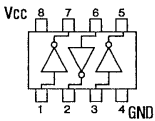
TC7SET08F-X [TOSHIBA]
(2-input AND GATE)



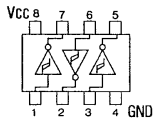
TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

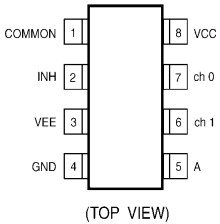
TC7W04F-X [TOSHIBA]
(Triple Inverter Gate)



TC7W14FU-X [TOSHIBA]
(Schmitt Trigger Triple Invert Gate)



TC7W53FU-X [TOSHIBA]
(2-Channel Multiplexer/Demultiplexer)

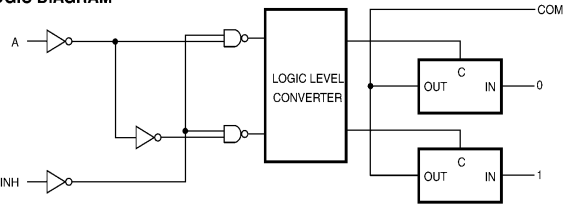


TRUTH TABLE

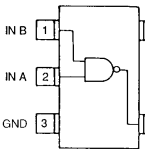
CONTROL INPUT		ON CHANNEL
INH	A	
L	L	ch 0
L	H	ch 1
H	x	NONE

x : Don't care

LOGIC DIAGRAM



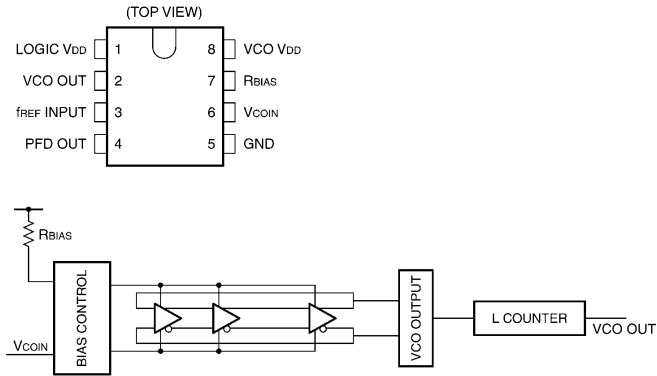
TC7SH00FU-X [TOSHIBA]
(2-Input NAND Gate)



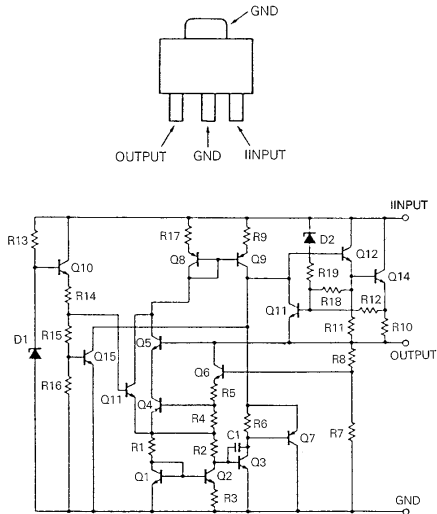
TRUE Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

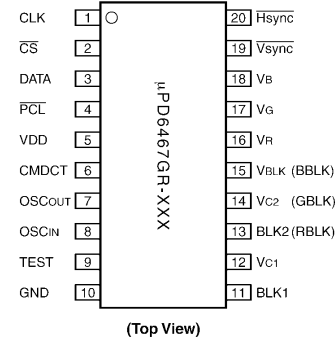
■ TLC2940IPW-X [TEXAS INSTRUMENTS]
(75MHz CMOS VCO)



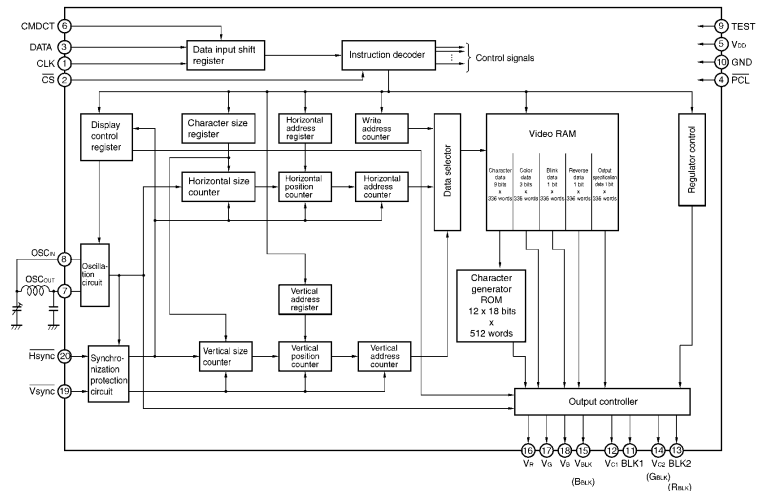
■ UPC78L05T-W [NEC]
(3-Terminal Positive Voltage Regulator (+5V))



■ UPD6467GR-519-X [NEC]
(ON-SCREEN CHARACTER DISPLAY)



BLOCK DIAGRAM



Remark Signals in () are set by using an initial status setting command (RGB + RGB compatible blanking).