System V/PRC Bus Interface

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1.1 Manual Overview

This manual provides detailed instructions for installing and operating the PESA System V to PRC Bus Interface. This manual is divided into seven sections as shown. Sections 3 and 4 contain operational and functional descriptions of the System V to PRC Bus Interface and the associated System V Bus Interface Card.

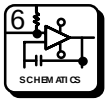
Section 1, **INTRODUCTION**, summarizes the manual, describes the product, presents a list of terms, and provides the panel specifications.

Section 2, **INSTALLATION**, provides installation and setup instructions.

Section 3, **OPERATION**, describes system operation procedures.

Section 4, **FUNCTIONAL DESCRIPTIONS**, presents an in-depth description of each component.

Section 5, **MAINTENANCE**, explains procedures for maintenance.



Section 6, **SCHEMATICS**, gives a complete package of technical documents such as schematics, and assembly drawings.

Section 7, **PARTS LIST**, provides a detailed list of system parts and components.

1.2 General

The PESA System 5 Bus Interface is designed to allow the Cougar Routing Switchers and the Jaguar Routing Switchers to be controlled by the 6600E, RC5000, or RC5500 Controllers. These controllers use the System 5 37-pin parallel bus to interface with the routing switcher system. The Cougar Frames and the Jaguar Frames use either a 9-pin "D" or a 5-pin screw-terminal connector working in conjunction with the PRC serial protocol to interface with the routing switcher system. The System 5 Bus Interface captures routing switcher commands from the System 5 bus and translates them to serial PRC commands.

2.1 Introduction

This section details the System 5 Bus Interface installation procedures. The following topics are discussed:

- Receipt Inspection
- Unpacking
- Location
- Mounting
- Cabling
- System 5 Bus Interface Card Installation
- Rear Panel Connectors
- System Connections

NOTICE

THE SYSTEM 5 BUS INTERFACE CONTAINS STATIC SENSITIVE DEVICES. CARE SHOULD BE USED WHEN IT IS NECESSARY TO HANDLE THE SYSTEM 5 BUS INTERFACE CARD. IT IS RECOMMENDED THAT A GROUND WRIST STRAP AND GROUNDING MAT BE USED BEFORE ATTEMPTING ANY EQUIPMENT INSTALLATIONS.

2.2 Receipt Inspection

The System 5 Bus Interface is tested and inspected prior to leaving the PESA factory. Upon receipt, inspect the control card and software package for shipping damage. If any damage is found, contact the carrier immediately and save all packing material.

2.3 Unpacking

System 5 Bus Interface shipments are comprised of a frame, a System 5 Bus Interface Card, and two interconnect cables. Prior to discarding packing material compare the parts received against the packing list. Carefully inspect the layers of packing material for any components which may have been overlooked during the initial unpacking.

2.4 Location

The System 5 Bus Interface may be located anywhere power is available. However, the unit should be mounted as close as possible to its associated equipment to minimize cable runs. Installation should be in an area where the ambient temperature does not exceed 40°C (104°F) inside the equipment rack.

2.5 Mounting

The System 5 Bus Interface is rack mountable in a standard 19” equipment rack. Sufficient space must be provided behind the equipment racks to allow for the control cables and power cable. All mounting holes should be utilized and mounting hardware tightened securely. As with all equipment installed in a rack, the bottom screw on each side should be installed before proceeding with the remainder of the screws. Then all screws should be securely tightened. Support the System 5 Bus Interface Frame's bottom while installing it in the rack. Figure 2-1 illustrates chassis installation in the equipment rack.

To install a System 5 Bus Interface Frame in an equipment rack follow these steps:

1. Align the frame with the slotted opening in the rack.
2. Install the bottom screws first.
3. Install the two top screws
4. Tighten all four screws securely.

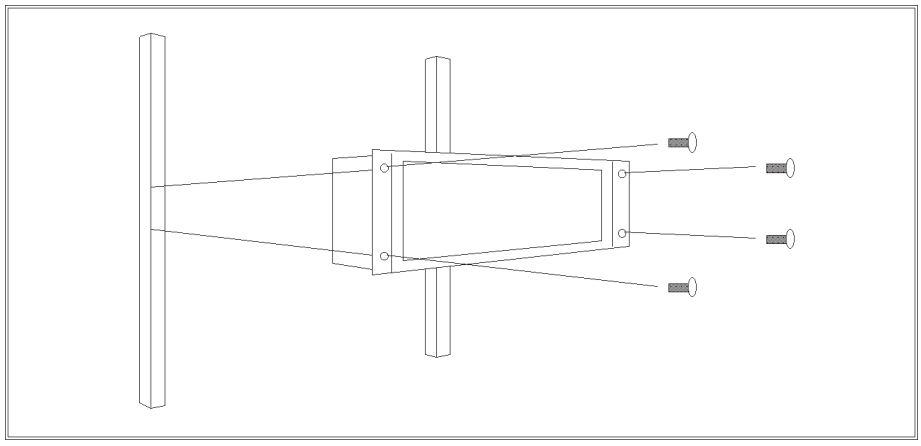


Figure 2-1 Chassis Installation

2.6 Cabling

Considerable weight will be added to the rear panel of the System 5 Bus Interface Frame by the control cables and power cable. Therefore, all cables should be strained relieved and secured to racks or other supporting structures. Failure to provide adequate cable support can result in cables separating from connectors. If cable runs are to be stored under an elevated floor, they should be tied to the racks as a guide. If cables are run along the floor, do not allow them to lay in the work area behind the racks. Stepping or tripping on the cables may result in connections being pulled free or wire breakage inside the insulation. The System 5 Bus Interface Frame should be installed in the equipment rack prior to attaching cables.

Use the following rules when cabling the System 5 Bus Interface Frame:

1. Lay all cables in their intended positions, separating control and power cables wherever possible.

2. Provide proper support for each cable during the cabling process. The use of tie-wraps is recommended, as shown below in Figure 2-2.

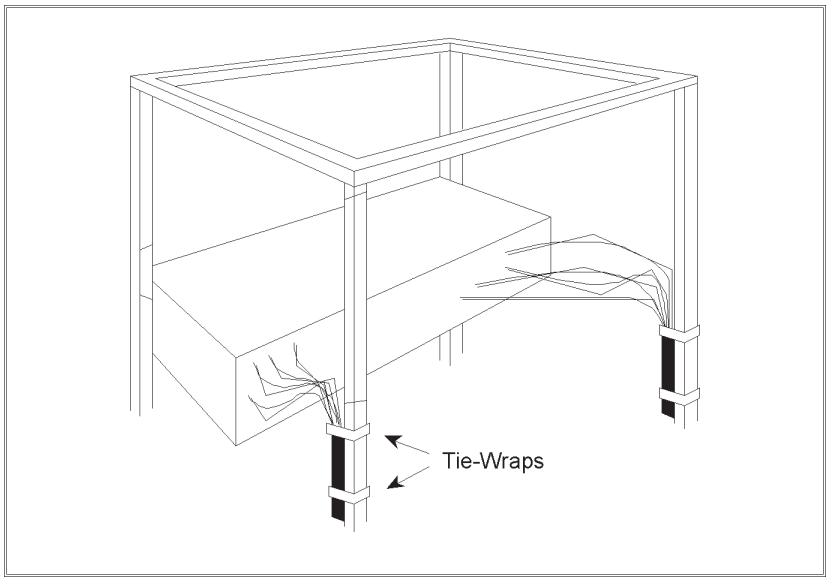


Figure 2-2 Cables Attached to Supports

2.7 System 5 Bus Interface Card Switch Settings

Prior to installing the System 5 Bus Interface Card in the System 5 Bus Interface Frame, check the switch settings on the interface card to insure proper operation. Although the interface card has several switches installed on it, only the setting of the 8-position switch labeled U7 is important. U7 contains eight individual switches, labeled 1 - 8. These switches are used to select which of the System 5 strobes the System 5 Bus Interface will act upon. Switch 1 corresponds to strobe 1, switch 2 to strobe 2, switch 3 to strobe 3, switch 4 to strobe 4, and switch 5 to strobe 5. Switches 6, 7, and 8 are unused, their position is unimportant. Placing a given switch in the ON position allows the System 5 Bus Interface to intercept and respond to System 5 commands on the strobe corresponding to the given switch position. Cougar Frames and Jaguar Frames may be mapped to the System 5 bus according to the following table:

U7 Switch Position On	Level Code for the Cougar or Jaguar Frame*
1	0 (DDDDDD)
2	1 (DDDDDU)
3	2 (DDDDUD)
4	3 (DDDDUU)
5	4 (DDDUDD)

NOTE: Level codes for the Jaguar Frames are set on the mid-plane, located inside the Jaguar Frame. Level codes for the Cougar Frames are set on the backplane, on the inside of the Cougar Frames. The level code is a binary encoded 6 bit number. D equals down, U equals up.

Each System 5 strobe is mapped to a Cougar or Jaguar level. If only one level of Cougar or Jaguar is installed in the switching system, only one position of U7 should be ON. If two levels of Cougar or Jaguar are installed in the switching system, two positions of U7 should be ON, etc.

2.8 System 5 Bus Interface Card Installation

To install the System 5 Bus Interface Card in the System 5 Bus Interface Frame take the following steps while referring to Figure 2-3:

1. Align the System 5 Bus Interface Card with the set of circuit card guides in the System 5 Bus Interface Frame.

2.8 System 5 Bus Interface Card Installation Continued:

2. Carefully push the System 5 Bus Interface Card into the System 5 Bus Interface Frame until the circuit card connectors make initial contact with backplane connectors. At this point, firmly but carefully continue pushing the interface card into the frame while making sure the connectors are properly aligned and that no connector pins are being bent. Continue pushing the interface card until it is in place and the connectors are firmly mated.

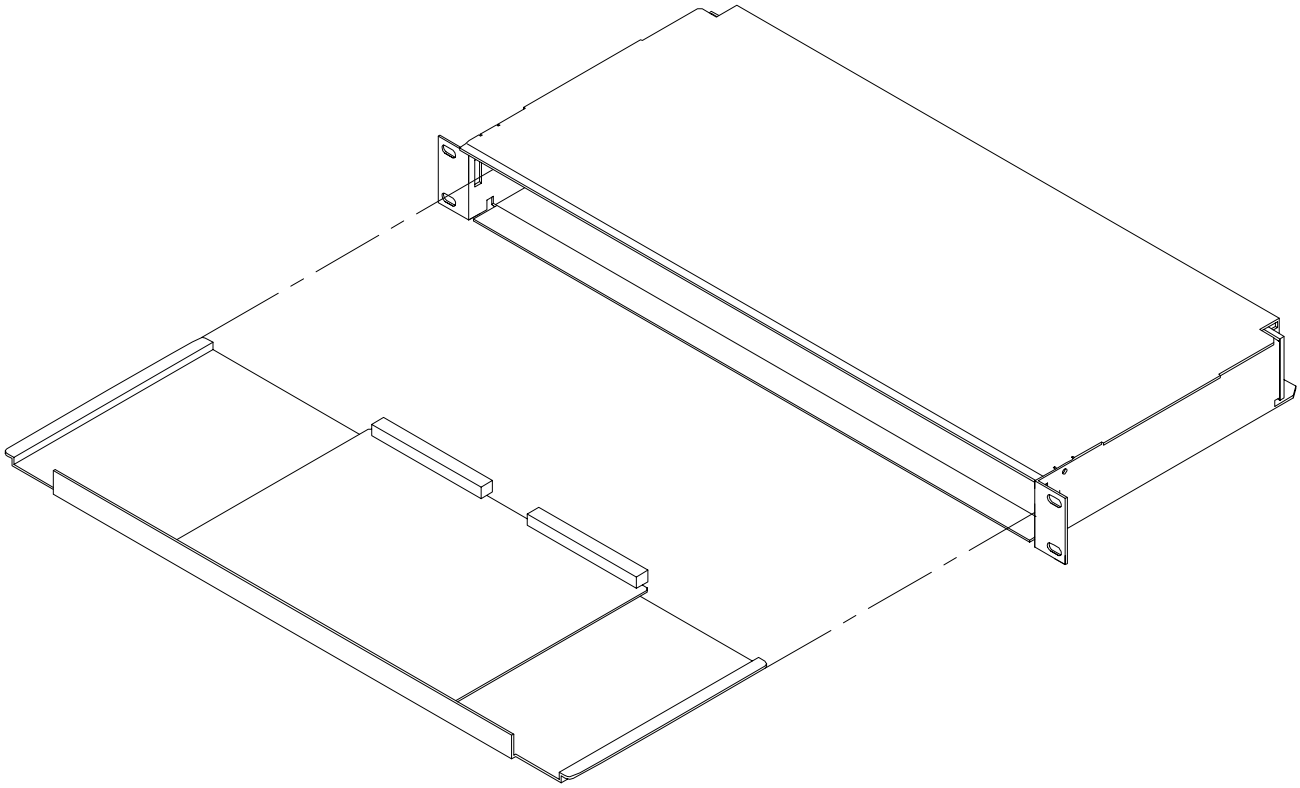


Figure 2-3 System 5 Bus Interface Card Installation

2.9 Rear Panel Connectors

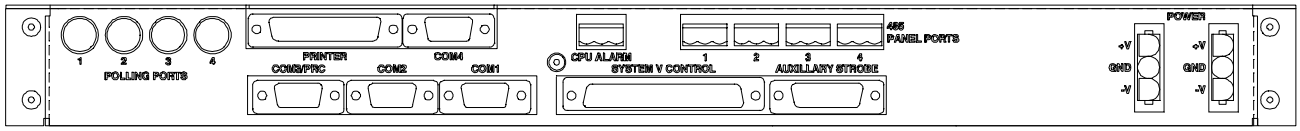


Figure 2-4 System 5 Bus Interface Frame (Rear View)

2.9 Rear Panel Connectors Continued:

System V Control Connector

System 5 Bus Interface is connected to System 5 and Lynx Series equipment items through the System V Control connector. The System V Control connector provides a port for bi-directional data exchange between System 5 components and the bus interface.

Auxiliary Strobe Connector

NOT USED AT THIS TIME

Power Loop Through Connectors

Two 3-pin power loop through connectors are located on the right-hand side of the rear of the System 5 Bus Interface Frame. Power from the external video power supply is supplied through these connectors. Power can also be looped from RM4000, RM5000, and SD5000 Video Frames or from Cougar and Jaguar Frames.

RS422 Connectors

Two RS422 I/O connectors are located on the rear of the System 5 Bus Interface for RS422 data exchange.

COM3/PRC Connector

The System 5 Bus Interface is connected to the Cougar or Jaguar Frames through the COM3/PRC connector. The COM3/PRC connector provides a port for bidirectional data exchange between the Cougar or Jaguar switching matrix and the System 5 Bus Interface. The pinout of the PRC connector is as follows:

PIN NO.	DESCRIPTION
1	GROUND
2	RX+ DATA
3	TX- DATA
4	GROUND
5	SPARE
6	GROUND
7	RX- DATA
8	TX+ DATA
9	GROUND

2.9 Rear Panel Connectors Continued:

RS422 Connectors Continued:

COM1

The COM1 connector is reserved for future PRC expansion. The pinout of the COM1 connector is as follows:

PIN NO.	DESCRIPTION
1	GROUND
2	RX+ DATA
3	TX- DATA
4	GROUND
5	SPARE
6	GROUND
7	RX- DATA
8	TX+ DATA
9	GROUND

RS232 Connectors

Two RS232 I/O connectors are located on the rear of the System 5 Bus Interface for RS232 data exchange.

COM2

The COM2 (CPU Link) connector allows serial communication between the System 5 Bus Interface and a external computer. The System 5 Bus Interface supports asynchronous, bidirectional communications, at 9600 baud. The protocol used in communications via this port is a propriety protocol developed by PESA for switcher control. The pinout for the COM2 connector is as follows:

PIN NO.	DESCRIPTION
1	CD
2	RX DATA
3	TX DATA
4	DTR
5	GROUND
6	DSR
7	RTS
8	CTS
9	N/C

2.9 Rear Panel Connectors Continued:

RS232 Connectors Continued:

COM4

NOT USED AT THIS TIME

Polling Port Connectors

There are four polling port connectors located on the rear panel of the System 5 Bus Interface. Port 1 provides connection of an external sync signal to the System 5 System Interface. The external sync input can be either a composite video signal or a video black signal. Port 2, Port 3, and Port 4 are not used at this time.

CPU Alarm Connector

NOT USED AT THIS TIME.

Printer Connector

NOT USED AT THIS TIME.

RS485 Panel Port Connectors

NOT USED AT THIS TIME.

2.9 System Connections

Once the System 5 Bus Interface is installed in the equipment rack, system connections can be made. Use the following guide and the sample connection illustrations, Figures 2-5 and 2-6, to insure that the System 5 Bus Interface system connections are properly connected and that the control and power cables are correctly installed.

Connection Guide

1. Remove power from the Cougar or Jaguar Frame before installing the System 5 Bus Interface power and control cables.

2. Install the 3-pin to 6-pin power cable (P/N 81906516530) from the Power In/Out Connector on the Cougar or Jaguar Frame to either of the two 3-pin power connectors on the right rear of the System 5 Bus Interface.

2.9 System Connections Continued:

Connection Guide Continued:

3. Install the 9-pin "D" to 9-pin "D" control cable (P/N 81902804000) between the System 5 Bus Interface's COM3/PRC Connector and the Cougar or Jaguar Frame's Control Connector.

4. Install the 37-pin ribbon cable (P/N 81906511892) between the System 5 Bus Interface's System V Control Connector and the appropriate connector on the rear of the 6600E, RC5000, or RC5500 System Controller. Refer to the controller manual for further details.

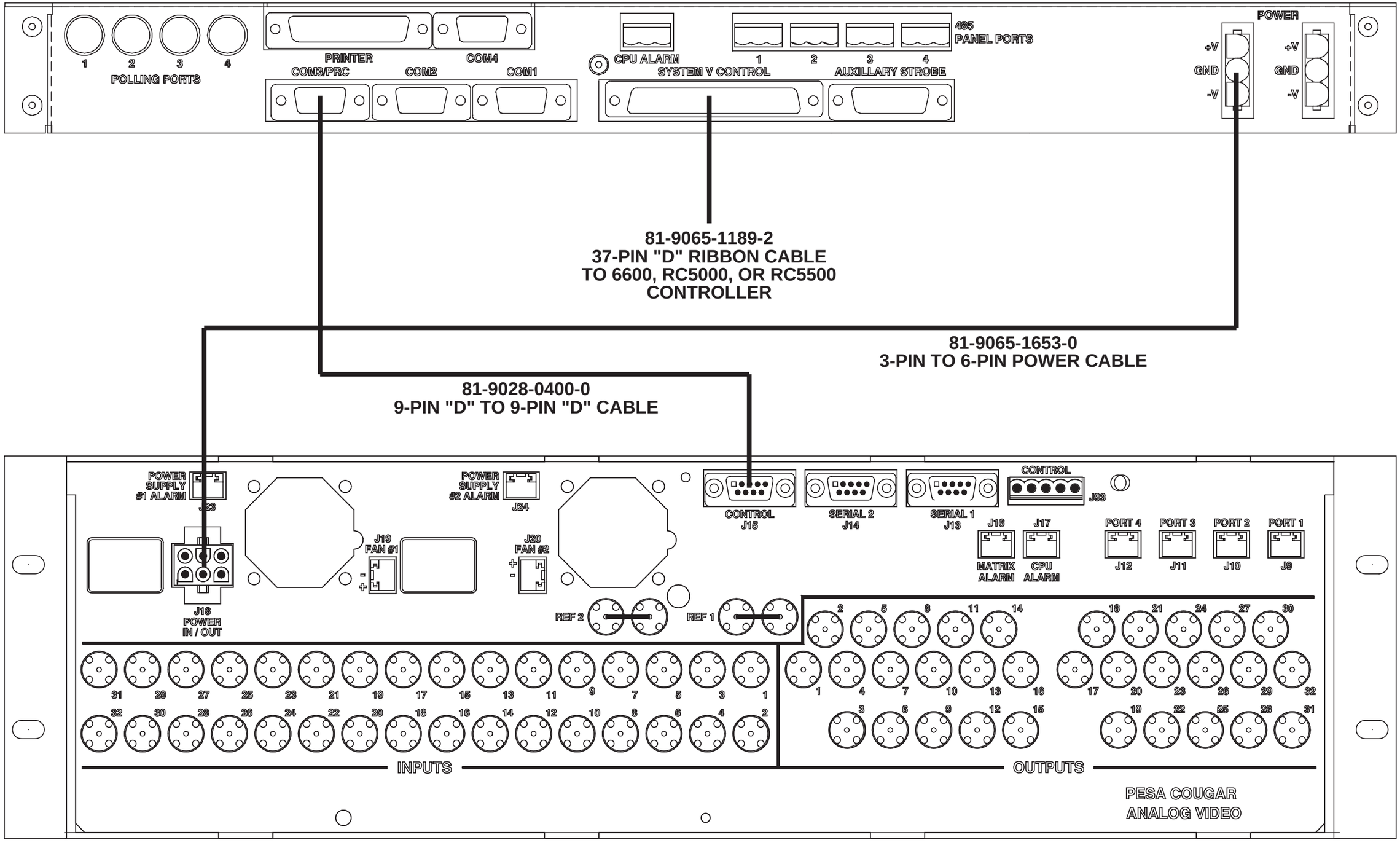


Figure 2-5 System 5 Bus Interface Connection to Cougar Video Frame

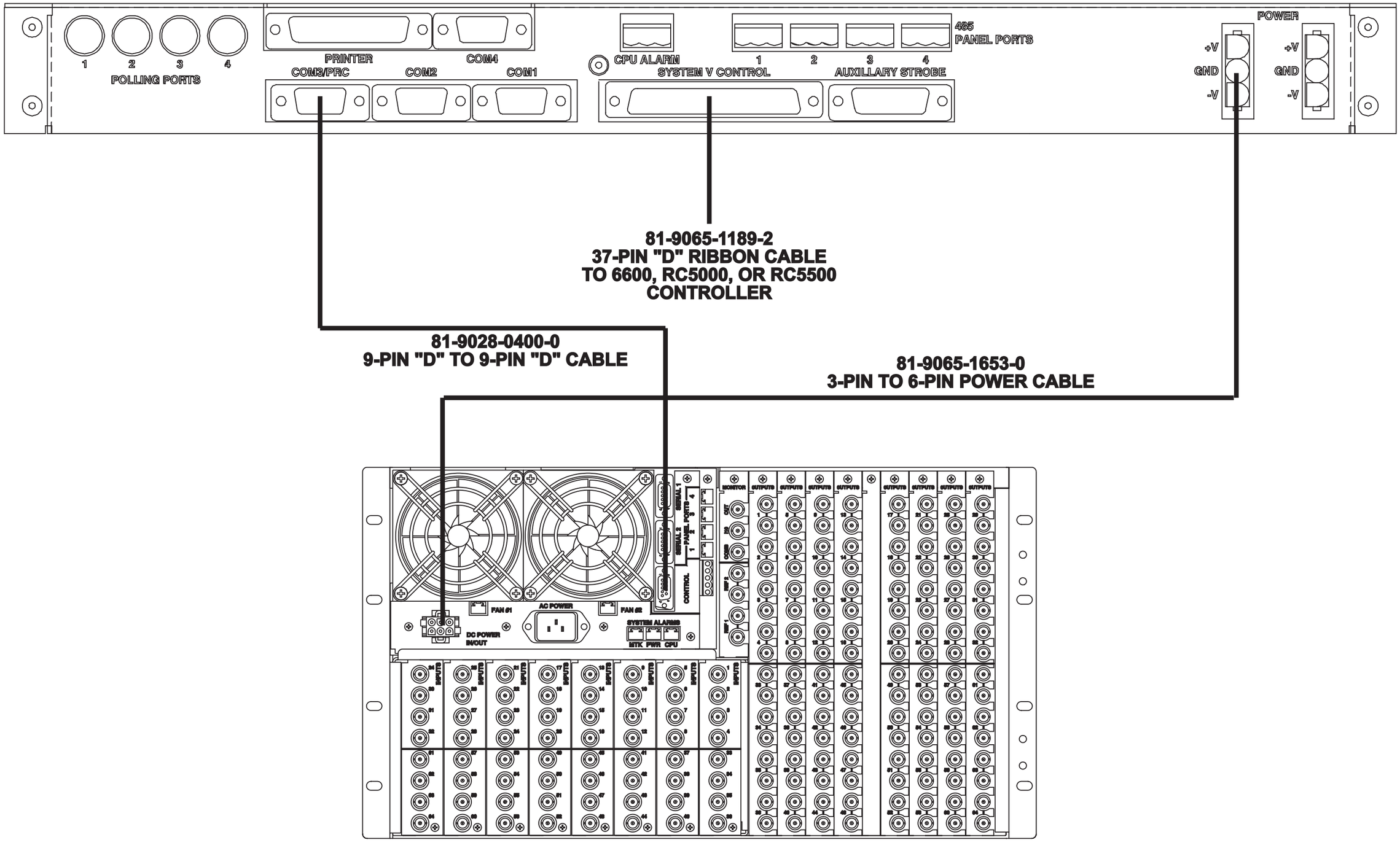


Figure 2-6 System 5 Bus Interface Connection to Jaguar Video Frame

3.1 Introduction

This section details the System 5 Bus Interface operational procedures. The following topics are discussed:

- System 5 Bus Interface Operation

3.2 System 5 Bus Interface Operation

The operation of the System 5 Bus Interface operation consists of monitoring the POWER LED for the proper indication (illuminated) and periodically testing the System 5 Bus Interface Card for proper operation by taking test switches on the Cougar or Jaguar Frames.

4.1 Introduction

The PESA System 5 Bus Interface is designed to allow the Cougar Routing Switchers and the Jaguar Routing Switchers to be controlled by the 6600E, RC5000, or RC5500 Controllers. The System 5 Bus Interface, utilizing the electronic circuits on the System 5 Bus Interface Card, captures routing switcher commands from the System 5 bus and translates them to serial PRC commands. The following manual sections describe the functions of the System 5 Bus Interface Card's electronic circuits. The following subjects are discussed:

- Power Supply
- Reset/Battery Backup
- Microprocessor
- Memory
- Serial Ports
- Sync Separator
- Configuration Switches
- System 5 Bus Capture
- Strobe Encoding/Validation
- Reading the Captured Data
- Primary Write Cycles
- Primary Read Cycles
- Confidence Reads

4.2 Power Supply

The Power Supply section consists of U1, L1, L2, D101, F1, and associated capacitors. U1 is a Switching voltage regulator that reduces the incoming +VEXT down to +5V. Fuse F1 provides over-current protection for the board. Zener D101 eliminates start-up transients generated by the regulator. Choke L1 and capacitor C1 provide filtering for the regulator input, and L2, C2, and C3 filter the regulator output. Bypass capacitors (.1 uF) are scattered about the board. LED CR1 provides a visual indication that power is applied to the board.

4.3 Reset/Battery Backup

Microprocessor supervisory circuit U36 provides the board with power-on reset, power supply monitoring, and battery backup switch-over on power failure. When power is first applied to the board, U36 ensures that the RESET line is held low for a sufficient amount of time to allow the microprocessor and other circuitry to properly initialize. The circuit also monitors the power supply voltage and holds the RESET line low when the voltage drops out of range. Capacitor C70 provides battery backup voltage for the RAM (U20, U21) when power is removed from the board. Transistor Q3 and resistors R9. R10, and R11 provide a charging circuit for the capacitor. When the proper voltage is applied to the board, U36 drives the VSTBY (Standby Voltage) from the +5V supply. When power fails or drops out of specification, U36 drives VSTBY from the battery voltage.

4.4 Microprocessor

The heart of the design is the Motorola 68332 microprocessor U37. This integrated circuit contains the CPU as well as most of the address decode circuitry and several peripheral devices. The address bus is presented on A18-A0. The data bus is presented on D15-D0. Address decode circuitry within the microprocessor generates individual chip select signals for the various memory mapped devices (CSROM, CSRAM1, CSRAM2, CSDPRAM, CSSWX, and CSSER). Various control signals are also generated by U37 (UDWE, LDWE, OE, R/W, AS, DS and others). The microprocessor derives all of its timing from a 16 MHz oscillator U25. Programmable logic device (PLD) U35 provides wait state generation and bus sizing by driving DSACK0 and DSACK1. Wait states are generated when the dual port RAM (DPRAM) U32 is being simultaneously accessed by both the microprocessor and the System 5 Bus circuitry. When simultaneous access is attempted, arbitration circuitry inside the DPRAM grants access to only one side at a time and asserts a busy signal to inform the other side that access is not granted. The signal DPBUSY is asserted when the DPRAM is in use by the System 5 Bus circuitry and the microprocessor requests access. The PLD monitors CSDPRAM and DPBUSY for this condition and generates wait states until the System 5 Bus releases control. Likewise, the signal SBUSY is asserted when the DPRAM is in use by the microprocessor and the System 5 Bus circuitry requests access. The PLD drives the SWAIT signal to force the System 5 Bus to wait until the microprocessor releases control. The PLD also monitors CSSER and SER_DTACK and generates wait states until the UART completes its bus cycles.

4.5 Memory

The board contains both read only memory (ROM) and random access memory (RAM). Two 128K x 8 devices (U23 and U24) provide 256K of ROM to contain program code. Signal CSROM provides a chip select signal that is active (low) when the microprocessor selects an address within the range of the ROM. Address bus signals A17-A1 select the specific address within each device. U24 presents data to data bus signals D15-D8, while U23 presents data to D7-D0. In a similar manner, two 128K x 8 devices (U20 and U21) provide 256K of RAM to contain program data. Signals CSRAM1 and CSRAM2 provide chip select signals that are active (low) when the microprocessor selects an address within the range of the RAM. CSRAM1 selects U21 while CSRAM2 selects U20. Address bus signals A17-A1 select the specific address within each device. U21 presents data to and receives data from data bus signals D15-D8, while U20 presents data to and receives data from D7-D0. The direction of data is specified by the state of R/W. When R/W is high, data is read from the selected RAM(s) onto the data bus. When R/W is low, data is written from the data bus into the RAM(s).

4.6 Serial Ports

The design contains three independent asynchronous serial ports. The Motorola 68681 integrated circuit (U13) is a dual universal asynchronous receiver transmitter (Dual UART). CSSER provides a chip select signal that is active (low) when the microprocessor selects an address within the range of the UART. Address bus signals A3-A0 select the specific register within the device. U13 presents data to and receives data from data bus signals D15-D8. The direction of data is specified by the state of R/W. When R/W is high, data is read from the UART onto the data bus. When R/W is low, data is written from the data bus into the UART. A bidirectional bus transceiver U14 is placed on the data bus between the microprocessor and the UART to ensure that the read/write timing specifications of the microprocessor are not violated by the UART. The UART terminates read/write cycles by asserting SER_DTACK (low). The UART may interrupt the microprocessor by asserting SERINT (low). Oscillator U11 provides a 3.6864 MHz clock from which the UART derives all its timing.

4.6 Serial Ports Continued:

Port “A” of the UART (TXA, RXA, CTSA, CDA, DSRA, RTSA, and DTRA) connect to an RS232 driver/receiver circuit U8 (MAX238). This device translates the TTL level outbound signals from the UART into RS232 specified levels for connection to external devices. Likewise, inbound RS232 level signals are translated into TTL level signals and are passed into the UART. Filters FL1-FL7 provide EMI filtering for the signals leaving the board. TXA is transmit data; RXA is receive data; CTSA, CDA, DSRA, RTSA, and DTRA are all RS232 specified handshake lines.

Port “B” of the UART (TXB, RXB, and RTSB) connect to an RS422 driver/receiver circuit U9 (MAX489). This device translates the TTL level outbound signals from the UART into RS422 specified levels for connection to external devices. Likewise, inbound RS422 level signals are translated into TTL level signals and are passed into the UART. Filters FL8-FL11 provide EMI filtering for the signals leaving the board. TXB is transmit data; RXB is receive data; RTSB is used to enable/disable the transmit driver. (Note: CTSB, CDB, DSRB, and DTRB are unused.)

Port “C” is provided by the microprocessor U37 (TXC, RXC, TXENC). These signals connect to an RS422 driver/receiver circuit U10 (MAX489). This device translates the TTL level outbound signals from the microprocessor’s UART into RS422 specified levels for connection to external devices. Likewise, inbound RS422 level signals are translated into TTL level signals and are passed into the microprocessor’s UART. Filters FL12-FL15 provide EMI filtering for the signals leaving the board. TXC is transmit data; RXC is receive data; TXENC is used to enable/disable the transmit driver.

4.7 Sync Separator

The design includes a sync separator circuit that provides a means of synchronizing the board’s operation to a video reference signal, if necessary. The video reference signal is buffered by Q2. R5 and C39 provide a low-pass filter. C38 provides AC coupling into the sync separator integrated circuit U12. R2 and C35 set the internal timing of the sync separator. The microprocessor monitors the odd/even flag from the sync separator and derives video field/frame information as necessary.

4.8 Configuration Switches

The design includes four 8 position DIP switches (labelled U39, U41, U43, and U45) that may be used to configure the board's operation. CSSWX provides a chip select signal to U33 that is active (low) when the microprocessor selects an address within the range of the switches. Address signals A3 and A4 must be low and A5 must be high to select one of the four switches. The state of Address signals A1-A0 specifies which one of the four switches is selected. When A1 and A0 are both low, U33 pin 15 is asserted (low). This enables U38 to drive the data bus D15-D8 with the switch settings of U39. When individual switches of U39 are closed, the corresponding input of U38 is connected to ground through the switch. For those switches left open, resistor pack RP10 pulls the corresponding input of U38 is pulled to +5V. These signals are placed on the data bus when U38 is selected. The remaining switches work in similar manner.

4.9 System 5 Bus Capture

The primary purpose of the board is to capture System 5 Bus activity and to translate the captured commands into a serial protocol. The individual protocols are beyond the scope of this discussion, but the System 5 Bus capture mechanism is common to all operations and will be discussed.

4.9 System 5 Bus Capture Continued:

The System 5 Bus commands consist of read and write cycles very similar to memory read/write cycles. The output address signals OAD1 - OAD256 specify the output to be affected and are analogous to the address bus of a microprocessor. The input address signals INAD1 - INAD256 specify the input to be selected and are analogous to the data bus of a microprocessor during write cycles. While both of these busses are 9 bits wide, only the lower 8 bits are supported in this design. The readback data signals RBD1 - RBD128 are used to read input status from the System 5 Bus and are analogous to the data bus of a microprocessor during read cycles. Read cycles occur when SWX_RW is high; write cycles occur when SWX_RW is low. All data transfer to/from the System 5 bus is controlled by the strobe lines STB1 - STB5. These signals are somewhat analogous to chip select signals in a microprocessor design. Each strobe typically represents individual planes of switching matrix. With an 8 bit (active) output bus and an 8 bit (active) input bus and 5 strobes, this design can handle up to a maximum of 5 levels of 256 x 256 matrices. The System 5 Bus also includes the control signals P/S, VTINH, and CONF. The state of P/S determines whether the read/write cycles are primary (i.e. router input/output switches) or secondary (i.e. auxiliary control functions). This design only deals with primary read/write cycles. These occur when P/S is high. VTINH is a vertical trigger inhibit signal used by some router controllers to temporarily delay a series of switches from occurring. This design does not use the VTINH signal. The confidence signal CONF is used to interrogate block of routing matrix to determine what portion of a matrix is populated and active. In this design, the CONF signal is generated by this board and drives the System 5 Bus during read cycles.

Each of the incoming System 5 Bus signals pass through a low-pass RC filter to help eliminate noise and to minimize signal bounce in the capture circuitry. The input address bus is buffered by U2 and is captured by U3. Likewise, the output address bus is buffered by U4 and captured by U6. The upper input and output address bits (INAD256 and OAD256) are buffered by U18 and captured by U15. The strobes and other miscellaneous control lines are buffered by U5 and captured by U16. Note that the strobes pass through DIP switch U7 after being buffered and before being captured. This switch is used to select which strobes are to be monitored by this board. By closing one or more of the switches, the corresponding strobe signal is allowed to pass through the switch to the capture circuitry. When a switch is left open, the corresponding strobe line feeding the capture circuitry is pulled inactive by resistor pack RP8.

4.10 Strobe Encoding/Validation

Since all data transfers to/from the System 5 bus are controlled by the strobe lines, it is important that the circuitry be able to detect when any strobe is valid. After the strobes have been buffered (U5) and enabled or selected by switch U7, the resulting BSTB1 - BSTB5 are processed by programmable logic device (PLD) U19. Under normal operation, only one of the strobes will be active at any given time. U19 acts as an encoder to translate the individual strobes into a binary representation of the strobe on S2, S1, and S0. When BSTB1 is asserted (low), S2 - S0 are driven to binary 000. When BSTB2 is asserted, S2 - S0 are driven to binary 010. This pattern follows for all 5 strobes. When BSTB5 is asserted, S2 - S0 are driven to binary 100. In addition to the encoding process, U19 also generates the signal STB_VALID whenever any of the five strobes are active. STB_VALID is used by a second PLD U22 to determine what type of action is being performed on the System 5 Bus. The third function of U19 is to generate a pulse on the signal LATCH_BUS whenever a valid strobe is detected. LATCH_BUS is used to latch the state of the buffered System 5 Bus into U3, U6, U15, and U16. The fourth function of U19 is to provide an interrupt signal LATCHINT to the microprocessor when data is latched. The microprocessor has control over when the interrupts are enabled, disabled, and cleared by writing appropriate values into the PLD. CSSWX provides a chip select signal that is active (low) when the microprocessor selects an address within the range of the PLD. Address signal A5 must also be low to select the PLD. This device is write only, so the data present on data bits D9 and D8 are latched when the PLD is selected.

4.11 Reading the Captured Data

As stated above, a valid strobe causes the state of the System 5 Bus to be captured into U3, U6, U15, and U16. The microprocessor is notified by the assertion of LATCHINT. Upon servicing the interrupt, the microprocessor may read the captured data. CSSWX provides a chip select signal to U33 that is active (low) when the microprocessor selects an address within the range of the capture latches. Address signals A4 must be low and A3 and A5 must be high to select one of the four capture latches (U3, U6, U15, and U16). The state of Address signals A1-A0 specifies which one of the four latches is selected. When A1 and A0 are both low, U33 pin 11 is asserted (low). This enables capture latch U3 to drive the data bus D15-D8 with the captured Input Address. The remaining capture latches may be read in similar manner.

4.12 Primary Write Cycles

As stated earlier, this design handles primary read and primary write cycles on the System 5 Bus. A primary write cycle is used to make switcher changes by selecting a new input for a given output. During a primary write cycle, the external device controlling the System 5 Bus drives the Output Address bus OAD256 - OAD1 with the output number to be changed. The Input Address bus INAD256 - INAD1 is driven with the input number to be used by the output. SWX_RW is driven low for a write cycle and P/S is driven high for primary cycles. Finally, the appropriate strobe STB5 - STB1 is driven active (low), and then inactive (high). As mentioned earlier, the strobe is detected and validated by PLD U19, and a binary representation of the strobe is generated on S2 - S0. The STB_VALID signal is asserted when any strobe is active. PLD U22 monitors the STB_VALID signal, as well as the System 5 read/write line (BSR/W) and primary/secondary (BP/S) to detect primary write cycles. When a primary write cycle is detected, U22 generates a chip select signal PCE to enable the Dual Port RAM (DPRAM) U32. The System 5 buffered Output Address BOUT8 - BOUT1 drive a portion of the DPRAM's address pins (A7 - A0). The binary encoded strobe signals S2 - S0 drive the remaining address pins (A10 - A8). The least significant buffered Output Address pin BOUT0 determines which half of the DPRAM's data bus is driven by the System 5 buffered Input Address bus. When BOUT0 and BSR/W are both low U17 asserts the PWRA signal. This enables U30 to drive the DPRAM data pins PD7 - PD0 with the System 5 buffered input address. At the same time U22 asserts SLDWE (lower data write enable). The combination of PCE and SLDWE cause the data on PD7 - PD0 to be latched into the DPRAM. Likewise, when BOUT0 is high and BSR/W is low U17 asserts the PWRB signal. This enables U31 to drive the DPRAM data pins PD15 - PD8 with the System 5 buffered input address. At the same time U22 asserts SUDWE (upper data write enable). The combination of PCE and SUDWE cause the data on PD15 - PD8 to be latched into the DPRAM.

4.13 Primary Read Cycles

A primary read cycle is used to read status from the switcher. During a primary read cycle, the external device controlling the System 5 Bus drives the Output Address bus OAD256 - OAD1 with the output number to be queried. SWX_RW is driven high for a read cycle and P/S is driven high for primary cycles. Finally, the appropriate strobe STB5 - STB1 is driven active (low), and then inactive (high). While the strobe is low the external controller samples the readback data pins of the System 5 Bus (RBD128 - RBD1) to determine what input is connected to the specified output. These pins must be driven by the circuitry on this board based on the contents of the DPRAM. As mentioned earlier, the strobe is detected and validated by PLD U19, and a binary representation of the strobe is generated on S2 - S0. The STB_VALID signal is asserted when any strobe is active. PLD U22 monitors the STB_VALID signal, as well as the System 5 read/write line (BSR/W) and primary/secondary (BP/S) to detect primary read cycles. When a primary read cycle is detected, U22 generates a chip select signal PCE to enable the Dual Port RAM (DPRAM) U32. The System 5 buffered Output Address BOUT8 - BOUT1 drive a portion of the DPRAM's address pins (A7 - A0). The binary encoded strobe signals S2 - S0 drive the remaining address pins (A10 - A8). The least significant buffered Output Address pin BOUT0 determines which half of the DPRAM's data bus is routed to the System 5 buffered readback bus. When BOUT0 is low and BSR/W is high U17 asserts the PRDA signal. This enables U28 to drive BRB7 - BRB0 with the contents of the DPRAM data pins PD7 - PD0. At the same time U22 negates SLDWE (lower data write enable). The combination of PCE asserted and SLDWE negated cause the DPRAM to present data on PD7 - PD0. U22 generates a pulse on the signal RBLATCH. This pulse causes the contents of BRB7 - BRB0 to be latched into U27. When BOUT0 and BSR/W are both high U17 asserts the PRDB signal. This enables U29 to drive BRB7 - BRB0 with the contents of the DPRAM data pins PD15 - PD8. At the same time U22 negates SUDWE (upper data write enable). The combination of PCE asserted and SUDWE negated cause the DPRAM to present data on PD15 - PD8. As before, U22 generates a pulse on the signal RBLATCH. This pulse causes the contents of BRB7 - BRB0 to be latched into U27. For the duration of primary read cycles, U22 asserts the readback enable signal RBENABLE. This signal enables U26 to drive the System 5 readback pins with the latched data from the DPRAM.

4.14 Confidence Reads

In addition to switcher status, the System 5 Bus also provides a confidence signal CONF that must be driven during primary read cycles. CONF is used to indicate the presence/absence of blocks of System 5 matrix. In this implementation, the microprocessor generates the signals CONF7 - CONF0 based on detecting or not detecting matrices on the slave switcher port. During primary read cycles, U34 uses the binary encoded strobe signals S2 - S0 to select one of CONF7 - CONF0. The selected signal drives transistor Q1, which drives the System 5 bus CONF line.

5.1 Introduction

This section will cover the maintenance, troubleshooting, and repair of the System 5 Bus Interface.

NOTICE

THIS EQUIPMENT CONTAINS STATIC SENSITIVE DEVICES. IT IS RECOMMENDED THAT A GROUNDED WRIST STRAP AND MAT BE USED WHILE MAKING REPAIRS OR ADJUSTMENTS.

5.2 General

There no adjustments on the System 5 Bus Interface Card and the need for regular maintenance is minimal.

5.3 Test Equipment

The test equipment recommended for servicing the System 5 Bus Interface is listed below. Equivalent test equipment may be used.

Digital Voltmeter
Digitizing Oscilloscope
Oscilloscope

5.4 Maintenance

The System 5 Bus Interface is designed and manufactured to give long, trouble free service with minimum maintenance requirements. If problems do occur, follow the troubleshooting procedure provided in this section. If additional technical assistance is required, refer to the General Assistance and Service information in the front of the manual. Section 6 contains component layout drawings and schematics for assistance in troubleshooting and Section 7 contains the lists of replacement parts for repairing the System 5 Bus Interface.

5.5 Corrective Maintenance

The following paragraphs provide information to assist the servicing technician in maintenance of the System 5 Bus Interface.

Factory Repair Service

If desired, equipment or boards may be returned to the factory (transportation prepaid) for repair. Refer to the General Assistance and Service information sheet in the front of this manual. Call the PESA Service Department for a RMA number before shipping an equipment item.

NOTE

PACK THE EQUIPMENT SECURELY AND LABEL WITH THE CORRECT ADDRESS. PROPER PACKAGING SAVES MONEY. THE SMALL AMOUNT OF EXTRA CARE AND TIME IT TAKES TO CUSHION A PART OR UNIT PROPERLY MAY PREVENT COSTLY DAMAGE WHILE IN TRANSIT. MAKE CERTAIN THAT THE ADDRESS IS BOTH LEGIBLE AND COMPLETE. FAILURE TO DO SO OFTEN RESULTS IN DELAY OR EVEN LOSS.

Troubleshooting

The best troubleshooting tool is a familiarity with the equipment and a through understanding of its operation. Before troubleshooting the System 5 Bus Interface review Sections 3 and 4 of this manual. Use the functional descriptions and adjustment procedures to quickly locate problems.

- If a problem is suspected with a interface card, first swap out the card and recheck the system for the problem. If the problem can be isolated to the card , and your facility is equipped for component level repair, proceed with repairs using the schematics provided in Section 6 of this manual.

NOTE

BEFORE PROCEEDING WITH COMPONENT LEVEL REPAIR MAKE SURE THE EQUIPMENT IS OUT OF WARRANTY. REPAIRING EQUIPMENT COVERED BY A WARRANTY WILL VOID THE WARRANTY.

5.5 Corrective Maintenance Continued:

System Checks

Prior to troubleshooting the System 5 Bus Interface the following basic system checks should be performed.

1. Verify the AC circuit condition. Ensure the unit is receiving the correct voltage from the main AC power source.

2. Check all line fuses and power cords.

3. Ensure that all circuit cards are firmly seated

4. Ensure all interconnecting cables and connectors are plugged in or firmly seated.

5. If applicable, ensure main power switch is turned on.

Replacement Parts

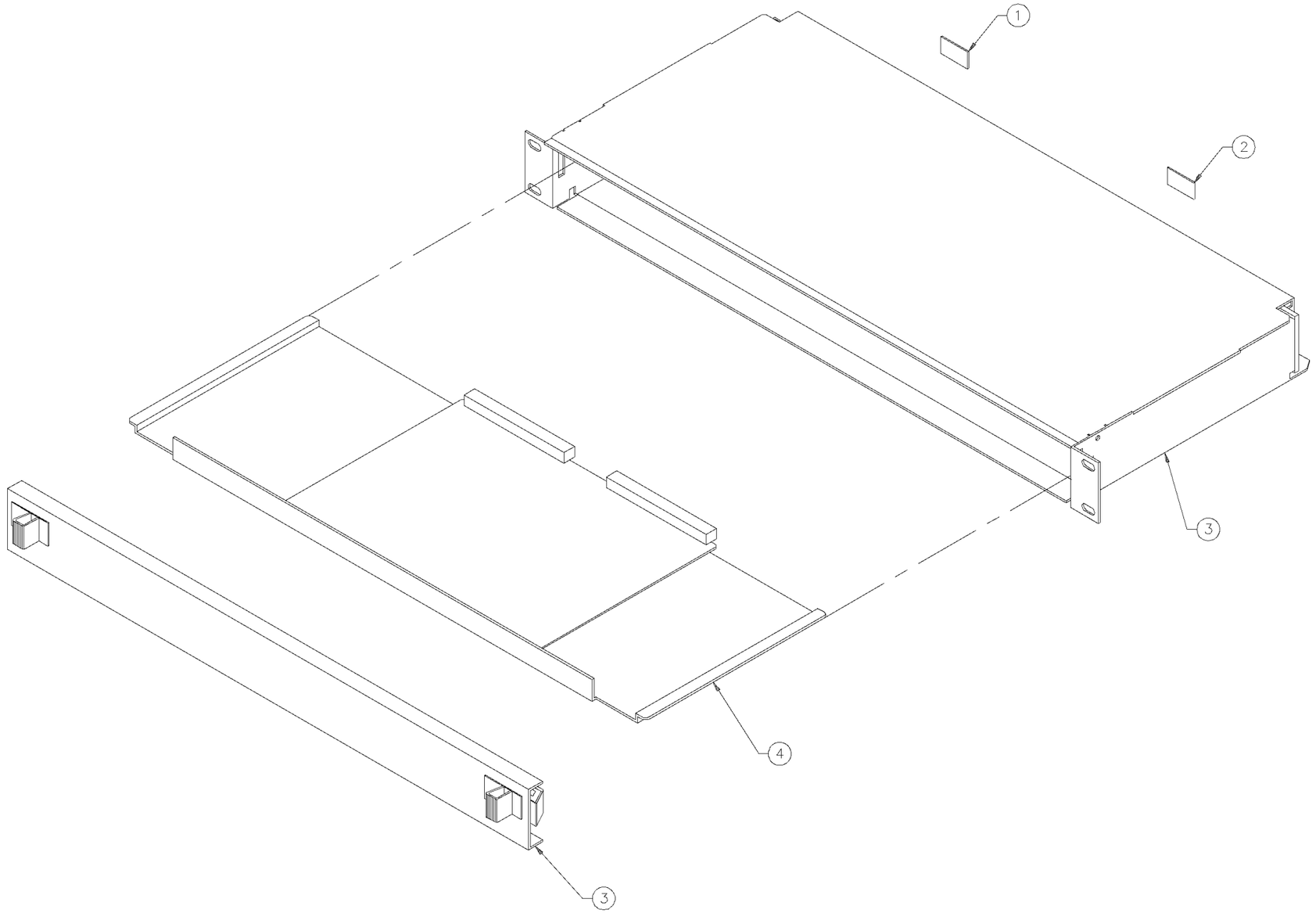
Only parts of the highest quality have been used in the design and manufacture of the System 5 Bus Interface. If the inherent stability and reliability are to be maintained, replacement parts must be of the same quality. A replacement parts list is provided in Section 7 of this manual. When replacing parts, avoid using excessive solder on the printed circuit card. Always make sure that the solder does not short two circuits together. Be sure the replacement part is identical to the original, and is placed in exactly the same position with same lead lengths (if applicable).

6.1 Schematics

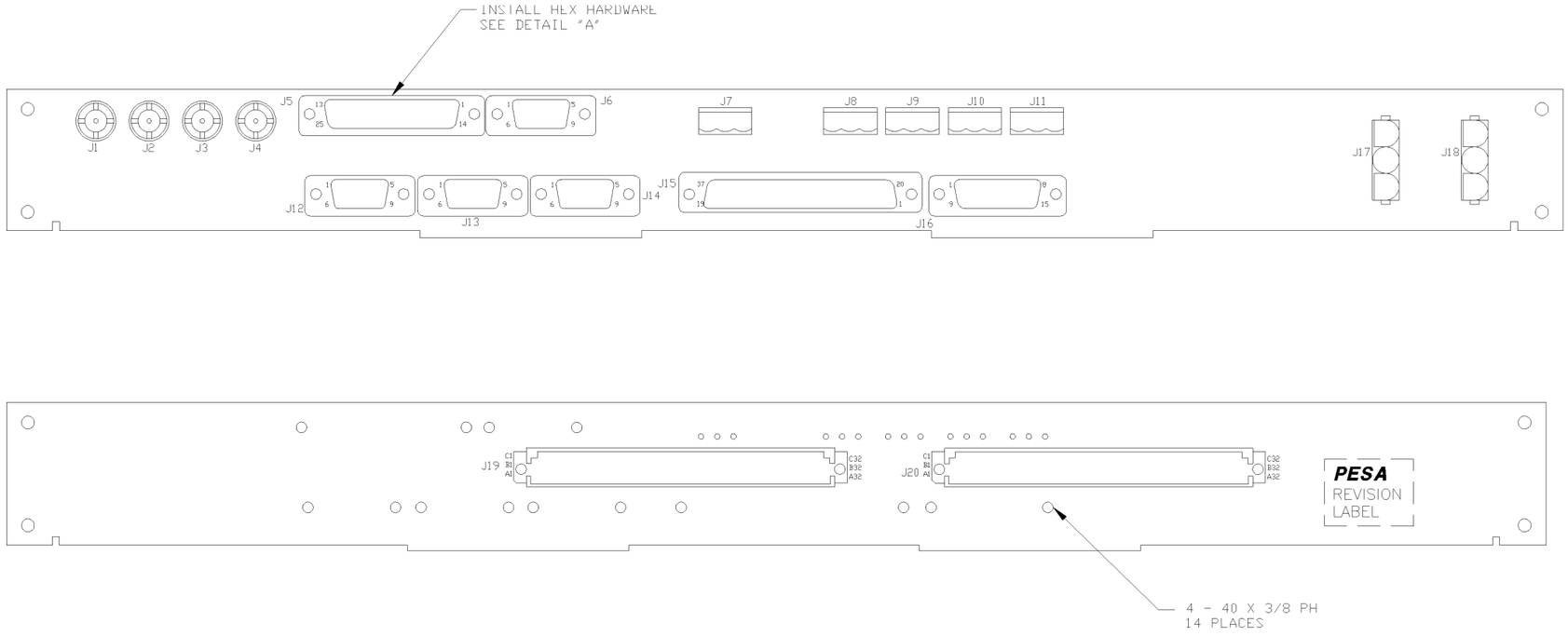
General

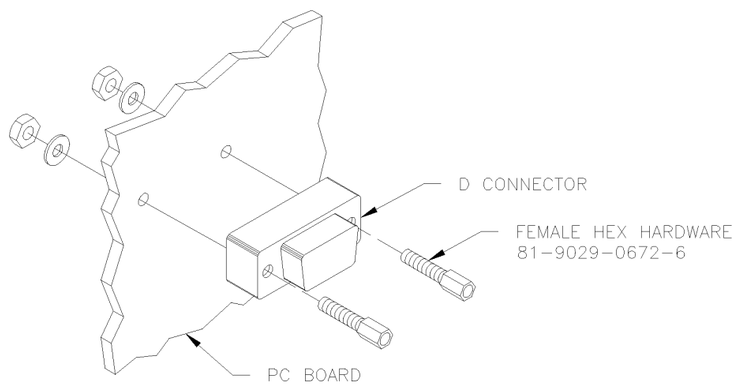
This section contains the schematic diagrams and parts location diagrams for the System V to PRC Bus Interface . Please refer to this section when troubleshooting the equipment or replacing defective parts.

4	81906518850	SYSTEM 5 BUS INTER ASSY	1.0	EA
3	81906515100	BACKPLANE/CHASSIS ASSY	1.0	EA
2	81902101500	LABEL WARNING FCC-EMI	1.0	EA
1	81902101468	LABEL EQUIP SERIALIZATION	1.0	EA
NO	PART NUMBER	DESCRIPTION	QTY	UNIT
HARDWARE SCHEDULE				



Configuration Drawing • System V Bus Interface Assembly • CD63-0780



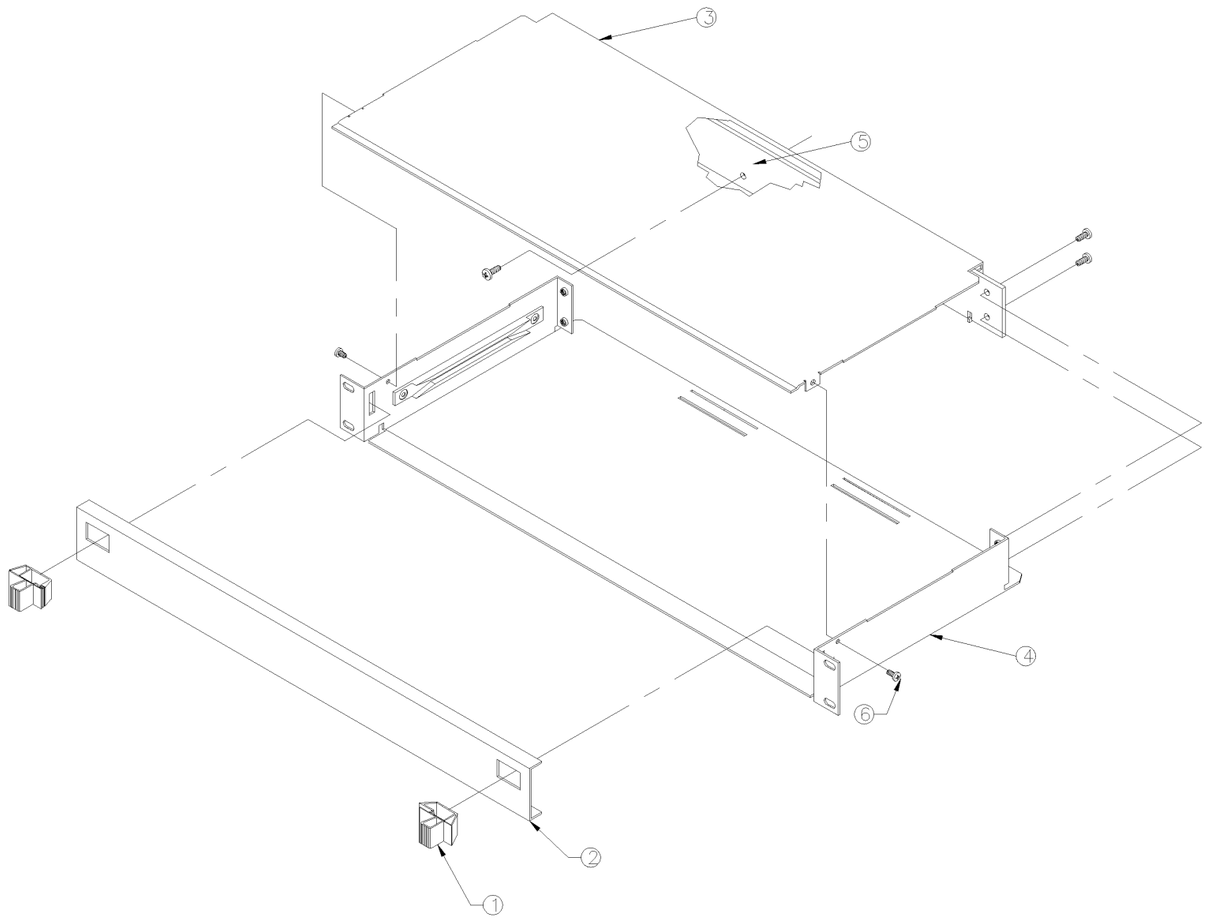


DETAIL "A"

NOTES: (UNLESS OTHERWISE POSTED)

1. INSTALLATION OF J19 AND J20 MUST BE COMPLETED FIRST.
2. INSTALLATION OF J17 AND J18 MUST BE COMPLETED SECOND.
3. ALL OTHER CONNECTORS TO BE SOLDERED.

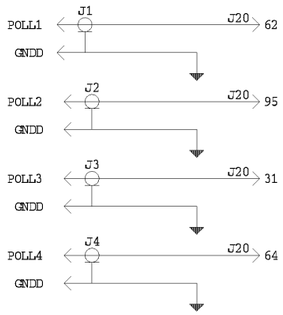
NO	REF. DESIGNATOR	DESCRIPTION	QTY	UNIT
		HARDWARE SCHEDULE		
6	81902202704	SCREW, 4-40 X 3/8	7.0	EA
5	81902411830	BACKPLANE ASSY	1.0	EA
4	81903462180	TRAY	1.0	EA
3	81903462190	TOP/REAR	1.0	EA
2	81903462200	FRONT DOOR	1.0	EA
1	81902003227	SNAP-IN LATCH	2.0	EA

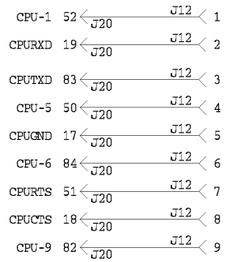


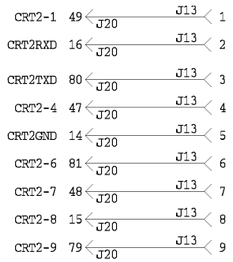
NOTES:

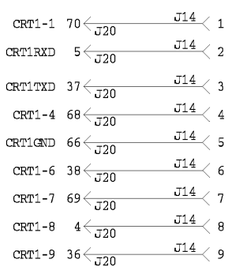
1. INSTALL BACKPLANE TO TOP/REAR COVER WITH ONE 4 - 40 X 3/8 SCREW. INSURE SLOTS & TABS ON EACH END ARE SECURE.
2. WITH BACKPLANE ATTACHED ALIGN THE METAL AND PCB TABS ON THE BOTTOM WITH THE SLOTS IN THE TRAY.
3. SECURE THE PCB/TOP/REAR ASSY TO THE TRAY AS SHOWN.
4. WITH THE SNAP-IN LATCH'S INSTALLED TO THE FRONT DOOR, PUSH THE DOOR OVER THE CHASSIS RELIEFED EDGES UNTIL THE LATCHES SNAP INTO PLACE.

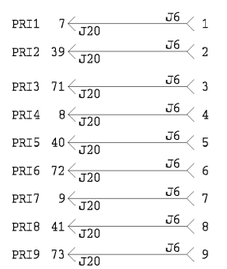
Component Assembly (Sheet 2 of 2) • Backplane/Chassis Assembly • CA25-1183

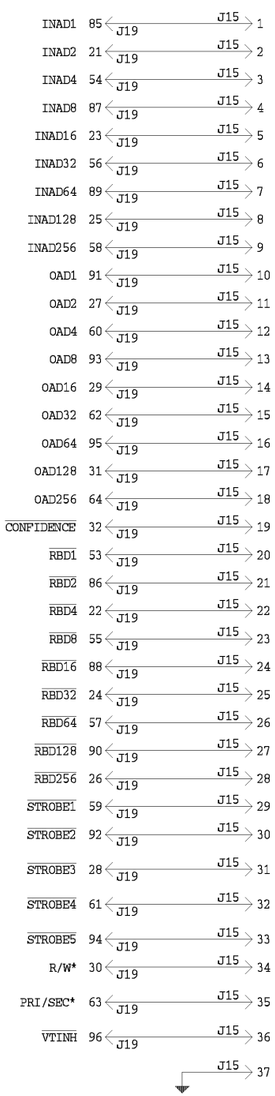

POLL1 J1 J20 62
GNDD
POLL2 J2 J20 95
GNDD
POLL3 J3 J20 31
GNDD
POLL4 J4 J20 64
GNDD

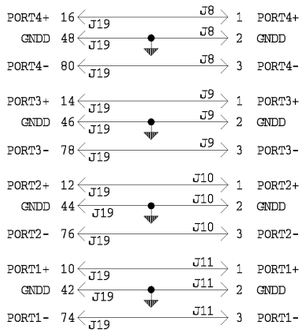

CPU-1 52 J20 J12 1
CPURXD 19 J20 J12 2
CPUTXD 83 J20 J12 3
CPU-5 50 J20 J12 4
CPUGND 17 J20 J12 5
CPU-6 84 J20 J12 6
CPURTS 51 J20 J12 7
CPUCTS 18 J20 J12 8
CPU-9 82 J20 J12 9

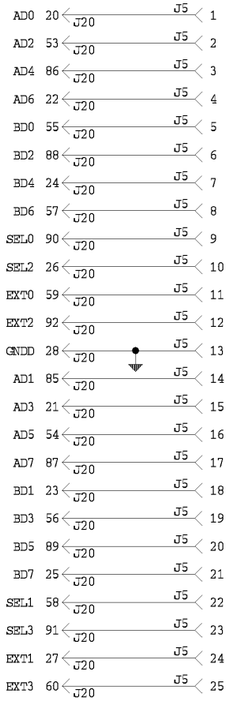

CRT2-1 49 J20 J13 1
CRT2RXD 16 J20 J13 2
CRT2TXD 80 J20 J13 3
CRT2-4 47 J20 J13 4
CRT2GND 14 J20 J13 5
CRT2-6 81 J20 J13 6
CRT2-7 48 J20 J13 7
CRT2-8 15 J20 J13 8
CRT2-9 79 J20 J13 9

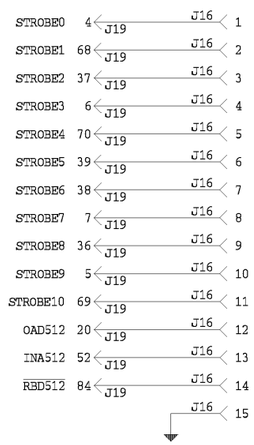

CRT1-1 70 J20 J14 1
CRT1RXD 5 J20 J14 2
CRT1TXD 37 J20 J14 3
CRT1-4 68 J20 J14 4
CRT1GND 66 J20 J14 5
CRT1-6 38 J20 J14 6
CRT1-7 69 J20 J14 7
CRT1-8 4 J20 J14 8
CRT1-9 36 J20 J14 9

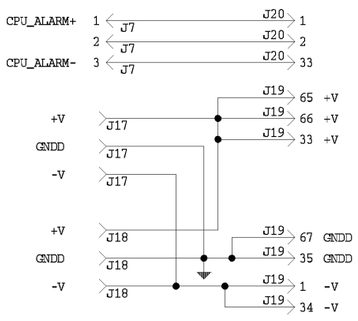

PRI1 7 J20 J6 1
PRI2 39 J20 J6 2
PRI3 71 J20 J6 3
PRI4 8 J20 J6 4
PRI5 40 J20 J6 5
PRI6 72 J20 J6 6
PRI7 9 J20 J6 7
PRI8 41 J20 J6 8
PRI9 73 J20 J6 9

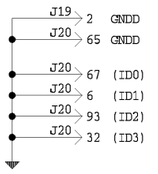

INAD1 85 J19 J15 1
INAD2 21 J19 J15 2
INAD4 54 J19 J15 3
INAD8 87 J19 J15 4
INAD16 23 J19 J15 5
INAD32 56 J19 J15 6
INAD64 89 J19 J15 7
INAD128 25 J19 J15 8
INAD256 58 J19 J15 9
OAD1 91 J19 J15 10
OAD2 27 J19 J15 11
OAD4 60 J19 J15 12
OAD8 93 J19 J15 13
OAD16 29 J19 J15 14
OAD32 62 J19 J15 15
OAD64 95 J19 J15 16
OAD128 31 J19 J15 17
OAD256 64 J19 J15 18
CONFIDENCE 32 J19 J15 19
RBD1 53 J19 J15 20
RBD2 86 J19 J15 21
RBD4 22 J19 J15 22
RBD8 55 J19 J15 23
RBD16 88 J19 J15 24
RBD32 24 J19 J15 25
RBD64 57 J19 J15 26
RBD128 90 J19 J15 27
RBD256 26 J19 J15 28
STROBE1 59 J19 J15 29
STROBE2 92 J19 J15 30
STROBE3 28 J19 J15 31
STROBE4 61 J19 J15 32
STROBE5 94 J19 J15 33
R/W* 30 J19 J15 34
PRI/SEC* 63 J19 J15 35
VTINH 96 J19 J15 36
J15 37 GNDD

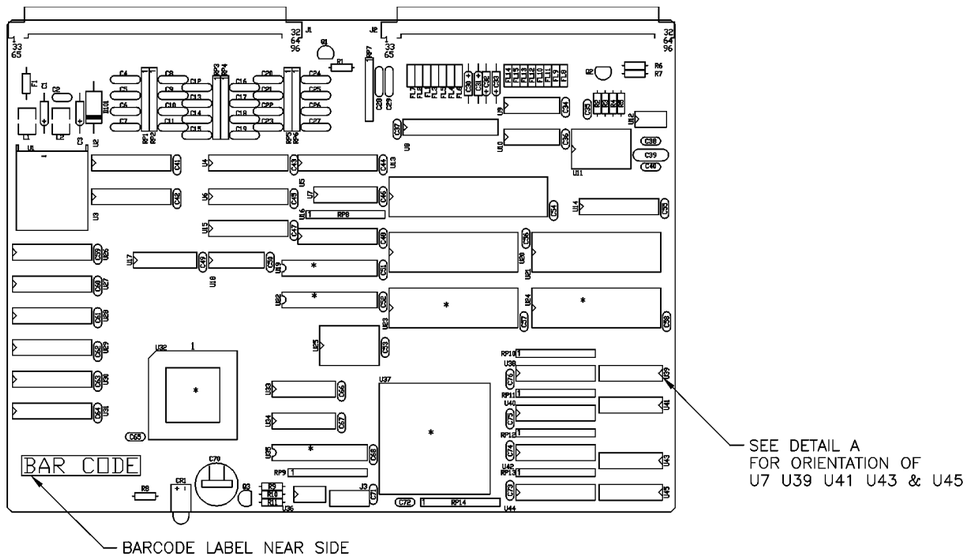

PORT4+ 16 J19 J8 1 PORT4+
GNDD 48 J19 J8 2 GNDD
PORT4- 80 J19 J8 3 PORT4-
PORT3+ 14 J19 J9 1 PORT3+
GNDD 46 J19 J9 2 GNDD
PORT3- 78 J19 J9 3 PORT3-
PORT2+ 12 J19 J10 1 PORT2+
GNDD 44 J19 J10 2 GNDD
PORT2- 76 J19 J10 3 PORT2-
PORT1+ 10 J19 J11 1 PORT1+
GNDD 42 J19 J11 2 GNDD
PORT1- 74 J19 J11 3 PORT1-

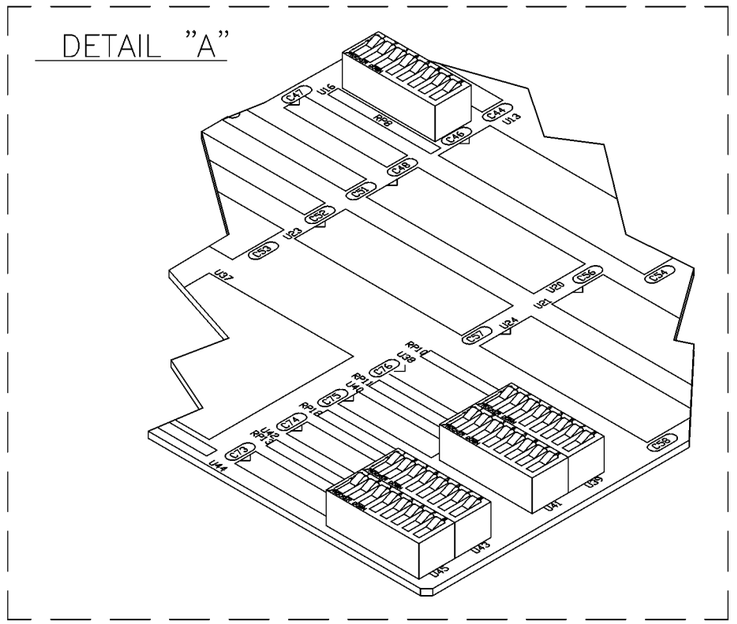

AD0 20 J20 J5 1
AD2 53 J20 J5 2
AD4 86 J20 J5 3
AD6 22 J20 J5 4
BD0 55 J20 J5 5
BD2 88 J20 J5 6
BD4 24 J20 J5 7
BD6 57 J20 J5 8
SEL0 90 J20 J5 9
SEL2 26 J20 J5 10
EXT0 59 J20 J5 11
EXT2 92 J20 J5 12
GNDD 28 J20 J5 13
AD1 85 J20 J5 14
AD3 21 J20 J5 15
AD5 54 J20 J5 16
AD7 87 J20 J5 17
BD1 23 J20 J5 18
BD3 56 J20 J5 19
BD5 89 J20 J5 20
BD7 25 J20 J5 21
SEL1 58 J20 J5 22
SEL3 91 J20 J5 23
EXT1 27 J20 J5 24
EXT3 60 J20 J5 25

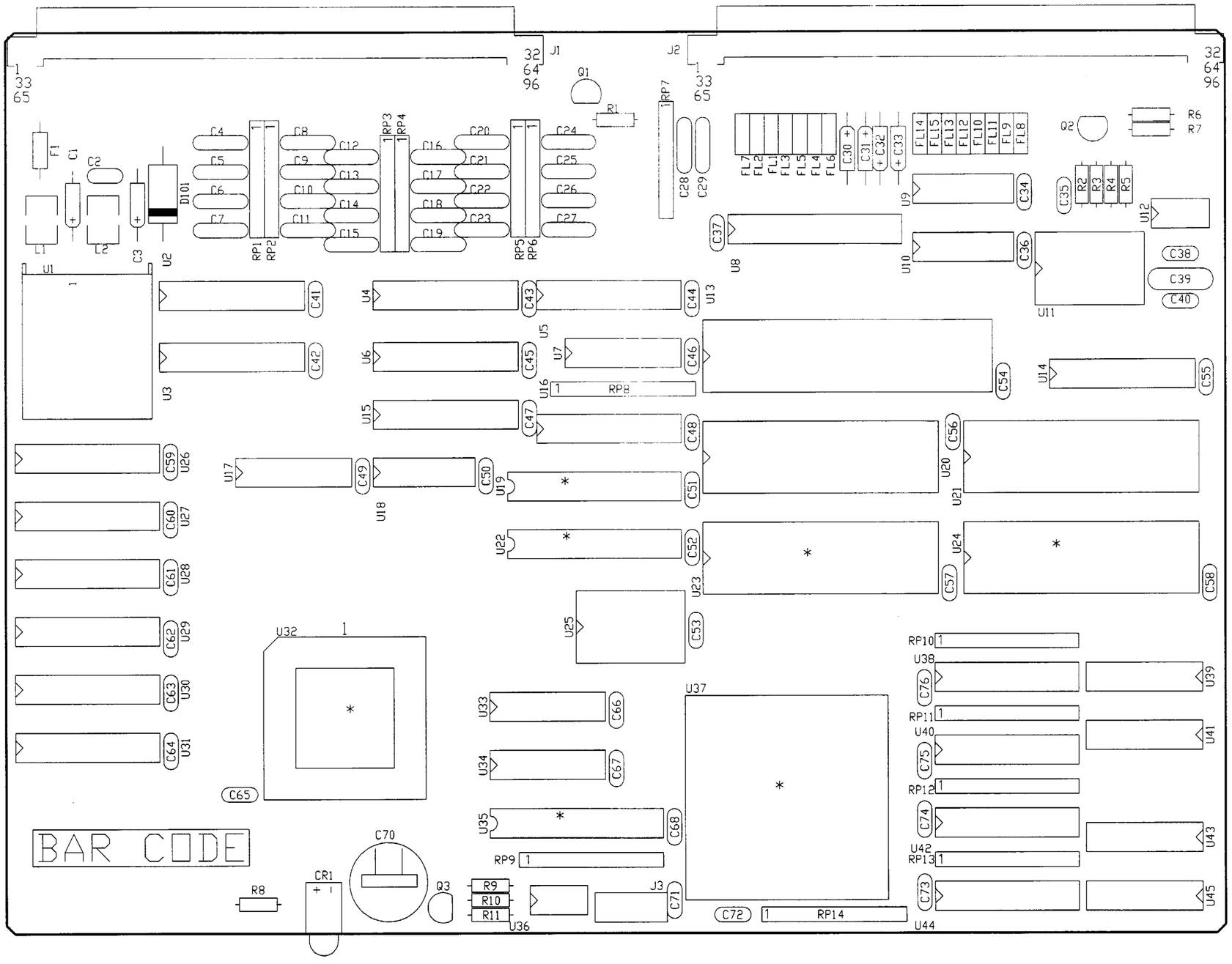

STROBE0 4 J19 J16 1
STROBE1 68 J19 J16 2
STROBE2 37 J19 J16 3
STROBE3 6 J19 J16 4
STROBE4 70 J19 J16 5
STROBE5 39 J19 J16 6
STROBE6 38 J19 J16 7
STROBE7 7 J19 J16 8
STROBE8 36 J19 J16 9
STROBE9 5 J19 J16 10
STROBE10 69 J19 J16 11
OAD512 20 J19 J16 12
INA512 52 J19 J16 13
RBD512 84 J19 J16 14
J16 15


CPU_ALARM+ 1 J7 J20 1
2 J7 J20 2
CPU_ALARM- 3 J7 J20 33
+V J17 J19 65 +V
J19 66 +V
GNDD J17 J19 33 +V
-V J17
+V J18 J19 67 GNDD
GNDD J18 J19 35 GNDD
-V J18 J19 1 -V
J19 34 -V

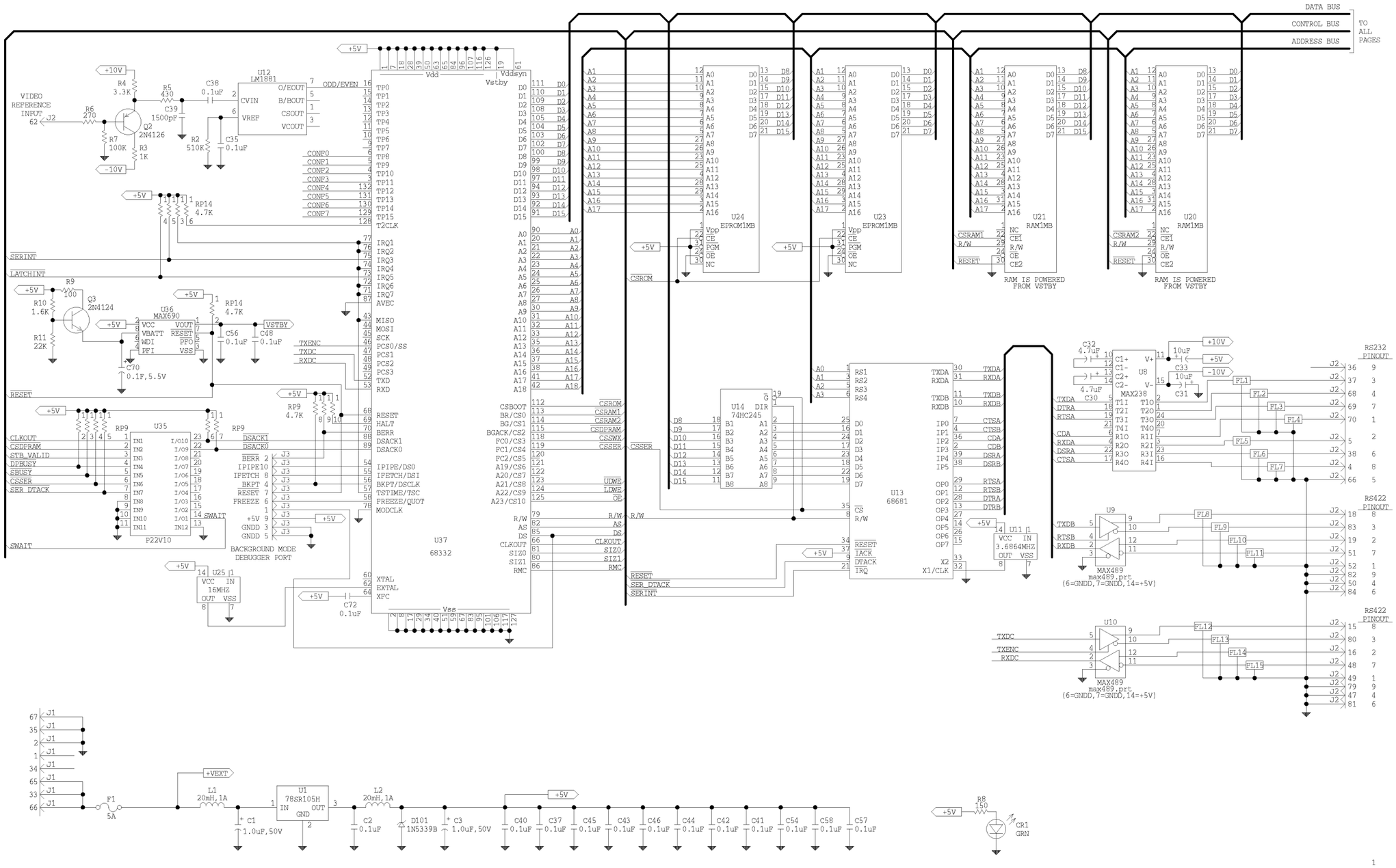

J19 2 GNDD
J20 65 GNDD
J20 67 (ID0)
J20 6 (ID1)
J20 93 (ID2)
J20 32 (ID3)


BAR CODE
BARCODE LABEL NEAR SIDE
SEE DETAIL A
FOR ORIENTATION OF
U7 U39 U41 U43 & U45

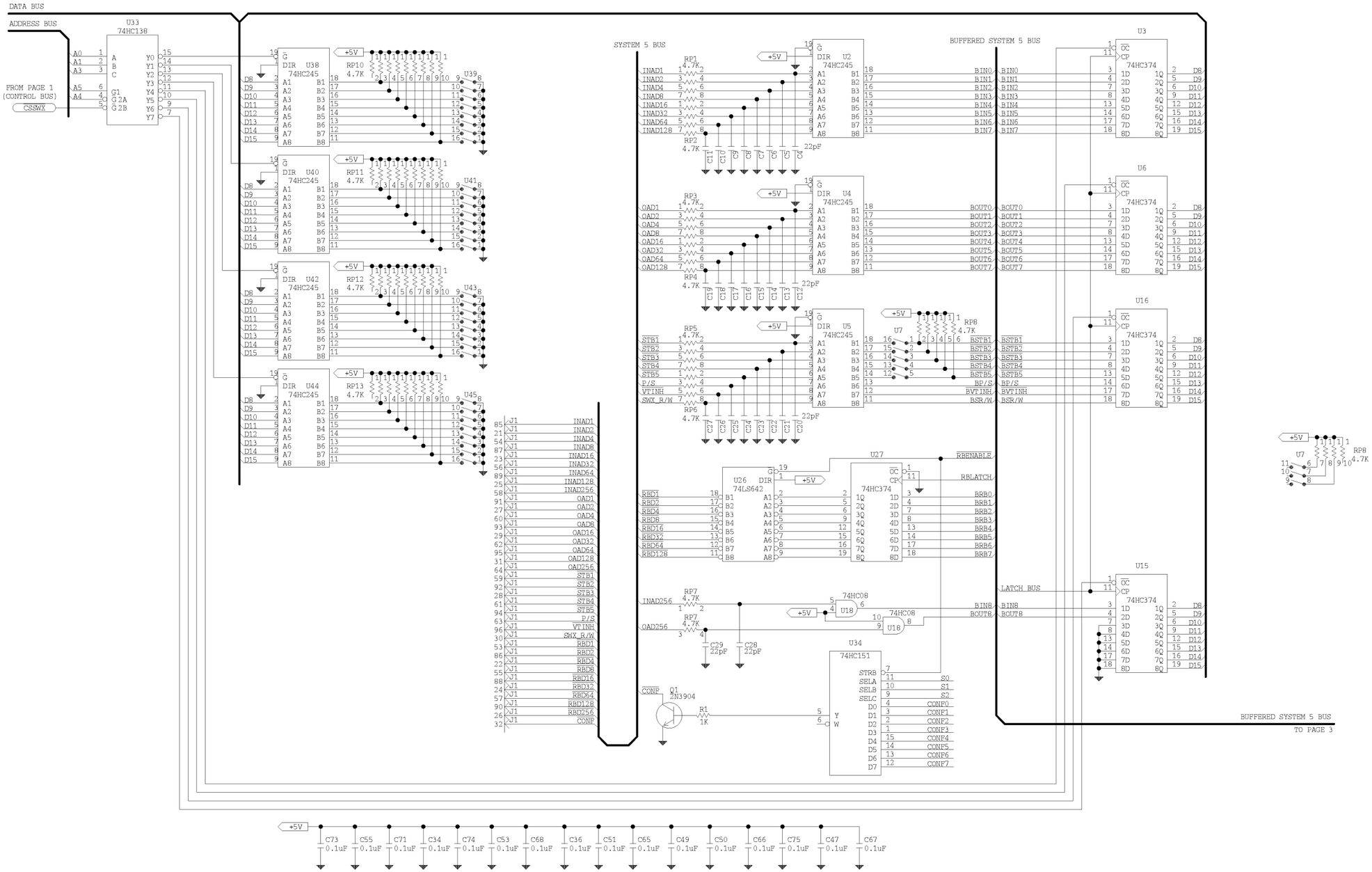

DETAIL "A"



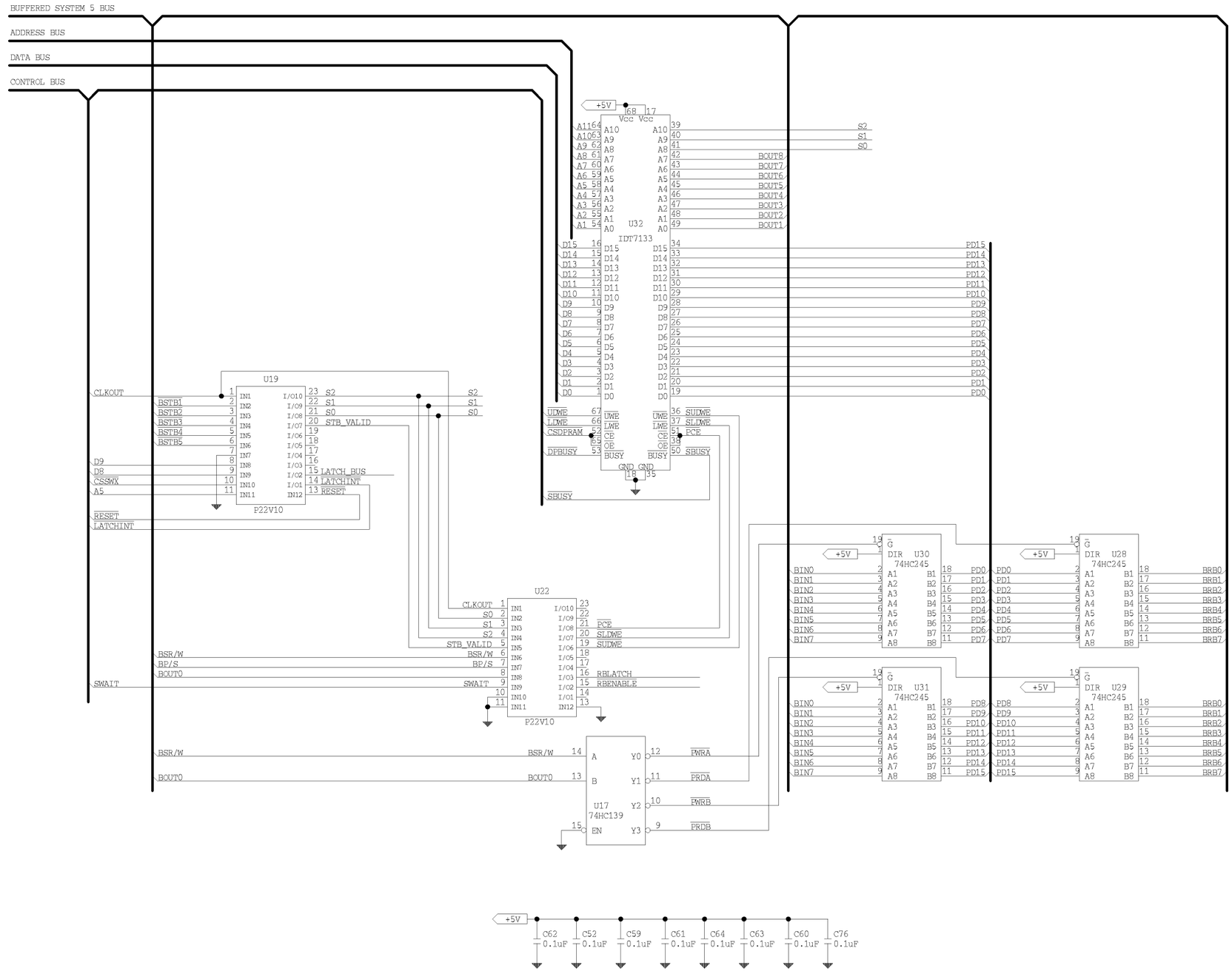
Component Assembly (Sheet 2 of 2) • System V Bus Interface Card • CA25-1352



Schematic (Sheet 1 of 3) • System V Bus Interface Card • SC33-1352



Schematic (Sheet 2 of 3) • System V Bus Interface Card • SC33-1352



Schematic (Sheet 3 of 3) • System V Bus Interface Card • SC33-1352

7.1 Parts List

General

The Parts List in this section have been grouped according to each assembly associated with the System V to PRC Bus Interface. Refer to each list by name of card, board, or section of the equipment requiring replacement parts.

System V Bus Interface Assembly - 81906519060

81901702830	ADAPTER 37D FEMALE/FEMALE	1	EA
81902101468	LABEL EQUIPMENT SERIALIZATION	1	EA
81902101500	LABEL WARNING FCC-EMI	1	EA
81902804000	CABLE 9 PIN F TO 9 PIN F	1	EA
81906511892	CABLE LOOP THRU CONTROL	1	EA
81906515100	BACKPLANE/CHASSIS ASSEMBLY	1	EA
81906516530	CABLE POWER 24X16 EXT 3-6	1	EA
81906518850	SYSTEM V BUS INTERFACE CARD	1	EA
CD63-0780	DOC SYSTEM V BUS INTERFACE	REF	

Backplane/Chassis Assembly - 81906515100

81902003227	LATCH SLIDE BLACK TAB CEI	2	EA
81902202704	SCREW 4-40X3/8 PAN HEAD SIMM	21	EA
81902411830	PCB BACKPLANE SRU 6600EXS	1	EA
81902905421	CONN 25-PIN D FEMALE STR REC	1	EA
81902906320	CONN 3-PIN MALE PRESS-IN	2	EA
81902906353	CONN 3-POS MALE POLAR STR	5	EA
81902906726	HARDWARE HEX 4/40X.56 LNG	1	EA
81902906908	CONN 96-PIN MALE PRESS-IN	2	EA
81902906932	CONN 9-PIN MALE D SOLDER	4	EA
81902907370	CONN BNC SOLDER-IN 75 OHM	4	EA
81902907650	CONN 37-PIN "D" MALE 4-40	1	EA
81902907660	CONN 15-PIN "D" MALE 4-40	1	EA
81903462180	METAL TRAY SRU 6600EXS	1	EA
81903462190	METAL TOP/REAR 6600EXS	1	EA
81903462200	METAL FRONT DOOR 6600EXS	1	EA
PK65-1510	DOC TRAY/BPLN SRU 6600EXS	REF	

24X16 Power Cable Assemby - 81906516530

81902201714	SCREW #6X5/8 PAN HEAD	4	EA
81902800341	SHRINK TUBING 3/8" BLACK	4	IN
81902802453	WIRE 16AWG BLACK/RED/WHITE	72	IN
81902901602	CABLE HEAD M-N-L 6-POS RED	1	EA
81902901610	STRAIN RELIEF M-N-L RED	2	EA
81902903210	PIN MALE FOR M-N-L	3	EA
81902903228	PIN FEMALE FOR M-N-L	3	EA
81902906494	CONN PLUG M-N-L 3-POS RED	1	EA
81902906700	STRAIN RELIEF M-N-L RED	2	EA
PK65-1653	DOC CABLE POWER 24X16 EXT	REF	

Loop-Thru Control Cable - 81906511892

81902801232	WIRE 28 AWG 3302/37	100	IN
81902900265	SCREW HEX FEMALE	1	EA
81902904374	CONN 37-PIN MALE DELTA	2	EA
81902904382	CONN 37-PIN FEMALE RIBBON	1	EA
81902907580	SCREW MALE RETAINER (AMP)	2	EA
PK65-1189	DOC LOOPING CONTROL CABLE	REF	

System V Bus Interface Card - 81906518850

81900200429	RESISTOR 100 OHM 5% 1/4W	R9	1	EA
81900200460	RESISTOR 150 OHM 5% 1/4W	R8	1	EA
81900200528	RESISTOR 270 OHM 5% 1/4W	R6	1	EA
81900200577	RESISTOR 430 OHM 5% 1/4W	R5	1	EA
81900200668	RESISTOR 1K 5% 1/4W	R1 R3	2	EA
81900200718	RESISTOR 1.6K 5% 1/4W	R10	1	EA
81900200783	RESISTOR 3.3K 5% 1/4W	R4	1	EA
81900200981	RESISTOR 22K 5% 1/4W	R11	1	EA
81900201138	RESISTOR 100K 5% 1/4W	R7	1	EA
81900201302	RESISTOR 510K 5% 1/4W	R2	1	EA
81900600768	SIP 4.7K 8-PIN 4 RESISTOR	RP1-RP7	7	EA
81900600958	SIP 4.7K 10-PIN 9 RESISTOR	RP8-RP14	7	EA
81900700055	CAP 0.1MF 50V CERAMIC RADIAL	C2 C34-C38 C40-C68 C71-C76	41	EA
81900700295	CAP 22PF 1000V CERAMIC RADIAL	C4-C29	26	EA
81900800616	CAP 1500PF 300V MICA RADIAL	C39	1	EA
81900900168	CAP 1MF 50V TANTLM AXIAL	C1 C3	2	EA
81900900291	CAP 10MF 20V TANTLM AXIAL	C31 C33	2	EA
81900900309	CAP 4.7MF 20V TANTLM AXIAL	C30 C32	2	EA
81901000840	CAP 0.1F 5.5V	C70	1	EA
81901400051	TRANS 2N4124 NPN TO-92	Q1 Q3	2	EA
81901400069	TRANS 2N4126 PNP TO-92	Q2	1	EA
81901500930	ZENER IN5339B 5.6V 5W	D101	1	EA
81901604314	IC 74HC245 CMOS BUSTRANSV	U2 U4 U5 U14 U28-U31 U38 U40 U42 U44	12	EA
81901604827	IC 1 OF 8 DECODER/MULTIPLXR	U33	1	EA
81901605139	IC 74HC374 OCTAL D-FLIP FL	U3 U6 U15 U16 U27	5	EA
81901606061	IC MAX690CPA PWR SUP MON	U36	1	EA
81901606079	IC IDT7133L70J DUAL PORT	U32	1	EA
81901601611	IC 16MHZ OSCILLATOR	U25	1	EA
81901606178	IC 128KX8 STATIC RAM 70NS	U20 U21	2	EA
81901606196	IC 68681 DUAL UART REC/TX	U13	1	EA
81901606251	IC LM1881 VIDEO SYNC SEPAR	U12	1	EA
81901606376	IC MAX238 RS232 DRVR/RCVR	U8	1	EA
81901606720	OSCILLATOR 3.6864MHZ	U11	1	EA
81901606840	IC 74HC08 QUAD AND 2 INPUT	U18	1	EA
81901606900	IC 68322 PROCESS 16.78MHZ	U37	1	EA
81901606920	REG 78SR105 +5V SWITCHING	U1	1	EA
81901607020	DECODER 74HC139 DUAL 1 OF 4	U17	1	EA
81901607110	IC 74HC151 8 INPUT MUX	U34	1	EA
81901607120	IC 74LS642 OCTAL BUS TNSC	U26	1	EA
81901607130	IC MAX489 RS485/RS422 INT	U9 U10	2	EA
81902202647	SCREW 4-40X1/4 SIMM PAN HEAD		4	EA
81902413520	PCB SYSTEM V BUS INTERFACE		1	EA
81902600436	SWITCH 8-POS DIP 16-PIN	U7 U39 U41 U43 U45	5	EA
81902700880	FUSE 5A PICO AXIAL 125V	F1	1	EA
81902905652	SOCKET 24-PIN DIP .3" CENTER	REF: U19 U22 U35	3	EA
81902906106	SOCKET 32-POS DIP .60CL	REF: U23 U24	2	EA

System V Bus Interface Card - 81906518850 Continued:

81902906114	SOCKET 68-POS PLCC	REF: U32	1	EA
81902906668	CONN R/A FEMALE 96-POS 3 ROW	J1 J2	2	EA
81902907470	CONN 132-PIN QFP FLAT PACK	REF: U37	1	EA
81902907480	CONN 132-PIN PQFP COVER	REF: U37	1	EA
81903200541	LED GREEN R/A HI-EFF PCB	CR1	1	EA
81903464920	SHIELD BUSS INT CARD SYS 5		1	EA
81903900700	INDUCT 20MH 1A TORIODIAL	L1 L2	2	EA
81903900740	FILTER EMI SUPPRESSION	FL1-FL15	15	EA
81906519040	SOFT SYS 5 BUS INTERFACE	REF: U23 U24	1	EA
81906519050	PLD SYS 5 BUS INTERFACE ASSY	REF: U19 U22 U35	1	EA

System V Bus Interface Software Assembly - 81906519050

81901606574	IC 22V10 EEPROM PLD 15NS	3	EA
81902104413	LABEL WHITE (.300 WIDE)	3	EA
81905603510	SOFT PLD PRC TO SYS 5 INT	REF	

System V Bus Interface Software - 81906519040

81901606210	IC 128KX8 EPROM	2	EA
81902103233	LABEL EPROM COPYRIGHT	2	EA
81905603500	SOFT PRC TO SYS 5 INT	REF	
81906203230	DOC PROGRAMMING EPROMS	REF	