# Design Guide
# For
# "Pesa AADC 3102"
# Audio Analog to Digital Converter

## Revision History:

| Revision | Filename | Date | Author |
|---|---|---|---|
| Draft | Pesa ADC - Design Guide - Draft Ax. Doc | 03/20/01 | John Siau |
| Rev A | Pesa ADC - Design Guide - Rev A. Doc | 04/05/01 | John Siau |

## MINIMUM PRODUCT REQUIREMENTS:

- Two AES/EBU digital channel pairs (total: four channels of audio)
- Three AES/EBU digital outputs per channel pair (total: six connectors)
- Jumper selected 75 ohm unbalanced, or 110 ohm balanced digital outputs
- One AES/EBU digital audio reference input – high-Z
- Must accept 44.1, 48, 88.2, and 96 kHz reference inputs
- Four balanced analog inputs
- Jumper selected 600 ohm or high-Z analog input impedance
- Maximum Analog Input Level = +30 dBu
- 24-bit 96-kHz or 48-kHz digital to analog conversion
- Two Stereo Headphone jacks – fixed level
- THD+N < 0.005%
- SNR 110 dB A-weighted
- Frequency Response < +/- 0.1 dB 20 to 20 kHz
- Must operate from unregulated +/- 24 (- 2.0, +6) VDC supply rails
- Loads on +/- 24 VDC supply must be balanced to within +/- 10%.
- Pesa DA3100 Form Factor

## ADDITIONAL FEATURES TO BE CONSIDERED:

- LR Swap
- Invert
- Sum
- Difference
- Tone Generator
- Error Indicators
- Clip Indicators
- Meters

## PRELIMINARY FEATURE SET:

- Two AES/EBU digital channel pairs (total: four channels of audio)
- Three AES/EBU digital outputs per channel pair (total: six connectors)
- Jumper selected 75 ohm unbalanced, or 110 ohm balanced digital outputs
- One AES/EBU digital audio reference input – high-Z
- Will accept 28 kHz to 100 kHz reference inputs
- Four balanced analog inputs
- Jumper selected 600 ohm or high-Z analog input impedance
- Maximum Analog Input Level = +30 dBu
- 24-bit 96-kHz at reference rates of 88.2 kHz and above
- 24-bit 48-kHz conversion at reference rates below 88.2 kHz
- Full varispeed capability
- Two Stereo Headphone jacks – fixed level – pre-conversion
- Operates from unregulated +/- 24 (- 2.0, +6) VDC supply rails
- Pesa DA3100 Form Factor
- Benchmark Phase Accurate – Jitter Immune - SRC ADC technology
- Lock LED
- 96 kHz LED
- Four Power LEDs
- Adjustable Input Levels – Multi-turn trimmers – 1 trimmer per input (Range TBD)
- Tone Generator will not be included.
- Modular DC to DC converter to power digital circuits
- Linear +/- 20 VDC regulators for analog stage
- Four Signal Presence LEDs (-20 dBFS)
- Four Clip LEDs (0 dBFS)

## PRELIMINARY SPECIFICATIONS:

### *Analog:*

- Maximum Input Level = +30 dBu
- Maximum Sensitivity (trimmers fully CW) = 0 dBFS at +0 dBu
- Minimum Sensitivity (trimmers fully CCW) = 0 dBFS at +30 dBu
- Input Impedance = 66 or 600 ohms – jumper selected

### *Digital:*

- Word Length = 24, 20, 18 or 16-bits – jumper selected
- Sample Frequency Range = 28 to 100 kHz
- THD+N < 0.005%
- SNR > 110 dB A-weighted
- Frequency Response < +/- 0.1 dB 20 to 20 kHz at Fs = 48 kHz
- Digital Output Impedance = 75 ohm unbalanced, or 110 ohm balanced (jumper selected)
- Digital Reference Input Impedance = High-Z

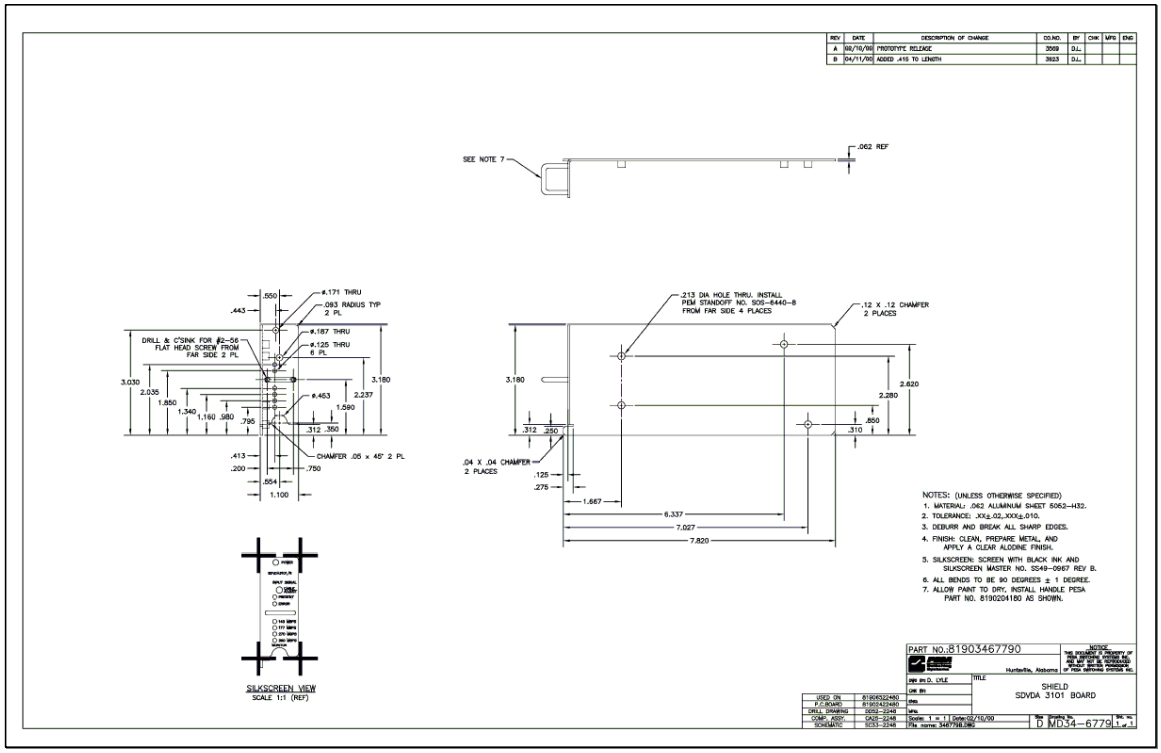
### *Power Supply:*

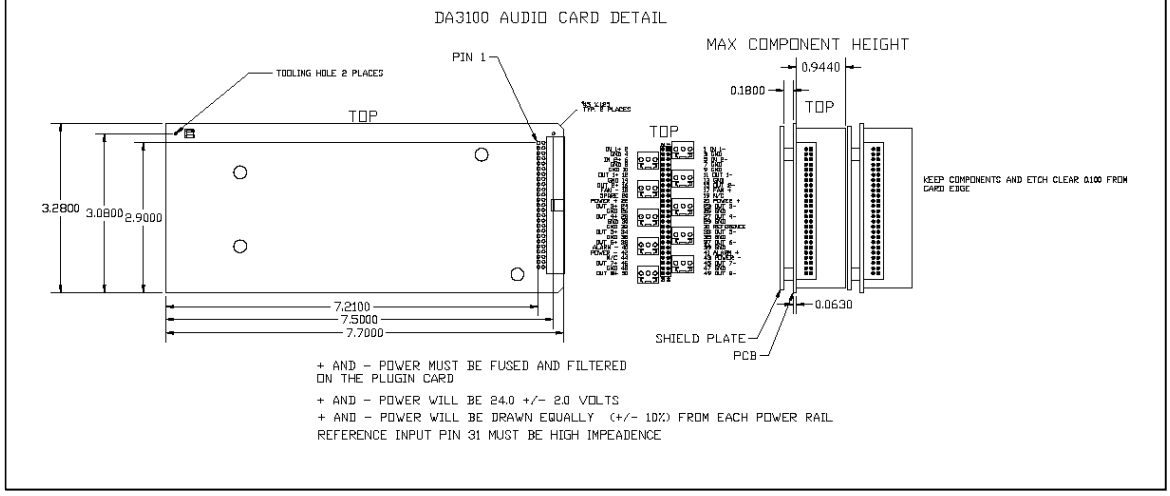
- Minimum Supply Voltage = +/- 22 VDC.
- Maximum Allowable Supply Voltage = +/- 35 VDC
- Loads on +/- 24 VDC supply are balanced to within +/- 10%.

### *Mechanical:*

- Pesa DA3100 Form Factor
- Card Shield/Faceplate – Not Included (To be added or supplied by Pesa)

## DIMENSIONS:


SEE NOTE 7
.062 REF
.213 DIA HOLE THRU. INSTALL PEM STANDOFF NO. SOS-6440-8 FROM FAR SIDE 4 PLACES
.12 X .12 CHAMFER 2 PLACES
.04 X .04 CHAMFER 2 PLACES
SILKSCREEN VIEW
SCALE 1:1 (REF)
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. MATERIAL: .062 ALUMINUM SHEET 5052-H32.
2. TOLERANCE: XX±.02,.XXX±.010.
3. DEBURR AND BREAK ALL SHARP EDGES.
4. FINISH: CLEAN, PREPARE METAL, AND APPLY A CLEAR ALODINE FINISH.
5. SILKSCREEN: SCREEN WITH BLACK INK AND SILKSCREEN MASTER NO. SS49-0967 REV B.
6. ALL BENDS TO BE 90 DEGREES ± 1 DEGREE.
7. ALLOW PAINT TO DRY. INSTALL HANDLE PESA PART NO. 8190204180 AS SHOWN.
PART NO.:81903467790
SHIELD
SDVDA 3101 BOARD


DA3100 AUDIO CARD DETAIL
MAX COMPONENT HEIGHT
TOOLING HOLE 2 PLACES
PIN 1
TOP
TOP
TOP
3.2800
3.0800
2.9000
7.2100
7.5000
7.7000
0.9440
0.1800
0.0630
SHIELD PLATE
PCB
KEEP COMPONENTS AND ETCH CLEAR 0.100 FROM CARD EDGE
+ AND - POWER MUST BE FUSED AND FILTERED ON THE PLUGIN CARD
+ AND - POWER WILL BE 24.0 +/- 2.0 VOLTS
+ AND - POWER WILL BE DRAWN EQUALLY (+/- 10%) FROM EACH POWER RAIL
REFERENCE INPUT PIN 31 MUST BE HIGH IMPEADENCE

# I/O:

### *Analog Inputs:*

- Four analog inputs.
- EMI filtered.
- Input Impedance selected with jumpers (one jumper per input).
- Input sensitivity adjustable via trimmer (one trimmer per analog channel).
- Input sensitivity adjustment range = 30 dB (0 dBFS at 0 dBu to +30 dBu).

### *Digital Outputs:*

- Six AES/EBU balanced outputs (balanced feed to rear panel for both 75 and 100-ohm operation).
- Transformer Coupled
- Single 3-pin jumper per output for selection of 75 ohm or 110 ohm output impedance.
- DC blocking capacitors after transformers.
- Series resistor for protection and isolation of non-powered or faulty outputs.
- Diode ESD and overload protection.
- Shield and "S-" should be tied together at rear panel connector when feeding 75-ohm unbalanced loads.

### *Digital Reference I/O Port:*

This port is bi-directional. A 3-pin "MASTER/SLAVE" jumper controls port direction.

- In "SLAVE" mode this port acts as a high-z unbalanced input.
- In "MASTER" mode this port acts as a 75-ohm unbalanced output.

#### Digital Reference Input - "Slave" Mode (factory default):

This input is connected to the reference bus on the Pesa card frame. It provides a phase and frequency reference to which the digital outputs will lock.

- Accepts AES/EBU professional or consumer digital audio formats
- Does not accept video, or word clock signals
- Unbalanced
- High-Z
- Transformer Coupled
- DC blocking capacitor before transformer
- Series resistor for protection and isolation of a non-powered or faulty input.
- Diode ESD and overload protection

#### Digital Reference Output - "Master" Mode:

This output provides a phase and frequency reference to which other devices can be locked.

- AES/EBU professional-format unbalanced 75-ohm output
- 1 Vpp into 75-ohms
- Transformer Coupled
- DC blocking capacitor after transformer
- Series resistor for protection and isolation of a non-powered or faulty output.
- Diode ESD and overload protection

***Pin Assignments:***

| | | | |
|---|---|---|---|
| A IN 1+ | 2 | 1 | A IN 1- |
| GND | 4 | 3 | GND |
| A IN 2+ | 6 | 5 | A IN 2- |
| GND | 8 | 7 | GND |
| GND | 10 | 9 | GND |
| A IN 3+ | 12 | 11 | A IN 3- |
| GND | 14 | 13 | GND |
| A IN 4+ | 16 | 15 | A IN 4- |
| N/C | 18 | 17 | N/C |
| N/C | 20 | 19 | N/C |
| POWER + | 22 | 21 | POWER + |
| D OUT 12 A+ | 24 | 23 | D OUT 12 A- |
| GND | 26 | 25 | GND |
| D OUT 12 B+ | 28 | 27 | D OUT 12 B- |
| GND | 30 | 29 | GND |
| GND | 32 | 31 | D REF IN |
| D OUT 12 C+ | 34 | 33 | D OUT 12 C- |
| GND | 36 | 35 | GND |
| D OUT 34 A+ | 38 | 37 | D OUT 34 A- |
| N/C | 40 | 39 | GND |
| POWER - | 42 | 41 | N/C |
| N/C | 44 | 43 | POWER - |
| D OUT 34 B+ | 46 | 45 | D OUT 34 B- |
| GND | 48 | 47 | GND |
| D OUT 34 C+ | 50 | 49 | D OUT 34 C- |

## POWER REQUIREMENTS:

### *Available Power:*

+/- 24 volts unregulated
Minimum unregulated input voltage = +/- 22 volts.
Maximum unregulated input voltage = +/- 30 volts.
Allowable current draw = 200 mA at unregulated inputs
Loads to be balanced to better than +/- 10 %

### *Power Requirement Calculations:*

Maximum Requirements with +30 dBu Input Levels, and 2 Digital Loads:

| Component | Qty | Amps at +5V | Amps at 3.3V | Amps at +/- 20V | DC to DC Amps Out | DC to DC Efficiency | Amps at +/-24V | Watts on Card | Watts Total |
|---|---|---|---|---|---|---|---|---|---|
| AES REC | 1 | 0.000 | 0.040 | 0.000 | 0.040 | 85% | 0.005 | 0.24 | 0.24 |
| SRC | 2 | 0.000 | 0.086 | 0.000 | 0.086 | 85% | 0.011 | 0.51 | 0.51 |
| ADC | 2 | 0.260 | 0.000 | 0.000 | 0.260 | 85% | 0.032 | 1.53 | 1.53 |
| AES XMIT | 1 | 0.003 | 0.000 | 0.000 | 0.003 | 85% | 0.000 | 0.02 | 0.02 |
| AES LOADS | 2 | 0.146 | 0.000 | 0.000 | 0.146 | 85% | 0.018 | 0.52 | 0.86 |
| XCO | 2 | 0.030 | 0.000 | 0.000 | 0.030 | 85% | 0.004 | 0.18 | 0.18 |
| FPGA | 1 | 0.030 | 0.000 | 0.000 | 0.030 | 85% | 0.004 | 0.18 | 0.18 |
| LED | 16 | 0.128 | | 0.000 | 0.128 | 85% | 0.016 | 0.75 | 0.75 |
| LED Buffer | 1 | 0.000 | | 0.000 | 0.000 | 85% | 0.000 | 0.00 | 0.00 |
| 5532 Op Amp | 7 | 0.000 | 0.000 | 0.070 | 0.000 | 85% | 0.070 | 3.36 | 3.36 |
| **TOTALS** | **27** | **0.597** | **0.126** | **0.070** | **0.723** | | **0.159** | **7.27** | **7.61** |

Maximum Requirements with +30 dBu Input Levels, and 7 Digital Loads *:

| Component | Qty | Amps at +5V | Amps at 3.3V | Amps at +/- 20V | DC to DC Amps Out | DC to DC Efficiency | Amps at +/-24V | Watts on Card | Watts Total |
|---|---|---|---|---|---|---|---|---|---|
| AES REC | 1 | 0.000 | 0.040 | 0.000 | 0.040 | 85% | 0.005 | 0.24 | 0.24 |
| SRC | 2 | 0.000 | 0.086 | 0.000 | 0.086 | 85% | 0.011 | 0.51 | 0.51 |
| ADC | 2 | 0.260 | 0.000 | 0.000 | 0.260 | 85% | 0.032 | 1.53 | 1.53 |
| AES XMIT | 1 | 0.003 | 0.000 | 0.000 | 0.003 | 85% | 0.000 | 0.02 | 0.02 |
| AES LOADS | 7 | 0.511 | 0.000 | 0.000 | 0.511 | 85% | 0.063 | 1.80 | 3.01 |
| XCO | 2 | 0.030 | 0.000 | 0.000 | 0.030 | 85% | 0.004 | 0.18 | 0.18 |
| FPGA | 1 | 0.030 | 0.000 | 0.000 | 0.030 | 85% | 0.004 | 0.18 | 0.18 |
| LED | 16 | 0.128 | | 0.000 | 0.128 | 85% | 0.016 | 0.75 | 0.75 |
| LED Buffer | 1 | 0.000 | | 0.000 | 0.000 | 85% | 0.000 | 0.00 | 0.00 |
| 5532 Op Amp | 7 | 0.000 | 0.000 | 0.070 | 0.000 | 85% | 0.070 | 3.36 | 3.36 |
| **TOTALS** | **32** | **0.962** | **0.126** | **0.070** | **1.088** | | **0.203** | **8.56** | **9.76** |

** Note: With 7 Loads Connected, 1.2 Watts are dissipated off card (in the termination resistors).*

## THEORY OF OPERATION:

The A/D converter ICs operate at a fixed sample rate of either 48 kHz or 96 kHz (jumper selected). The clock for the A/D conversion is divided down from a very low-jitter fixed-frequency crystal oscillator. The resulting conversion is entirely free of jitter induced artifacts. The 48 kHz A/D sample rate is used for applications requiring an output sample rate between 28 kHz and 54 kHz. The 96 kHz A/D sample rate is normally used for applications requiring an output sample rate between 54 kHz and 100 kHz, but will also support output sample rates as low as 28 kHz.

The fixed frequency outputs of the A/D converters are fed to SRC (Sample Rate Converter) devices. The SRC devices convert the fixed-frequency output of the A/D converters, to any sample rate between 28 kHz and 100 kHz. The AD1896 ICs represent Analog Device Corporation's 3rd generation of SRC devices. These 3rd generation devices have extremely high performance. THD+N never exceeds –124 dBFS and is typically better than -130 dBFS. These artifacts are much lower than the jitter induced artifacts that plague single-stage PLL designs. Many two-stage PLL designs fail to keep jitter induced energy below –124 dBFS. Two stage PLL designs are also plagued with narrow lock ranges, and long acquire times. The Benchmark SRC ADC technology provides, low-cost and flexible solution with consistently high performance that is isolated from jitter effects.

The SRC devices match the phase and frequency of the digital audio outputs to that of the digital audio reference input. If a reference signal is not present the digital outputs will fall back to a jumper-selected fixed-frequency of either 48 kHz or 96 kHz.

## FALLBACK FREQUENCY SELECTION:

### *48 kHz Fallback – Factory Default:*

48 kHz operation is enabled with the “48/96” jumper. The jumper controls the A/D conversion frequency, the reference lock range, the digital output fallback frequency, and the “48 kHz” and “96 kHz” LED displays.

When the “48/96” jumper is set to “48”, the A/D converter chips operate at a fixed 48 kHz sample rate that is not effected by reference sample rate. This 48 kHz output from the A/D converters is sample rate converted to match the phase and frequency of the reference signal over a range exceeding 28 kHz to 54 kHz. The SRC outputs, and the digital audio transmitters, are slaved to the reference signal. If the reference signal is lost, or exceeds 54 kHz, the digital outputs will default to 48 kHz (derived from an internal crystal reference), and the “LOCK ERROR” LED will illuminate. The transition from external to internal reference is nearly transparent, and conversion quality is identical in either mode.

### *96 kHz Fallback:*

96 kHz operation is enabled with the “48/96” jumper. The jumper controls the A/D conversion frequency, the reference lock range, the digital output fallback frequency, and the “48 kHz” and “96 kHz” LED displays.

When the “48/96” jumper is set to “96”, the A/D converter chips operate at a fixed 96 kHz sample rate that is not effected by reference sample rate. This 96 kHz output from the A/D converters is sample rate converted to match the phase and frequency of the reference signal over a range exceeding 28 kHz to 100 kHz. The SRC outputs, and the digital audio transmitters, are slaved to the reference signal. If the reference signal is lost, the digital outputs will default to 96 kHz (derived from an internal crystal reference) and the “LOCK ERROR” LED will illuminate. The transition from external to internal reference is nearly transparent, and conversion quality is identical in either mode.

If the “48/96” jumper is set at “96”, reference signals below 54 kHz will illuminate the “RANGE ERROR” LED. The “RANGE ERROR” LED is simply a warning that the A/D conversion frequency, and the digital output fallback frequency do not match the reference frequency. Please note that a “RANGE ERROR” will not cause the audio to mute. A “RANGE ERROR” is simply a warning that the converter system is being operated in a non-optimal configuration. The 96 kHz output of the A/D converter chips will be sample rate converted to match the phase and frequency of the reference frequency.

## MASTER/SLAVE MODE SELECTION:

### *SLAVE MODE – Factory Default:*

The reference pin provides the input signal to the digital audio receiver. The digital audio receiver and digital audio outputs follow the phase and frequency of the digital audio reference.

### *MASTER MODE:*

This jumper-selected mode disables the digital audio reference input, and routes digital channel "1-2" to the reference pin. This 75 Ohm unbalanced digital audio reference signal is then distributed throughout the frame, and is available on the reference BNC connector at the rear of the frame. In a given frame, only one card may operate in "MASTER" mode. All other cards must be set to "SLAVE" mode. An entire second frame can be slaved to the output of a frame containing a card that is set to "MASTER" mode. The second frame is slaved to the first by connecting a BNC cable between the two reference jacks.

## AES/EBU RECEIVER (AK4112):

Receiver operates in a clock master mode, I2S FORMAT, with output clocks derived from received signal, with automatic fallback to a crystal reference. SRC outputs, and AES/EBU output transmitters are slaved to the receiver. The receiver is strapped in a parallel control mode. Lock range is 22 kHz to 108 kHz.

### *RECEIVER FALLBACK FUNCTION:*

If no reference signal is present, or if the reference signal cannot be decoded, the receiver will automatically switch to a crystal reference clock source. The receiver divides the crystal reference frequency by 512 (producing 48 kHz) or by 256 (producing 96 kHz) in order to provide the appropriate fallback sample rate at the I2S port. A 24.576 MHz crystal allows jumper selected fallback to either 48 kHz or 96 kHz. The OCKS1 pin is tied low for 48 kHz fallback and high for 96 kHz fallback. The crystal oscillator is connected to the XTI pin.

### *RECEIVER MODE PINS:*

**P**/S – **HIGH** – PARALLEL MODE ENABLED
RX2/**DF0** – **HIGH** – 24-BIT I2S – MASTER
RX2/**DF1** – **LOW** – 24-BIT I2S – MASTER
RX2/**DF2** – **HIGH** – 24-BIT I2S – MASTER
**OCKS0**/CSN – **LOW** – 256X at 96 kHz, 512X at 48 kHz
**OCKS1**/CCLK – **JUMPER SELECTED** – LOW = 96 kHz, HIGH = 48 kHz.
**CM0**/CDT0 – **LOW** – PLL, X'TAL FALLBACK
**CM1**/CDTI – **HIGH** – PLL, X'TAL FALLBACK

### *INPUT PINS:*

DAUX – Tie **LOW** – AUXILARY DIGITAL INPUT

### *OUTPUT PINS:*

**V**/TX – **NO CONNECTION** – VALIDITY BITS OUT
XTO – **NO CONNECTION** – CRYSTAL DRIVE PIN
MCLKO1 – To Transmitter "MCLK" – 512X/256X CLOCK OUTPUT
MCLKO2 – **NO CONNECTION** – 256X CLOCK OUTPUT

### *96 kHz STATUS OUTPUT PIN:*

FS96 – **HIGH = (96 kHz), LOW = (48 kHz or reference error)**

The FS96 pin changes state between 54 kHz and 88.2 kHz. The FS96 pin is guaranteed to be high at 88.2 kHz, and is guaranteed to be low at 48 kHz. The FS96 pin is also low whenever a valid reference signal is not detected. The FS96 pin will be used to drive a "RANGE ERROR" LED.

## Sample Rate Converter (AD1896):

### *SRC Delay Matching:*

Theory:

An 11-bit counter determines the sample rate ratio between FS_OUT and FS_IN. The equation for the ratio is as follows:

Ratio = (FS_OUT/FS_IN) * 2047

Since Ratio is an 11-bit number, truncate off any fractional part remaining.

Due to the hysteresis in measuring the Ratio in which the hysteresis is 2 LSBs, the Ratio value between two AD1896s can be off by 4 LSBs.

Lets call Ratio_True the true sample rate ratio between FS_IN and FS_OUT.

Lets call Ratio1 the ratio measured by the first AD1896 to be due to hysteresis.
Ratio1 = Ratio_True + 2

Lets call Ratio2 the ratio measured by the second AD1896 to be due to hysteresis.
Ratio2 = Ratio_True - 2

The number of taps used by the first AD1896 is:

# of taps = 2^17/Ratio1

The number of taps used by the second AD1896 is:

# of taps = 2^17/Ratio2

The difference in the number of taps between the two AD1896s would be:

2^17/Ratio2 - 2^17/Ratio1 = 2^17*[1/(Ratio_True - 2) - 1/(Ratio_True + 2)]

The group delay in the AD1896 is defined as:

[16 + (# of taps/2)]/FS_IN

Therefore the worst group delay difference between two AD1896s is simply:

[2^16*[1/(Ratio_True - 2) - 1/(Ratio_True + 2)]]/FS_IN

For Example: FS_IN = 192 kHz, FS_OUT = 32 kHz

Ratio_True = 341
Ratio1 = 343
Ratio2 = 339

[2^16*[1/339 - 1/343]]/192000 = 11.7 microseconds

**Above comments are from Kevin McLaughlin at Analog Devices 03/14/2001, 03/19/2001.**

### Up-Conversion – Delay Matching Criteria:

When up-converting, two AD1896 SRC devices will exhibit identical delays if **both** of the following are true:

- Both devices have identical input and output frequencies.
- Neither device has operated in a down-convert mode since the last reset.

### Down-Conversion – Delay Matching Criteria:

When down-converting, two AD1896 SRC devices will exhibit identical delays if **all** of the following are true:

- The “phase mode” is used.
- Input clocks are common to all SRCs.
- Output clocks are common to all SRCs.

Note that the “phase mode” only works when **both** the input and output clocks are common across all SRC devices.

### *SRC Delay Error Calculations (AD1896):*

Maximum Delay Error – Up-Conversion – Board to Board – 48 kHz Mode:

Maximum error between boards referenced to a common 48 kHz signal after one or more board has received a reference frequency of 47 kHz or less:

| Fs_IN | Fs_OUT |
|---|---|
| 46,875 | 48,000 |

| RATIO | RATIO_AVG | RATIO_MIN | RATIO_MAX |
|---|---|---|---|
| 2047 | 2047 | 2045 | 2047 |

| TAPS_AVG | TAPS_MIN | TAPS_MAX | TAP_DIFF |
|---|---|---|---|
| 64 | 64.06256109 | 64 | 0.062622264 |

| DELAY_AVG | DELAY_MIN | DELAY_MAX | DELAY_DIFF |
|---|---|---|---|
| 1.02E-03 | 1.02E-03 | 1.02E-03 | 6.67E-07 |

| PHASE@20 kHz |
|---|
| 4.8 |

Maximum Delay Error – Down-Conversion – Board to Board – 48 kHz Mode:

Maximum error when operating in a down-convert mode:

| Fs_IN | Fs_OUT |
|---|---|
| 46,875 | 44,100 |

| RATIO | RATIO_AVG | RATIO_MIN | RATIO_MAX |
|---|---|---|---|
| 1925.818 | 1925 | 1923 | 1927 |

| TAPS_AVG | TAPS_MIN | TAPS_MAX | TAP_DIFF |
|---|---|---|---|
| 68.05399792 | 68.12474012 | 67.98340249 | 0.141484518 |

| DELAY_AVG | DELAY_MIN | DELAY_MAX | DELAY_DIFF |
|---|---|---|---|
| 1.07E-03 | 1.07E-03 | 1.07E-03 | 1.51E-06 |

| PHASE@20 kHz |
|---|
| 10.9 |

## Maximum Delay Error – Up-Conversion – Board to Board – 96 kHz Mode:

Maximum error between boards referenced to a common 48 kHz signal after one or more board has received a reference frequency of 47 kHz or less:

| Fs_IN | Fs_OUT |
|---|---|
| 93,750 | 96,000 |

| RATIO | RATIO_AVG | RATIO_MIN | RATIO_MAX |
|---|---|---|---|
| 2047 | 2047 | 2045 | 2047 |

| TAPS_AVG | TAPS_MIN | TAPS_MAX | TAP_DIFF |
|---|---|---|---|
| 64 | 64.06256109 | 64 | 0.062622264 |

| DELAY_AVG | DELAY_MIN | DELAY_MAX | DELAY_DIFF |
|---|---|---|---|
| 5.12E-04 | 5.12E-04 | 5.12E-04 | 3.34E-07 |

| PHASE@20 kHz |
|---|
| 2.4 |

## Maximum Delay Error – Down-Conversion – Board to Board – 96 kHz Mode:

Maximum error when operating in a down-convert mode:

| Fs_IN | Fs_OUT |
|---|---|
| 93,750 | 88,200 |

| RATIO | RATIO_AVG | RATIO_MIN | RATIO_MAX |
|---|---|---|---|
| 1925.818 | 1925 | 1923 | 1927 |

| TAPS_AVG | TAPS_MIN | TAPS_MAX | TAP_DIFF |
|---|---|---|---|
| 68.05399792 | 68.12474012 | 67.98340249 | 0.141484518 |

| DELAY_AVG | DELAY_MIN | DELAY_MAX | DELAY_DIFF |
|---|---|---|---|
| 5.34E-04 | 5.34E-04 | 5.33E-04 | 7.54E-07 |

| PHASE@20 kHz |
|---|
| 5.4 |

### *SRC Mode Pins –SRC 1 and SRC 2*:

GRPDLYS – **OPEN** (HIGH – USING INTERNAL PULL-UP) – SHORT GROUP DELAY
BYPASS – **LOW** - SRC ENABLED
SMODE_IN_0 – **HIGH** – I2S
SMODE_IN_1 – **LOW** – I2S
SMODE_IN_2 – **LOW** – I2S
WLNGTH_OUT_0 – Default = **LOW** = 24-BITS (Jumper Selected)
WLNGTH_OUT_1 – Default = **LOW** = 24-BITS (Jumper Selected)
SMODE_OUT_0 – **HIGH** – I2S
SMODE_OUT_1 – **LOW** – I2S

### *SRC Mode Pins –SRC 1*:

MSMODE_0 – **LOW** – SLAVE
MSMODE_1 – **LOW** – SLAVE
MSMODE_2 – **LOW** – SLAVE

### *SRC Mode Pins –SRC 2*:

MSMODE_0 – **LOW** – MATCHED PHASE MODE
MSMODE_1 – **LOW** – MATCHED PHASE MODE
MSMODE_2 – **HIGH** – MATCHED PHASE MODE

### *SRC Clock and Data Pins – SRC 1:*

SCLK_I – **INPUT** – From ADC 1
LRCK_I – **INPUT** – From ADC 1
SDATA_I – **INPUT** – From ADC 1
SCLK_O – **INPUT** – From REC
LRCK_O – **INPUT** – From REC
SDATA_O – **OUTPUT** – To XMIT “SDTI 1” and SRC 2 “TDM_IN”
TDM_IN – **INPUT** – Tie to GND
MCLK_I – **INPUT** – 24.576 MHz (Fixed Frequency) – From Crystal Oscillator 2

### *SRC Clock and Data Pins – SRC 2:*

SCLK_I – **INPUT** – From ADC 1
LRCK_I – **INPUT** – From ADC 1
SDATA_I – **INPUT** – From ADC 2
SCLK_O – **INPUT** – From REC
LRCK_O – **INPUT** – From REC
SDATA_O – **OUTPUT** – To XMIT “SDTI 2”
TDM_IN – **INPUT** – From SRC 1 “SDATA_O” – Provides Phase-Mode Data to SRC 2
MCLK_I – **INPUT** – 24.576 MHz (Fixed Frequency) – From Crystal Oscillator 2

### *Unused Pins – SRC 1 and 2:*

MCLK_O – **OUTPUT** – No Connection

### *SRC Mute Pins:*

MUTE_I on SRC 1 must be connected to MUTE_O on SRC 1 – no other connection necessary
MUTE_I on SRC 2 must be connected to MUTE_O on SRC 2 – no other connection necessary

### *SRC Reset Pin:*

/RESET – **INPUT** – **LOW** = RESET, **HIGH** = RUN – From System Reset Controller

## Analog to Digital Converters (AK5393):

The AK5393 converters operate at a fixed sample frequency of 46.875 kHz or 93.75 kHz. The sample clock is supplied by a 12 MHz crystal oscillator, and is internally divided by either 128 or 256. Over sampling ratio is 128 Fs at 46.875 kHz and 64 Fs at 93.75 kHz. Output mode is I2S. ADC 1 is master and provides the clocks for the I2S interfaces on both ADCs as well as the input ports on both SRCs. The AK5393 has a 5V core.

Note: AK5394 converters could be substituted for slightly higher performance at a higher system cost. The first silicon AK5394 converters have high THD. AKM has assured us that this will be fixed Q2 or Q3 2001. Until then, the AK5394 offers the best performance available. The PCB shall accept either ADC device.

### *ADC Mode Pins – ADC 1 (MASTER):*

ZCAL – **LOW** – CALIBRATE FROM INTERNAL REFERENCE VOLTAGES
SMODE1 – **HIGH** – I2S MASTER MODE
SMODE2 – **HIGH** – I2S MASTER MODE
DFS (DFS0) – **LOW** = 256X (48 kHz), **HIGH** = 128X (96 kHz) – Controlled by "48/96" Jumper
TEST (DFS1) – **LOW** – NORMAL OPERATION (48 kHz or 96 kHz)
HPFE – **HIGH** – HIGH PASS FILTER ENABLED

### *ADC Mode Pins – ADC 2 (SLAVE):*

ZCAL – **LOW** – CALIBRATE FROM INTERNAL REFERENCE VOLTAGES
SMODE1 – **LOW** – I2S SLAVE MODE
SMODE2 – **HIGH** – I2S SLAVE MODE
DFS (DFS0) – **LOW** = 256X (48 kHz), **HIGH** = 128X (96 kHz) – Controlled by "48/96" Jumper
TEST (DFS1) – **LOW** – NORMAL OPERATION (48 kHz or 96 kHz)
HPFE – **HIGH** – HIGH PASS FILTER ENABLED

### *ADC Clock and Data Pins – ADC 1:*

SCLK – **OUTPUT** – To ADC 2, SRC 1 and SRC 2
LRCK – **OUTPUT** – To ADC 2, SRC 1 and SRC 2
FSYNC – **OUTPUT** – No Connection
SDATA – **OUTPUT** – To SRC 1
MCLK – **INPUT** – 12.000 MHz (Fixed Frequency) – From Crystal Oscillator #1

### *ADC Clock and Data Pins – ADC 2:*

SCLK – **INPUT** – From ADC 1
LRCK – **INPUT** – From ADC 1
FSYNC – **INPUT** – Connect to GND
SDATA – **OUTPUT** – To SRC 1
MCLK – **INPUT** – 12.000 MHz (Fixed Frequency) – From Crystal Oscillator #1

### *Unused Pins – ADC 1 and 2:*

CAL – **OUTPUT** – No Connection

### *ADC Reset Pin:*

/RST – **INPUT** – **LOW** = RESET, **HIGH** = RUN – From System Reset Controller

### *ADC Group Delay:*

| Fs | Digital Group Delay (uS) | Analog Group Delay (uS) | Total Delay (uS) |
|---|---|---|---|
| 46875 | 870.4 | 3.9 | 874.3 |
| 93750 | 435.2 | 3.9 | 439.1 |

## Analog Input Stage:

- -6 dB balanced receiver
- High and Low Frequency Common Mode Trim
- Variable Gain Stage
- Summing Amp
- Balanced ADC Drivers

## Digital Audio Transmitter:

### *Digital Audio Transmitter (AK4102) – Preferred Solution:*

The AK4102 is a 4-channel digital audio transmitter. It has two balanced RS422 outputs.

The AK4102 would operate in I2S slave mode, receive clock signals from the AES Receiver, and data from SRC 1 and SRC 2.

The AK4102 defaults to consumer mode, and cannot be operated in pro mode without using the serial control port. The internal RS422 outputs have 42-ohm impedances, and therefor cannot drive multiple outputs.

One AK4102 device and 7 balanced RS422 buffers will be required.

### *Digital Audio Transmitter (CS8403) – Alternate Solution #1:*

The CS8403 is a 2-channel digital audio transmitter. It has one balanced RS422 output. This output is low impedance and is capable of driving two digital AES/EBU loads.

The CS8403 operates in I2S slave mode, receives clock signals from the AES Receiver, and data from SRC 1 and SRC 2. The CS8403 can be strapped for either professional or consumer modes.

Two CS8403 devices and 7 balanced RS422 buffers will be required.

Sample rate will only be indicated in 48 kHz applications, and may be incorrect if frequencies other than 48 kHz are applied to the reference input while in 48 kHz mode.

### *Digital Audio Transmitter (AK4101) – Alternate Solution #2:*

The AK4101 is an 8-channel digital audio transmitter. It has four balanced RS422 outputs.

The AK4101 would operate in I2S slave mode, receive clock signals from the AES Receiver, and data from SRC 1 and SRC 2.

The AK4101 defaults to consumer mode, and cannot be operated in pro mode without using the serial control port. The internal RS422 outputs have 56-ohm impedances, and therefor cannot drive multiple outputs.

Two AK4101 devices could be used to directly drive all 7 of the digital outputs. As an alternative, one AK4101 device could drive 7 balanced RS422 drivers.

### *Digital Audio Transmitter (AK4103) – Alternate Solution #3:*

The AK4103 is a 2-channel digital audio transmitter. It has one balanced RS422 output.

The AK4103 would operate in I2S slave mode, receive clock signals from the AES Receiver, and data from SRC 1 and SRC 2.

The AK4103 defaults to consumer mode, and cannot be operated in pro mode without using the serial control port. The internal RS422 outputs have 54-ohm impedances, and therefor cannot drive multiple outputs.

Two AK4103 devices and 7 balanced RS422 buffers will be required.

## Digital Audio Transmitter (AK4102):

The AK4102 will be operated in the "asynchronous" (microprocessor controlled) mode. A 4-wire interface will be used to establish communications between the AK4102 and an FPGA controller. The FPGA will set the status mode to "professional", and will set the sample rate status bits to reflect the actual measured sample rate of the digital outputs.

### *AK4102 - Data Interface Pins:*

"BICK" – Input – From ADC1 "SCLK" – 64 Fs data clock from ADC1
"LRCK" – Input – From ADC1 "LRCK" – I2S Frame Clock from ADC1
"SDTI-1" – Input – From ADC1 "SDATA" – CH12 Data – From ADC1
"SDTI-2" – Input – From ADC2 "SDATA" – CH34 Data – From ADC2
"C1" – Input – Tie LOW, or tie to FPGA output pin
"C2" – Input – Tie LOW, or tie to FPGA output pin
"U1" – Input – Tie LOW, or tie to FPGA output pin
"U2" – Input – Tie LOW, or tie to FPGA output pin

### *AK4102 – RS422 Transmit Pins:*

TXP1 – Output – To RS422 Buffer #1 – CH12 AES/EBU +Output
TXN1 – Outputs – To RS422 Buffer #1 – CH12 AES/EBU –Output
TXP2 – Output – To RS422 Buffer #2 – CH34 AES/EBU +Output
TXN2 – Outputs – To RS422 Buffer #2 – CH34 AES/EBU -Output

### *AK4102 – Master Clock Pins:*

"CKS0" – Input – Tie LOW
"CKS1" – Input – HIGH = 48 kHz, LOW = 96 kHz – Controlled by fallback jumper
"MCLK" – Input – From REC "MCLK01" – 512 Fs in "48 kHz mode", 256 Fs in "96 kHz mode"
"BLS" – Output – No Connection – Block Start Flag

### *AK4102 - Control Pins:*

"TRANS" – Input – Tie LOW – Disables "Transparent Mode"
"RESETN" – Input – Tie to RESET bus
"FS0/**CSN**" – Input – From FPGA – Low to enable control interface
"FS1/**CDTI**" – Input – From FPGA – Control Data In
"FS2/**CCLK**" – Input – From FPGA – Control Data Clock
"FS3/**CDTO**" – Tristate Output – To FPGA with pull-up resistor – Control Data Out
"ASN" – Input – Tie LOW – Low to enable microprocessor interface mode
"DIF0" – Input – Tie HIGH – High to enable I2S
"DIF1" – Input – Tie LOW – Low to enable I2S
"DIF2" – Input – Tie HIGH – High to enable I2S

### *AK4102 - Power Pins:*

"DVDD" – Power (+5 V)
"DVSS" – Ground

### *Fs Frequency Counter/Encoder for use with AK4101, AK4102, or AK4103 Transmitters:*

A frequency counter/encoder circuit will be required to encode frequency information onto the channel status bits. If this circuit is omitted, frequency status information could be set by the "48/96" jumper. Please note that if the frequency information were derived from the jumper, the status bits would indicate the fallback frequency and would not change if other frequencies were applied to the external digital audio reference.

| **Reference Frequency 24576000** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Fs** | **22050** | **24000** | **32000** | **44100** | **48000** | **88200** | **96000** | **176400** | **192000** |
| **Exact Ratio** | 1115 | 1024 | 768 | 557.3 | 512 | 278.6 | 256 | 139.32 | 128 |
| **Min Threshold** | 1113 | 1022 | 766 | 555 | 510 | 277 | 254 | 137 | 126 |
| **Max Threshold** | 1117 | 1026 | 770 | 559 | 514 | 281 | 258 | 141 | 130 |
| **Freq at Min Threshold** | 22081 | 24047 | 32084 | 44281 | 48188 | 88722 | 96756 | 179387 | 195048 |
| **Freq at Max Threshold** | 22002 | 23953 | 31917 | 43964 | 47813 | 87459 | 95256 | 174298 | 189046 |
| **Pro. Mode - FS[3:0]** | **1001** | **1101** | **0011** | **0001** | **0010** | **1010** | **1110** | **1011** | **1100** |
| **Con. Mode - FS[3:0]** | 0000 | 0000 | 0011 | 0000 | 0010 | 0000 | 0000 | 0000 | 0000 |

### *Serial Interface Controller for AK4101, AK4102, and AK4103 Transmitters:*

The AK4101, Ak4102, and AK4103 transmitters default to consumer status mode and cannot be placed in professional mode without the use of the serial control interface. A microprocessor or FPGA will be required to configure these devices. An FPGA will be used in this design.

## RS422-Compatible Output Buffers (using SN74AC11240 drivers):

Two SN74AC11240 bus driver ICs will be used to provide 7 balanced digital audio outputs. The SN74AC11240 bus drivers have output impedances of 6 to 12 ohms (typically 10 ohms). This output impedance is fairly constant as the outputs are pulled from –1 V to (Vcc+1V). Also, the impedance of the complimentary output divers are well matched to each other. Use the following chart to select resistor values:

| DRIVER OUTPUT VOLTAGE | DRIVER OUTPUT IMPEDANCE | NUMBER OF DRIVERS | DESIRED OUTPUT IMPEDANCE | DESIRED OUTPUT VOLTAGE | SELECTED Rs | CALCULATED Rp | CALCULATED OUTPUT VOLTAGE | SELECTED Rp |
|---|---|---|---|---|---|---|---|---|
| 5 | 10 | 2 | 110 | 4 | 109.8 | 721.1 | 4.2 | 723 |
| 5 | 10 | 2 | 75 | 1 | 357 | 93.6 | 1.0 | 93.1 |
| 8 | 110 | 1 | 75 | 1 | 191 | 99.9 | 1.0 | 100 |
| 5 | 68.5 | 2 | 110 | 4 | 0 | 558.1 | 4.0 | 558 |

## FPGA:

Xilinx FGPA - part number: XCS05XL-4VQ100C
VCC = 3.3 V
5V tolerant I/O
360 flip-flops
77 User I/O pins
100-pin VQ package
Requires Xilinx XC17S05XL Configuration ROM

### *FPGA Minimum I/O Pin Set:*

A minimum of 14 I/O pins will be required:

Input Pins:

- RESET
- Master Clock
- LRCK
- BICK
- D12IN
- D34IN
- 48/96
- 96 Detect
- CDTO

Output Pins:

- 4 Status LEDs
- 8 Meter LEDs
- CSN
- CDTI
- CCLK

Bi-directional Pins:

None

### *FPGA Maximum I/O Pin Set:*

The following pin set will provide greater system flexibility. Many functions are controlled by the FPGA:

Input Pins:

- RESET
- Master Clock
- LRCK
- BICK
- D12IN
- D34IN
- 48/96
- 96 Detect
- CDTO
- RECV
- 4 OPTION JUMPERS

Output Pins:

- 4 Status LEDs
- 8 Meter LEDs
- CSN
- CDTI
- CCLK
- C1
- C2
- U1
- U2
- OCKS1
- D12OUT
- D34OUT

Bi-directional Pins:

None

## System Reset:

Reset line is common to the following:

- AK4112 Digital Audio Receiver
- AD1896 Sample Rate Converters
- AK5393 Analog to Digital Converters
- AK4102 Digital Audio Transmitter
- FPGA
- FPGA Serial ROM

Reset is active low (LOW = RESET).

### *Minimum Reset Time:*

Reset pulse must exceed the following:

- AK4112 = 150 ns
- AD1896 = 200 ns
- AK5393 = 150 ns, reset completed after 8960 samples (203 msec)
- AK4102 = 150 ns
- 3.3V Regulator Rise Time = ??

### *Reset Threshold Voltage:*

- The reset circuit shall measure the +5V supply.
- The threshold shall be high enough to assure that 3.3 V regulator has enough headroom.
- The threshold must be less than the minimum normal output level from the DC to DC converter. (5V +/- 5%).

### *Selected Device:*

National **LM809-4.38**
Threshold is 4.38V
Reset Pulse Width = 240 ms

## System Group Delay:

ADC Fs = 46.875 kHz, crystal frequency = 24 MHz, Output Fs = 48 kHz.

| ADC Fs | ADC (uS) | SRC (uS) | XMIT Fs | XMIT (uS) ** | TOTAL DELAY |
|---|---|---|---|---|---|
| 46875 | 874 | 1000 | 48000 | 100 | 1974.3 |
| 93750 | 439 | 533 | 96000 | 100 | 1072.1 |

** Transmitter delay is unknown. Estimated transmitter delay is less than 5 Fs cycles or <100uS.
Total system delay is approximately 2 msec at Fs(out) = 48000.

# USER INTERFACE:

## *CONTROLS:*

- One 10-turn trimmer per Analog Input (4 total)
- Trim Range: +10 dBu to +30 dBu at FSD0
- Extender card may be required for adjustment.

## *DISPLAYS:*

"+22V" – Green LED
"-22V" – Green LED
"+5V" – Green LED
"+3.3" – Green LED
"LOCK" – Green LED
"REC ERROR" – Red LED
"88-96" – Green LED
"RANGE ERROR" – Red LED
"CH1 SIG" – Green LED
"CH1 CLIP" – Red LED
"CH2 SIG" – Green LED
"CH2 CLIP" – Red LED
"CH3 SIG" – Green LED
"CH3 CLIP" – Red LED
"CH4 SIG" – Green LED
"CH4 CLIP" – Red LED

## *Monitor Outputs:*

Two fixed-gain stereo headphone jacks located on front panel (if layout permits).

## *TEST POINTS:*

One unbalanced test point per channel.
Test point shall be post gain control.
Test point shall consist of large vias at front edge of PCB (if layout permits).
Vias shall be sized and located to provide convenient clip points for a scope probe.
One ground tab shall be provided on front edge of PCB (to attach scope ground clip).

## *REMOTE CONTROL:*

None

# JUMPERS:

### *Master/Slave Jumper:*

One 3-pin header sets direction of digital audio reference port:
- Slave *** – Lock to Reference Input
- Master – Reference pin is an output and is driven from CH 12

| **Slave ***** | | **Master** | |
|---|---|---|---|
| **S** | **M** | **S** | **M** |
| **1 2** | **3** | **1** | **2 3** |

### *Fallback Jumpers:*

One 8-pin header sets fallback frequency to:
- 48 kHz fallback ***
- 96 kHz fallback
- 44.1 kHz fallback (requires optional crystal oscillator)
- 88.2 kHz fallback (requires optional crystal oscillator)

| | |
|---|---|
| 44.1 | 1 2 |
| 48 | 3 4 |
| 88.2 | 5 6 |
| 96 | 7 8 |

### *Digital-Output Impedance-Jumpers:*

One 4-pin header per digital output, allows selection of:
- 75 Ohm Output Impedance ***
- 110 Ohm Output Impedance

| **75 Ohms ***** | | **110 Ohms** | |
|---|---|---|---|
| 75 | **1 2** | 75 | **1 2** |
| 110 | **3 4** | 110 | **3 4** |

### *Analog Input Impedance Jumpers:*

One 2-pin header per analog input, allows selection of:
- High-Z Input Impedance ***
- 600-Ohm input Impedance

| **High-Z ***** | | **600 Ohms** | |
|---|---|---|---|
| 600 | **1 2** | 600 | **1 2** |

### *FPGA Option Jumpers:*

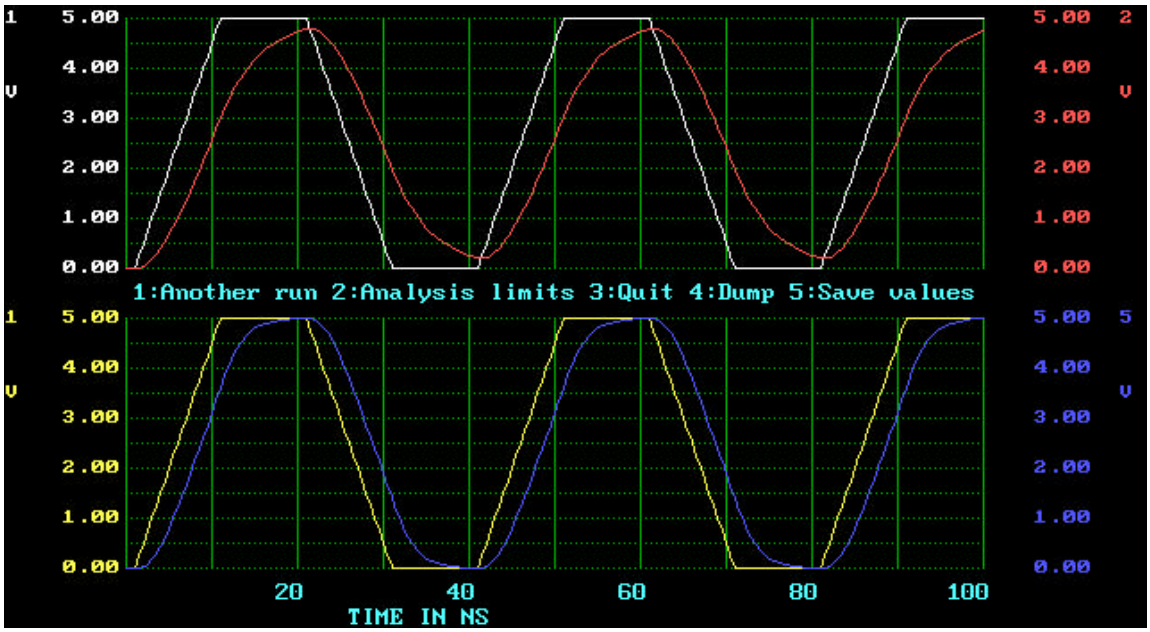
One 8-pin header reserved for software-controlled options:

| | |
|---|---|
| A | 1 2 |
| B | 3 4 |
| C | 5 6 |
| D | 7 8 |

*** FACTORY DEFAULTS

## CLOCK DISTRIBUTION:

The 24 MHz ADC clock signal must be buffered. Clock must drive four 20pF loads. Trace shows the output of the oscillator with no load. Trace 2 shows the effect of an 80pF load connected directly to the oscillator. Trace 5 shows the result of using three 10pF buffers connected directly to the oscillator, with each driving a 20 pF load. Note the improvement in rise time, wave shape, and amplitude.



## PCB STRIPLINE FOR CLOCK DISTRIBUTION:

The output impedance of the HC04 inverters is approximately 56 Ohms. Clocks shall be distributed via source terminated transmission lines, where the source termination is provided by the HC04 driver impedance.

| | | |
|---|---|---|
| PCB DIELECTRIC CONSTANT = | 5 | |

**Double Sided - Signal on one side, ground on the other side:**

| | | |
|---|---|---|
| MICROSTRIP WIDTH = | 85 | units |
| MICROSTRIP THICKNESS = | 2 | units |
| DISTANCE ABOVE GROUND PLANE = | 60 | units |
| MICROSTRIP IMPEDANCE = | 56.16 | Ohms |
| MICROSTRIP PROPAGATION DELAY = | 1.77 | ns/foot |

**4-Layer - Signal on Layer 1, Ground on Layer 2:**

| | | |
|---|---|---|
| MICROSTRIP WIDTH = | 18 | units |
| MICROSTRIP THICKNESS = | 2 | units |
| DISTANCE ABOVE GROUND PLANE = | 14 | units |
| MICROSTRIP IMPEDANCE = | 56.02 | Ohms |
| MICROSTRIP PROPAGATION DELAY = | 1.77 | ns/foot |

**4-Layer - Ground on Layers 1 and 4 - Signal on layer 2 or 3:**

| | | |
|---|---|---|
| STRIPLINE WIDTH = | 10 | units |
| STRIPLINE THICKNESS = | 1 | units |
| DISTANCE BETWEEN GROUND PLANES = | 60 | units |
| DISTANCE BETWEEN GROUND PLANES AND STRIPLINE = | 14 | units |
| STRIPLINE IMPEDANCE = | 56.75 | Ohms |
| STRIPLINE PROPAGATION DELAY = | 2.27 | ns/foot |

**4-Layer - Ground on Layers 1 and 3 - Signal on layer 2:**

| | | |
|---|---|---|
| STRIPLINE WIDTH = | 9 | units |
| STRIPLINE THICKNESS = | 1 | units |
| DISTANCE BETWEEN GROUND PLANES = | 45 | units |
| DISTANCE BETWEEN GROUND PLANES AND STRIPLINE = | 14 | units |
| STRIPLINE IMPEDANCE = | 56.41 | Ohms |
| STRIPLINE PROPAGATION DELAY = | 2.27 | ns/foot |

## Software Features:

Serial Control Interface – controls transmitter status bits.
Frequency Counter – measures output Fs and sets transmitter status bits.
4-Channel 2-Segment Digital Audio Meter – 2 LEDs per channel
Clock divide-by-two
Clock buffer

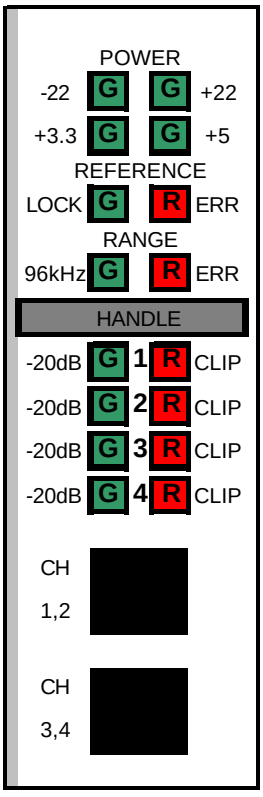
## Options:

None

## Front Panel Layout:

Top to bottom:

- Power Supply LEDs (4 - Green) – On when supplies are working.
- Lock LED (Green) – On when locked to an external reference.
- Reference Error LED (Red) – On when reference is faulty or absent.
- Range LED (Green) – On when 96 kHz fallback is selected.
- Range Error LED (Red) – On when reference is out of range.
- Channel 1 “-20dB” LED (Green) – On when channel 1 exceeds -20 dBFS.
- Channel 1 “CLIP” LED (Red) – On when channel 1 exceeds 0 dBFS.
- Channel 2 “-20dB” LED (Green) – On when channel 2 exceeds -20 dBFS.
- Channel 2 “CLIP” LED (Red) – On when channel 2 exceeds 0 dBFS.
- Headphone Jacks (2) – Stereo analog audio outputs – pre-conversion.




Front Panel Layout (not to scale)