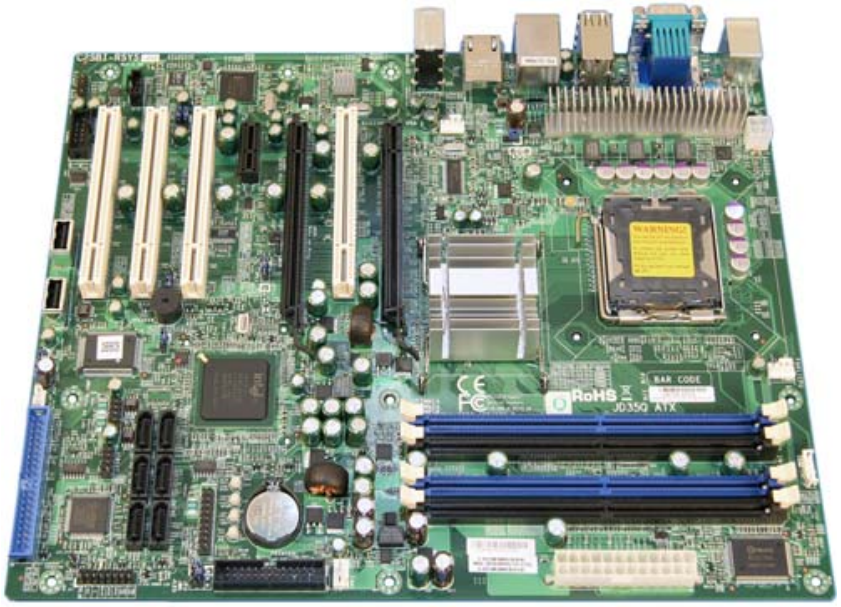
PROCELERANT™

ENDURA Q35 MOTHERBOARDS

PRODUCT MANUAL

QZ35Q
JD35Q



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Release history

Release	Date	Description
-0000	December 2007	First release.
-0001	May 2008	Second release. Updated to address issues discovered in first release.
-0002	May 2008	Third release. Correction: RAID is supported by SATA controller, not IDE.

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PREFACE

About this manual

This manual is written for engineers and technicians who will integrate the Procelerant™ Endura Q35 motherboards into their own products. For instructions on setting up an Endura Q35 motherboard, refer to the *Procelerant Endura Q35 Motherboard Quick Start Guide* available on the RadiSys® Web site, www.radisys.com.

Safety notices

Electrostatic discharge

WARNING! This product contains static-sensitive components and should be handled with care. Failure to employ adequate anti-static measures can cause irreparable damage to components.

To avoid electrostatic discharge (ESD) damage, the following precautions are strongly recommended.

- Keep each module/PCB in its ESD shielding bag until you are ready to install it.
- Before touching a module, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the module only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold modules only by their edges and mounting hardware. Avoid touching PCB components and connector pins.

For further information on ESD, visit www.esda.org.

Lithium cell battery

WARNING!

- When replacing the battery on the motherboard, use only lithium cell battery type CR2032. Using any other battery may damage the board.
- Do not use a conductive instrument to remove the battery.
- Dispose of the spent battery promptly. Do not recharge, disassemble, or incinerate the battery.
- Keep the battery away from children.

Where to get more product information

For additional product information, visit the motherboard product pages on the RadiSys Web site at www.radisys.com for access to datasheets, product documentation, BIOS releases, and drivers.

PRODUCT OVERVIEW 1

The Procelerant Endura Q35 ATX and microATX motherboards are designed for use in a variety of commercial products, such as medical imaging, gaming, test and measurement, industrial automation, and transaction terminals. All Endura Q35 motherboard models are RoHS compliant and Energy Star compliant.

Major features of the Q35 ATX motherboards include:

- Integrated Intel Graphics Memory Accelerator (GMA) 3100 graphics controller
- Dual PCI Express x16 graphics slots that can support PCI Express graphics acceleration cards, one slot is electrically x16 and the other electrically x4
- Media expansion card support
- PCI Express x4 interface for high-bandwidth data-capture devices
- Single- or dual-Gigabit Ethernet for high-bandwidth data communications

Product codes

Table 1. Endura Q35 product codes

Product code	ICH chipset	Gigabit Ethernet	Onboard video	GPIO and watchdog timer	I/O shield
JD1G03-0-0	ICH9DO	1	VGA	No	IOSHLD-JQ
JD2G03-0-0	ICH9DO	2	VGA	Yes	IOSHLD-JQ
QZ1G03-0-0	ICH9DO	1	VGA	No	IOSHLD-JQ
QZ2G03-0-0	ICH9DO	2	VGA	Yes	IOSHLD-JQ

Note: Processors and memory modules are not included with product codes ending in -0-0.

Board layout

Figure 1. JD35Q and QZ35Q board layout: rear I/O panel

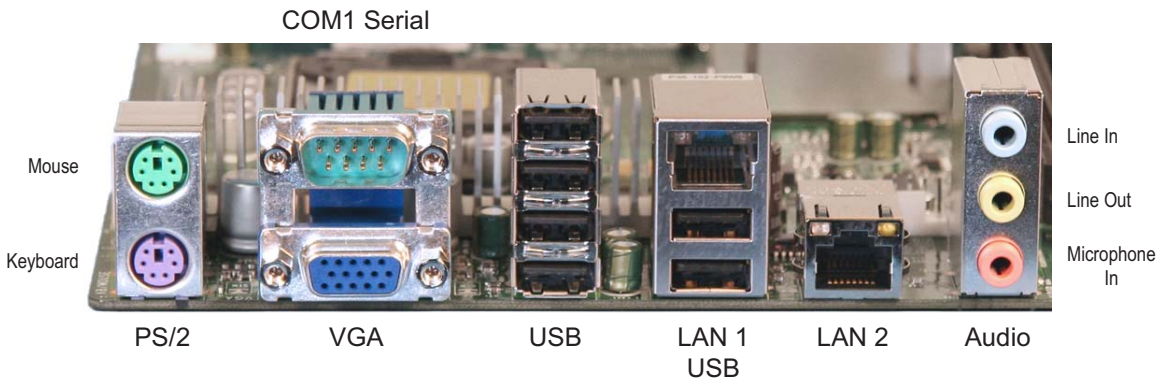


Figure 2. JD35Q board layout: top view

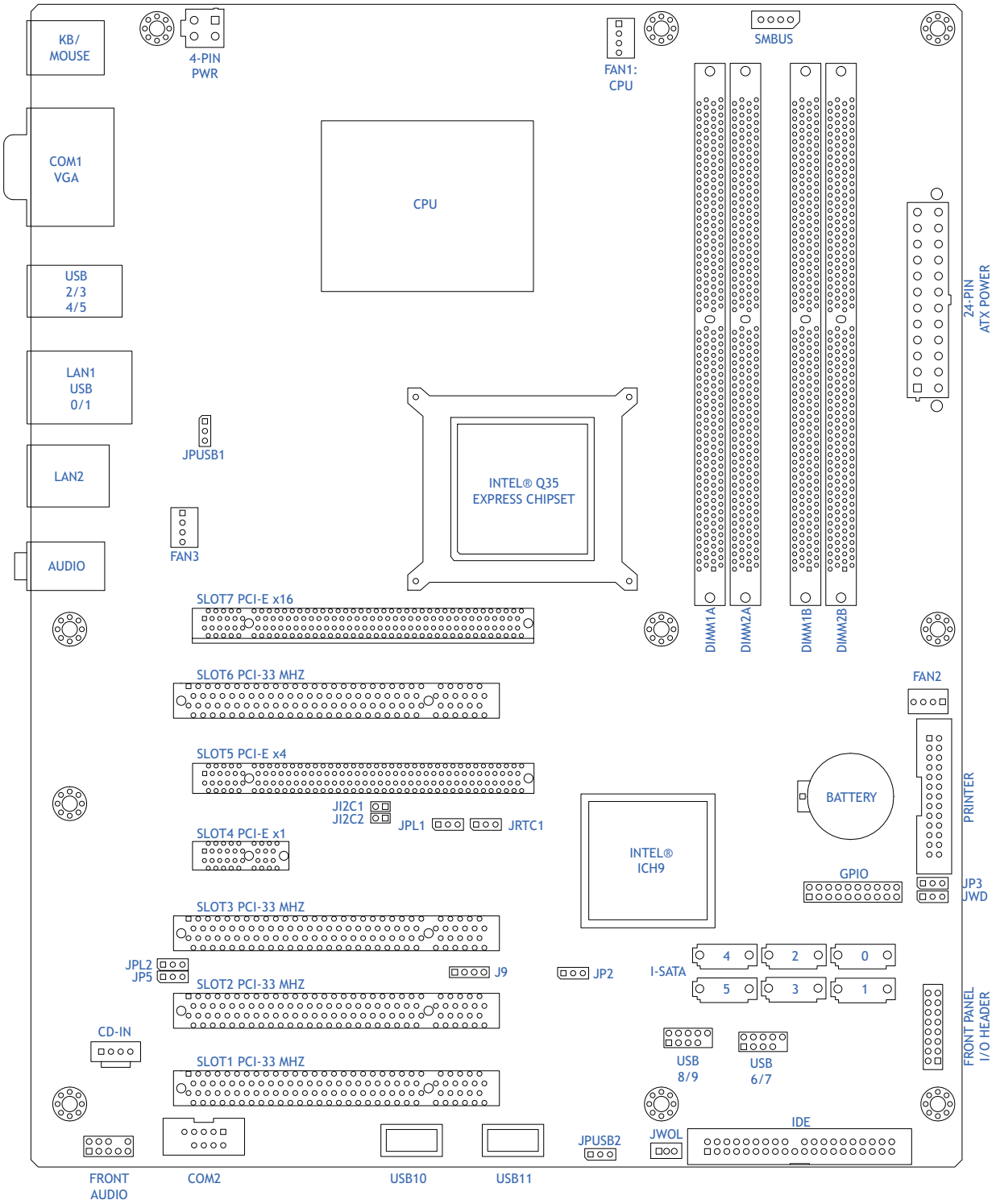
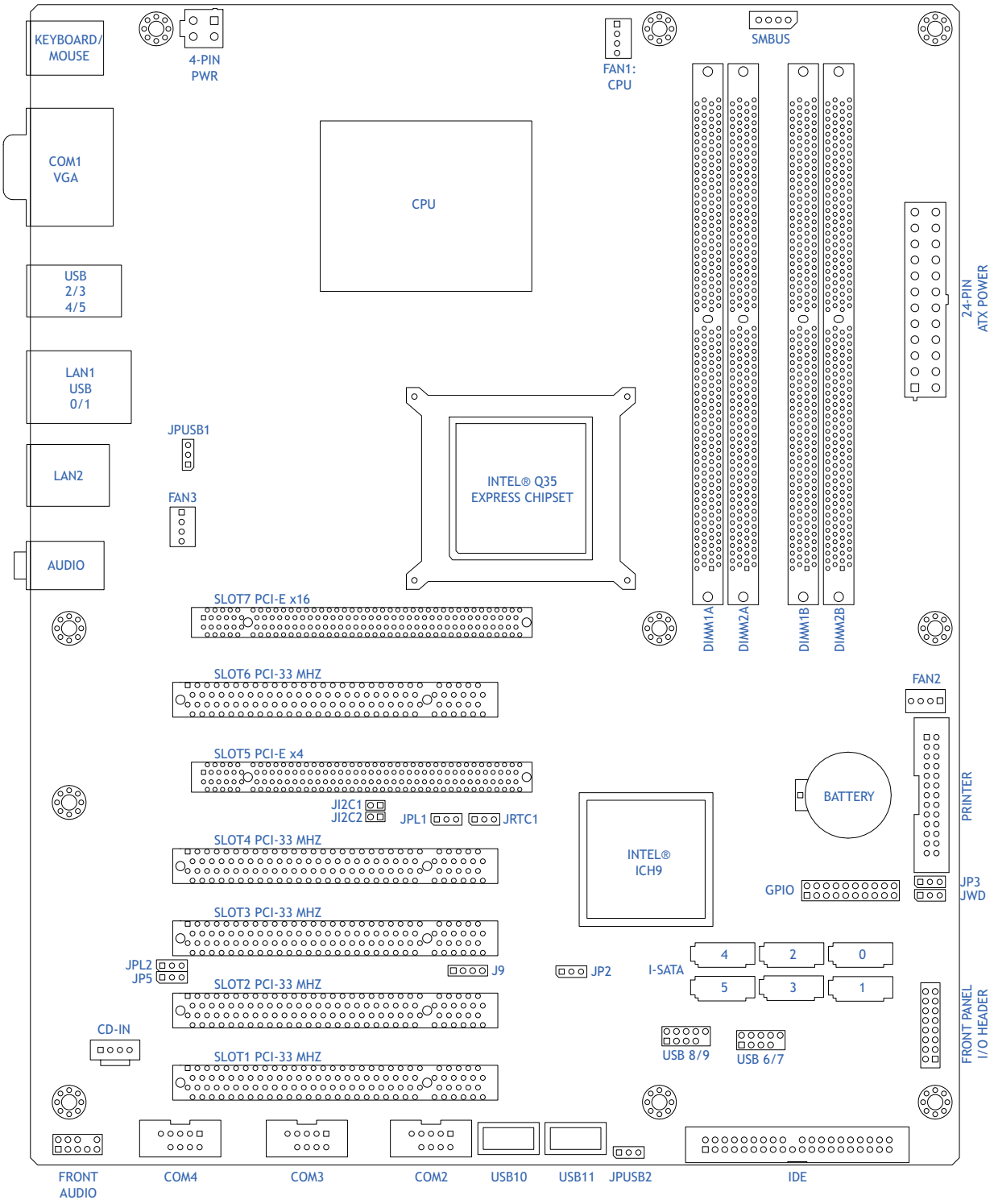


Figure 3. QZ35Q board layout: top view



Mechanical specifications

Motherboard

Figure 4. JD35Q board dimensions

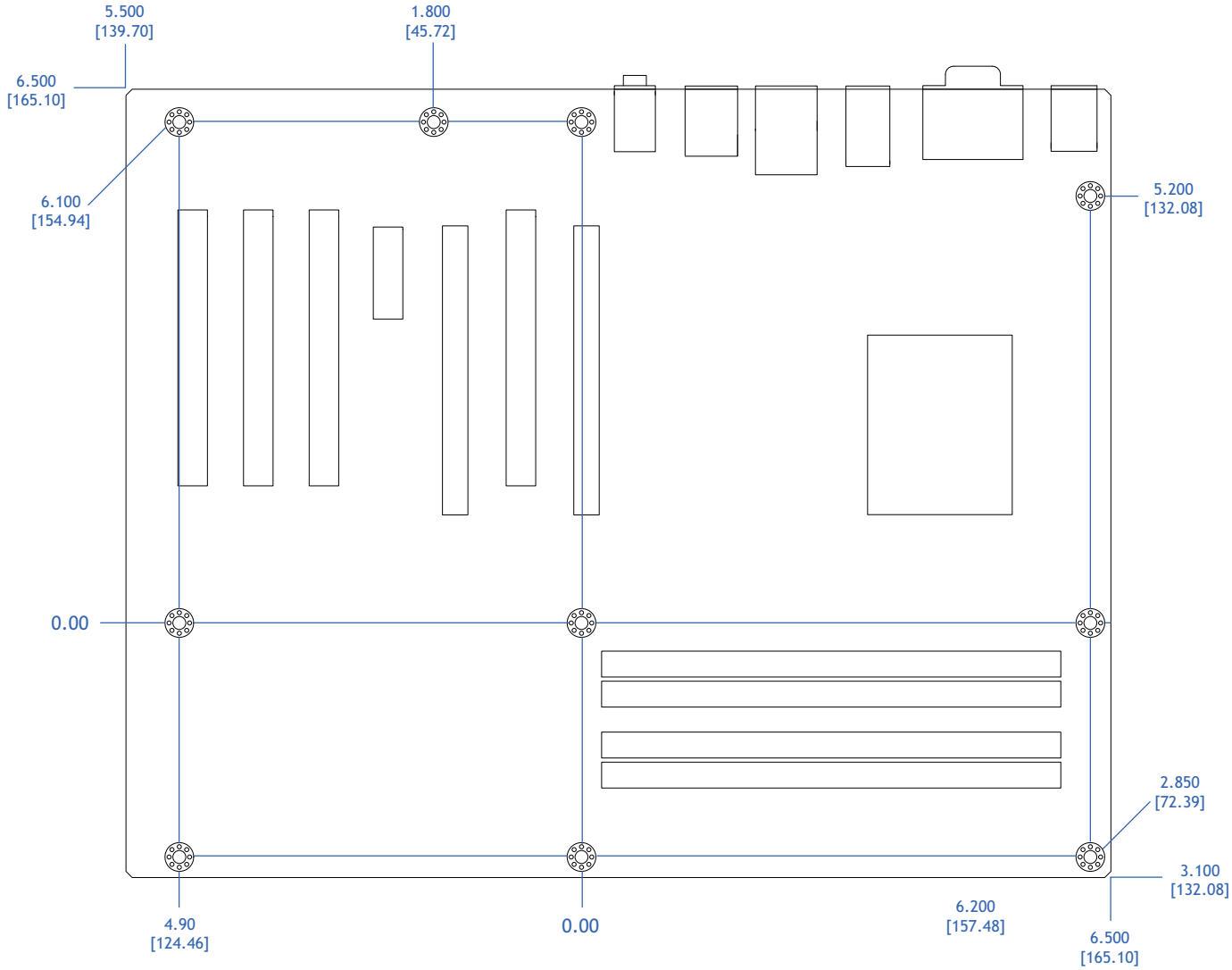
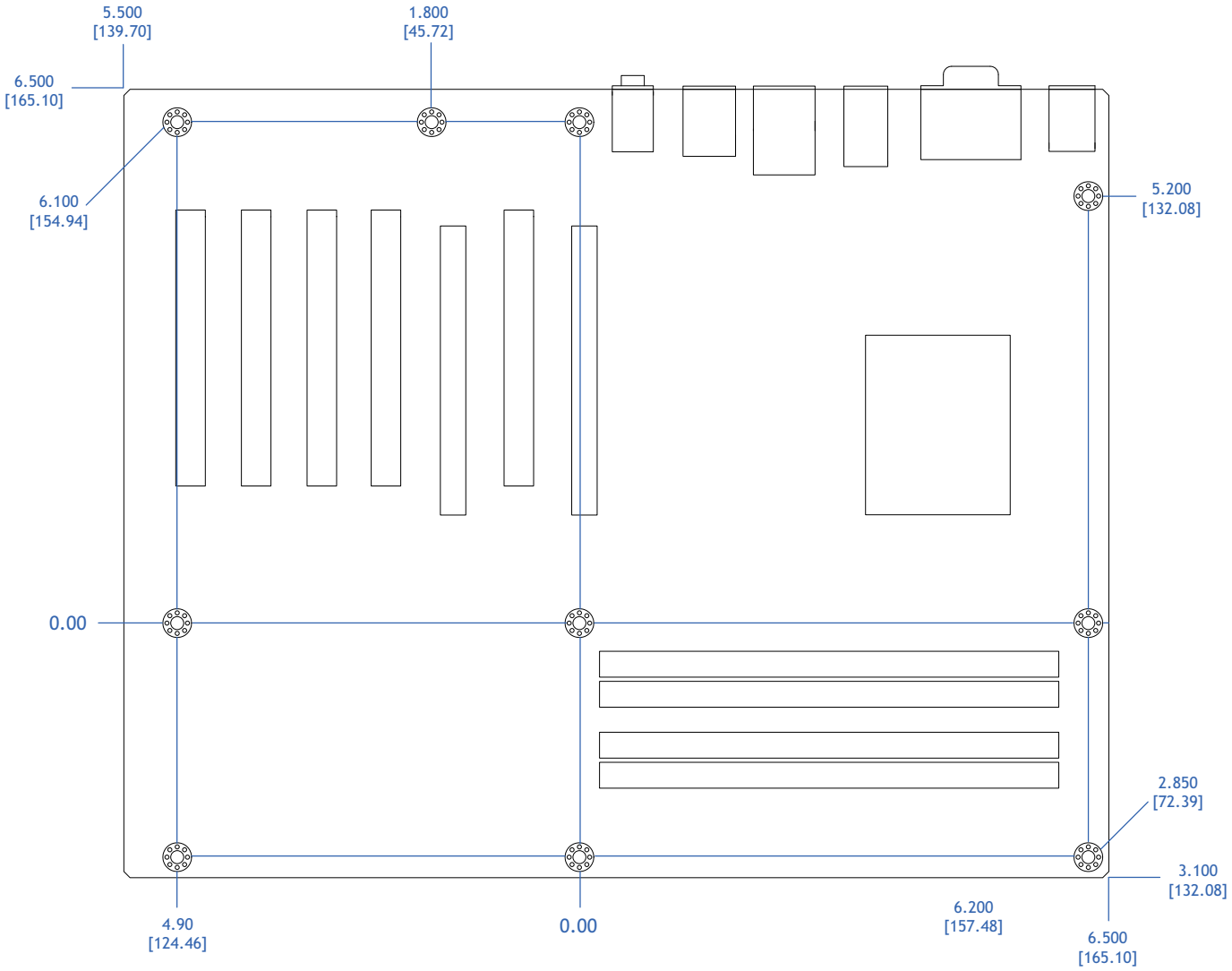
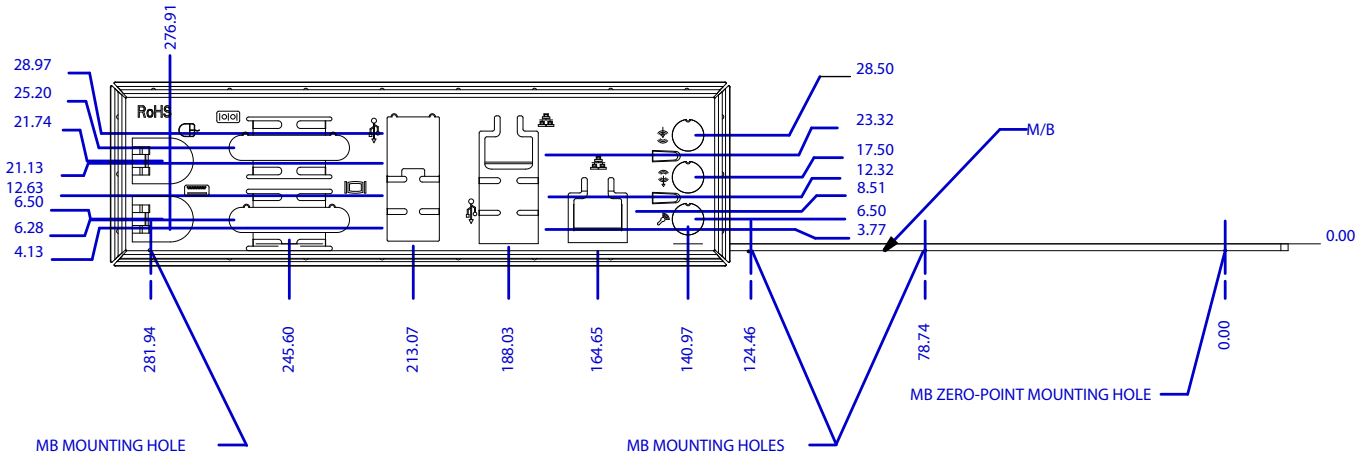


Figure 5. QZ35Q board dimensions



I/O shield

Figure 6. I/O shield for JD35Q and QZ35Q motherboards



Thermal specifications

When designing a custom thermal solution, it is helpful to know the Q35 motherboard thermal requirements, such as the thermal design power (TDP) of the processor (see *Processor* on page 34).

It is recommended that you perform thermal tests under the maximum ambient temperature, 55°C. Suitable airflow is required to maintain an ambient temperature that does not exceed the maximum thermal performance for each processor and its thermal solution.

WARNING! Always test the final system configuration to ensure the ambient temperature does not exceed the maximum. Failure to do so can lead to unstable operation, motherboard or processor damage, and shortened life.

Electrical specifications

Motherboard power consumption

The Q35 motherboards support soft-switched and hard-switched ATX power supplies via a standard 24-pin ATX power connector for main power supplies, and an extra 4-pin 12V ATX power connector for CPU use. For information about power supply selections, see *General specifications* on page 27.

Power consumption is highly dependent on the processor, memory, devices attached, running software, and the power state that the motherboard is in. Based on measurements of a real system, the following examples show the power requirements to expect under select conditions. They should not be interpreted as maximum requirements.

Test configuration

Component	Description
CPU	Code name: E6400 Part #: HH80557PH0462M Speed: 2.13 GHz FSB: 1066 MHz Quantity: 1
Memory	Manufacturer: ATP Part #: AJ28K72G8BHE7S Type: ECC Speed: DDR2-800 Quantity: 1 Size: 1GB
Power supply	Manufacturer: Ablecom Model: SP423-1S, Rev 3.1 Max Power: 420 W Max Current: +3.3V: 20A +5V: 30A +12V: 15A -12V: 1A +5V Standby: 2A Max allowable DC voltage drop: 2% Max allowable leakage: 0.3V Stress software: Intel/AMD CPU Maxpower, Memtest for Windows
Operating System	Microsoft® Windows® XP

JD35Q motherboard power consumption

These tests were run on a revision 1.00 JD35Q motherboard.

Table 2. JD35Q power consumption – DOS (stable)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	48
Voltage (V)	118.70	12.22		12.22	11.93	5.12	3.36	5.08	5.13	12.22	
Current (A)	0.63	1.86		0.30	0.05	1.06	2.64	0.11	0.40	0.31	Efficiency (%)
Power (W)	74.78	22.73	0.00	3.67	0.60	5.43	8.87	0.56	2.05	3.79	64
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	PASS	PASS	PASS	

Table 3. JD35Q power consumption – BIOS (stable)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	47
Voltage (V)	118.80	12.21		12.22	11.92	5.12	3.36	5.08	5.13	12.22	
Current (A)	0.62	1.87		0.34	0.01	0.95	2.41	0.11	0.41	0.31	Efficiency (%)
Power (W)	73.66	22.83	0.00	4.15	0.12	4.86	8.10	0.56	2.10	3.79	63
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	PASS	PASS	PASS	

Table 4. JD35Q power consumption – Windows desktop idle (stable)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	44
Voltage (V)	118.90	12.22		12.22	11.93	5.12	3.36	5.08	5.13	12.23	
Current (A)	0.60	1.69		0.27	0.04	0.97	2.56	0.13	0.41	0.30	Efficiency (%)
Power (W)	71.34	20.65	0.00	3.30	0.48	4.97	8.60	0.66	2.10	3.67	62
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	PASS	PASS	PASS	

Table 5. JD35Q power consumption – CPU stress (max)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	65
Voltage (V)	118.80	12.19		12.20	11.93	5.12	3.36	5.08	5.12	12.21	
Current (A)	0.79	3.45		0.24	0.03	0.98	2.57	0.08	0.41	0.29	Efficiency (%)
Power (W)	93.85	42.06	0.00	2.93	0.36	5.02	8.64	0.41	2.10	3.54	69
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	PASS	PASS	PASS	

Table 6. JD35Q power consumption – Windows stress (max)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	50
Voltage (V)	118.90	12.21		12.22	11.93	5.12	3.36	5.08	5.13	12.22	
Current (A)	0.66	2.04		0.31	0.01	1.10	2.73	0.11	0.47	0.30	Efficiency (%)
Power (W)	78.47	24.91	0.00	3.79	0.12	5.63	9.17	0.56	2.41	3.67	64
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	PASS	PASS	PASS	

JD35Q motherboard power leakage

These tests were run on a revision 1.00 JD35Q motherboard.

Table 7. JD35Q power leakage – Suspend (S3) with LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.40	0.00		0.00	0.00	0.01	0.05	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.00	0.01	0.35	0.00	0.00	Efficiency (%)
Power (W)	7.16	0.00	0.00	0.00	0.00	0.00	0.00	1.78	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 8. JD35Q power leakage – Suspend (S3) without LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.30	0.00		0.00	0.00	0.01	0.05	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.01	0.01	0.31	0.01	0.00	Efficiency (%)
Power (W)	7.16	0.00	0.00	0.00	0.00	0.00	0.00	1.57	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 9. JD35Q power leakage – Hibernate (S4) with LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	1
Voltage (V)	119.50	0.00		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.00	0.00	0.28	0.00	0.00	Efficiency (%)
Power (W)	7.17	0.00	0.00	0.00	0.00	0.00	0.00	1.42	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 10. JD35Q power leakage – Hibernate (S4) without LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	1
Voltage (V)	119.60	0.00		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.03		0.00	0.00	0.01	0.00	0.22	0.01	0.00	Efficiency (%)
Power (W)	7.18	0.00	0.00	0.00	0.00	0.00	0.00	1.12	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 11. JD35Q power leakage – Soft Off (S5) with LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.50	0.00		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.00	0.00	0.32	0.01	0.00	Efficiency (%)
Power (W)	7.17	0.00	0.00	0.00	0.00	0.00	0.00	1.63	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 12. JD35Q power leakage – Soft Off (S5) without LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.40	0.00		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.00	0.00	0.34	0.00	0.00	Efficiency (%)
Power (W)	7.16	0.00	0.00	0.00	0.00	0.00	0.00	1.73	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

QZ35Q motherboard power consumption

These tests were run on a revision 1.01 QZ35Q motherboard.

Table 13. QZ35Q power consumption – DOS (stable)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	46
Voltage (V)	119.00	12.21		12.22	11.92	5.12	3.36	5.08	5.13	12.22	
Current (A)	0.63	1.84		0.30	0.04	1.06	2.41	0.09	0.37	0.29	Efficiency (%)
Power (W)	74.97	22.47	0.00	3.67	0.48	5.43	8.10	0.46	1.90	3.54	61

Table 14. QZ35Q power consumption – BIOS (stable)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	46
Voltage (V)	119.30	12.22		12.22	11.92	5.12	3.36	5.08	5.12	12.23	
Current (A)	0.63	1.82		0.29	0.03	1.00	2.45	0.10	0.43	0.33	Efficiency (%)
Power (W)	75.16	22.24	0.00	3.54	0.36	5.12	8.23	0.51	2.20	4.04	62

Table 15. QZ35Q power consumption – Windows desktop idle (stable)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	44
Voltage (V)	119.20	12.22		12.22	11.92	5.12	3.36	5.08	5.13	12.23	
Current (A)	0.61	1.71		0.29	0.04	0.95	2.38	0.09	0.41	0.29	Efficiency (%)
Power (W)	72.71	20.90	0.00	3.54	0.48	4.86	8.00	0.46	2.10	3.55	60

Table 16. QZ35Q power consumption – CPU stress (max)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	66
Voltage (V)	119.00	12.19		12.20	11.92	5.12	3.36	5.08	5.13	12.21	
Current (A)	0.81	3.50		0.28	0.04	0.95	2.41	0.09	0.42	0.29	Efficiency (%)
Power (W)	96.39	42.67	0.00	3.42	0.48	4.86	8.10	0.46	2.15	3.54	68

Table 17. QZ35Q power consumption – Windows stress (max)

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	49
Voltage (V)	119.10	12.21		12.21	11.92	5.12	3.36	5.08	5.13	12.22	
Current (A)	0.65	2.06		0.26	0.03	1.05	2.49	0.08	0.49	0.33	Efficiency (%)
Power (W)	77.42	25.15	0.00	3.17	0.36	5.38	8.37	0.41	2.51	4.03	64

QZ35Q motherboard power leakage

These tests were run on a revision 1.01 QZ35Q motherboard.

Table 18. QZ35Q power leakage – Suspend (S3) with LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.80	0.00		0.00	0.00	0.01	0.06	5.07	0.01	0.00	
Current (A)	0.07	0.00		0.00	0.00	0.01	0.01	0.38	0.00	0.00	Efficiency (%)
Power (W)	8.39	0.00	0.00	0.00	0.00	0.00	0.00	1.93	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 19. QZ35Q power leakage – Suspend (S3) without LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.20	0.00		0.00	0.00	0.01	0.06	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.01	0.07	0.34	0.03	0.00	Efficiency (%)
Power (W)	7.15	0.00	0.00	0.00	0.00	0.00	0.00	1.73	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 20. QZ35Q power leakage – Hibernate (S4) with LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	1
Voltage (V)	119.80	0.00		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.02	0.00	0.28	0.02	0.00	Efficiency (%)
Power (W)	7.19	0.00	0.00	0.00	0.00	0.00	0.00	1.42	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 21. QZ35Q power leakage – Hibernate (S4) without LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	1
Voltage (V)	119.20	0.00		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.00		0.00	0.00	0.00	0.00	0.22	0.00	0.00	Efficiency (%)
Power (W)	7.15	0.00	0.00	0.00	0.00	0.00	0.00	1.12	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 22. QZ35Q power leakage – Soft Off (S5) with LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.10	0.00		0.00	0.00	0.01	0.00	5.07	0.01	0.00	
Current (A)	0.07	0.00		0.00	0.00	0.01	0.00	0.34	0.01	0.00	Efficiency (%)
Power (W)	8.34	0.00	0.00	0.00	0.00	0.00	0.00	1.72	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Table 23. QZ35Q power leakage – Soft Off (S5) without LAN connected

	AC Input	4-pin	8-pin	20/24-pin main power connector					Peripheral (HDD)		Consumption (W)
		+12V	+12V	+12V	-12V	+5V	+3.3V	$+5V_{STBY}$	+5V	+12V	2
Voltage (V)	119.40	0.01		0.00	0.00	0.01	0.00	5.08	0.01	0.00	
Current (A)	0.06	0.02		0.00	0.00	0.01	0.00	0.35	0.02	0.00	Efficiency (%)
Power (W)	7.16	0.00	0.00	0.00	0.00	0.00	0.00	1.78	0.00	0.00	–
Vdrop Result	–	PASS		PASS	PASS	PASS	PASS	–	PASS	PASS	

Power delivery to expansion slots

The following tables indicate the maximum current that should be drawn from each expansion slot. PCI Express slots are limited to 75W in total on the main +12V and +3.3V supplies, all of which can be drawn from either voltage rail. The total for the riser are for the total current/power delivered to the riser through the motherboard. If more is required, the riser must draw power from an additional source such as a separate power connector from the PSU.

WARNING! Do not exceed the limits for each slot or voltage rail shown in these tables.

Table 24. Maximum expansion slot currents on Qz35Q

Expansion slot	+3.3V (A)	+5V (A)	+12V (A)	-12V (A)	+5V standby (A)
PCI Express x16 graphics slot	3	–	5.5	–	–
PCI Express x4 graphics interface (x16 physically)	3	–	2.1	–	–
PCI slot	7.6	5	0.5	0.1	–

Table 25. Maximum expansion slot currents on JD35Q

Expansion slot	+3.3V (A)	+5V (A)	+12V (A)	-12V (A)	+5V standby (A)
PCI Express x16 graphics slot	3	–	5.5	–	–
PCI Express x4 graphics interface (x16 physically)	3	–	2.1	–	–
PCI Express x1 slot	3	–	0.5	0.1	–
PCI slot	7.6	5	0.5	–	–

Power budget

Before choosing a power supply, it is recommended that you always create a power budget for your system. A sample power budget for the Q35 motherboards populated with processor, memory, expansion cards, etc. are shown below.

Note: These sample values may not apply to your system.

Table 26. Power budget for JD35Q

Component	Motherboard current					Power consumption
	+3.3V	+5V	+12V	-12V	+5V standby	
Motherboard	2.6A	1.0A	3.7A	0.03A	0.1A	59W
12 USB ports	–	6A	–	–	–	30W
6 SATA ports	–	2.5A	1.9A	–	–	35.3W
2 serial ports	–	0.02A	0.02A	–	–	0.3W
1 IDE connector	–	1.5A	1.5A	–	–	25.5W
Expansion slots (total)	13.6A	5A	8.1A	0.1A	–	168.3W
Heatsink	–	–	0.4A	–	–	4.8W
Front panel I/O	0.1A	–	–	–	–	0.3W
Video DDC channel	–	0.05A	–	–	–	0.3W
GPIO header	–	0.1A	–	–	–	0.5W
Total	16.32A	16.17A	15.62A	0.13A	0.1A	325W

Table 27. Power budget for QZ35Q

Component	Motherboard current					Power consumption
	+3.3V	+5V	+12V	-12V	+5V standby	
Motherboard	2.6A	1.0A	3.7A	0.03A	0.1A	59W
12 USB ports	–	6A	–	–	–	30W
6 SATA ports	–	2.5A	1.9A	–	–	35.3W
4 serial ports	–	0.04A	0.02A	–	–	0.6W
1 IDE connector	–	1.5A	1.5A	–	–	25.5W
Expansion slots (total)	16.6A	5A	8.6A	0.1A	–	184.2W
Heatsink	–	–	0.4A	–	–	4.8W
Front panel I/O	0.1A	–	–	–	–	0.3W
Video DDC channel	–	0.05A	–	–	–	0.3W
GPIO header	–	0.1A	–	–	–	0.5W
Total	19.32A	16.19A	16.14A	0.13A	0.1A	341W

General Purpose I/O Lines

Table 28. General Purpose I/O lines

Parameter	Conditions	Min	Max
Input High Voltage (V_{IH})	-	2.0V	3.6V
Input Low Voltage (V_{IL})	-	-0.5V	0.8V
Input Leakage Current (I_{IL})	V_{IN} = 3.6V, V_{CC} = max	-	5uA
	V_{IN} = 0V, V_{CC} = max	-	-5uA
Output High Voltage (V_{OH})	I_{OH} = 4mA	Vcc3.3 - 0.5V	-
Output Low Voltage (V_{OL})	I_{OL} = 8mA	-	0.4V

Environmental specifications

All Q35 motherboards comply with the following environmental specifications.

Table 29. Environmental specifications

Characteristic	State	Value
Temperature (ambient)	Operating	0º to +55º C Operation above +30º C reduces the maximum operational relative humidity
	Operating gradient	±5°C per minute
	Non-operating	-40º C to +85º C, 5º C per minute maximum excursion gradient
Relative humidity	Operating	15% to 95% RH non-condensing
	Non-operating	15% to 90% RH non-condensing at +40°C
Vibration	Operating	0.25 G at 5 to 200 Hz. Approx. 15 min./axis.
	Non-operating	0.5 G at 5 to 200 Hz. Approx. 15 min./axis.
Shock	Non-operating	30g 11ms, half-sine, 3 axes
	Packaged	Drop test, 10-up bulk packaging, 30 inches free-fall, 152 inches/s velocity change.
Altitude	Operating	To 15,000 ft. (4,500m)
	Non-operating	To 40,000 ft. (12,000m)
MTBF		See *MTBF reliability predictions* on page 26.
Airflow		Based on standard Intel guidelines
Fuses		Self-resetting PTC fuse

Compliance

EMC compliance

When correctly installed in a suitable chassis, Q35 motherboards meet these EMC regulations.

Table 30. EMC compliance

Characteristic[1]	State	Value
ESD	Operating	IEC 1000-4-2/EN61000-4-2 ▪ 4kV direct contact, performance criteria B ▪ 6kV direct contact, performance criteria C ▪ 4kV air discharge, performance criteria B ▪ 8kV air discharge, performance criteria C
Fast transient/burst	Operating	IEC 1000-4-4/EN61000-4-4, performance criteria B
Surge voltages	Operating	IEC 1000-4-5/EN61000-4-5, performance criteria B
Conducted	Operating	IEC 1000-4-6/EN61000-4-6, performance criteria B
Radiated emissions	Operating	▪ CISPR 22 Class B ▪ EN55022, EN55024 ▪ FCC Class B
Radiated immunity	Operating	EN61000-4-3, performance criteria A
Conducted immunity	Operating	EN61000-4-6, performance criteria A
AC power dips and interrupts	Operating	EN61000-4-11, performance criteria B and C

[1] These are system-level tests. Because the Q35 motherboard is part of a larger system, radiated emissions and immunity are agency tested, but not certified, to these specifications. Other aspects of system performance will affect this motherboard's ability to conform to these specifications.

Safety compliance

When correctly installed in a suitable chassis, Q35 motherboards are designed to meet these safety regulations:

- UL60950, CSA60950, EN60950 and IEC60950
- CB report to IEC60950-1
- Accessory listing from UL to UL60950-1

Environmental compliance

- European RoHS
- China RoHS
- Designed for lead-free manufacturing processes

Industry compliance

Q35 motherboards are designed to the industry standards shown in *Appendix C, "Industry Standard References"* on page 93.

MTBF reliability predictions

The predicted MTBF for Q35 motherboards at 35ºC and 55ºC are shown in Table 31. The predictions are based on Telcordia SR-332 Issue 1, Method 1, Case 3 with the following underlying assumptions:

- 50% default stress ratio for all modeled components
- Application-specific stress ratios applied for electrolytic capacitors when available
- Ground benign in a controlled environment
- Level II quality grade on all components
- Mechanical components are not modeled
- No burn-in or pre-testing specified
- MTTR specified to be 30 minutes
- No component-specific thermal rises or other voltage/current stress applied
- Relex 7.7 modeling software

Table 31. MTBF reliability predictions

Product code	MTBF (hours) @ 35ºC	MTBF (hours) @ 55ºC
QZ1G03-0-0	227,995	119,501
QZ2G03-0-0	215,186	112,787
JD1G03-0-0	230,652	120,894
JD2G03-0-0	228,924	119,988

General specifications

JD35Q motherboards

Table 32. General specifications: JD35Q

Item		Description
Physical	Dimensions	12" x 9.6"
	Form Factor	ATX revision 2.2
Processor	–	▪ These processors are supported: ▪ Intel Core 2 Duo E8400 ▪ Intel Core 2 Duo E6400 ▪ Intel Core 2 Duo E4300 ▪ Intel Pentium Dual-Core E2160 ▪ Intel Celeron 440 ▪ Intel Core 2 Quad processors (future) ▪ FSB frequency at 800/1066/1333 MHz ▪ LGA775 socket
Chipset	–	Intel Q35 Express GMCH chipset and ICH9DO chipset
Memory	Type	Four 240-pin DIMM slots for single or dual channel non-ECC unbuffered DDR2 667/800 MHz memory
	Capacity	Maximum 8GB, minimum 256MB
Video	–	▪ VGA output for analog display, with a maximum VGA resolution of 2048x1536 with 32-bit color at 75Hz ▪ One PCI Express x16 graphics slot and one PCI Express x4 (x16 physically) slot for PEG graphics cards, with a maximum digital display 1920x1200@60Hz ▪ Support for dual independent displays ▪ Support for ADD2 and Media Expansion Cards
Audio	–	▪ Intel High Definition Audio using Realtek ALC883 eight channel CODEC ▪ Three audio jacks on rear I/O panel, with two hardware configuration options for two jacks (Microphone, Line Out) and three jacks (Microphone, Line Out, Line In) ▪ Audio enable header capable of enabling onboard audio connections ▪ One CD-ROM header for audio CD playback

Table 32. General specifications: JD35Q

Item		Description
Network	–	▪ Single or dual Intel Gigabit Ethernet: Intel 82566DM PHY controller for Ethernet 0 and Intel 82573L MAC/PHY controller for Ethernet port 1 ▪ Two Ethernet LEDs for Ethernet link and activity indication ▪ PXE boot and Wake-On-LAN support on either Ethernet port ▪ One or two RJ45 Ethernet connectors on rear I/O panel (note that Ethernet port 2 is automatically disabled if a PCI Express card is present in the x1 slot)
I/O	USB	▪ 12 USB 2.0 ports with a speed of up to 480Mbps: 6 ports on the rear I/O panel, two onboard ports, and two onboard dual USB headers ▪ 13 general purpose I/O ports (model JD2G03-0-0 only)
	SATA	6 devices supported with 5 SATA ports and 1 eSATA port (identified by a blue connector)
	IDE	One Ultra ATA100 interface via PCI controller
	Serial ports	Two Fast UART 16500 compatible serial ports: one on the rear I/O panel and one onboard header
	CPLD	Watchdog timer, GPIO, and BIOS write protect (model JD2G03-0-0 only)
	Miscellaneous	▪ One onboard parallel printer port header ▪ PS/2 mouse and keyboard on rear I/O panel
Expansion capabilities	PCI Express	▪ One PCI Express x16 slot ▪ One PCI Express x4 interface (x16 slot physically) ▪ One PCI Express x1 slot, capable of switching with the Ethernet port 1 via Ethernet port 1/PCI Express x1 signal switch
	PCI	Four PCI 2.3 32-bit at 33MHz slots
BIOS		▪ 2MB Firmware SPI Phoenix® TrustedCore™ BIOS including video BIOS, network boot, and PXE ▪ Clear CMOS jumper selection header capable of restoring factory defaults ▪ Customizable logo during boot BIOS default settings
System management		▪ Voltage, temperature, and fan monitoring (3 fans) ▪ Lithium cell voltage monitoring ▪ Automatic fan speed control (3 fans) ▪ Programmable watchdog timer ▪ SMBus header ▪ Watchdog time-out for SMI interrupt and system reset
Power	Requirement	▪ Standard 24-pin ATX power supply connector and 4-pin +12V ATX power supply connector ▪ Hard-switched or soft-switched power supplies
	Management	ACPI 3.0 supporting states S0, S3, S4, S5, and C0, C1, C2, C3, C4
OS support		▪ Windows XP® Professional SP2 ▪ Windows XP® Embedded SP2 ▪ Windows Vista Premium ▪ Red-Hat® Enterprise Linux® 5.0 AS ▪ Novell SUSE Linux Enterprise Server 10 ▪ Knoppix Linux 5.1.1 ▪ Solaris 10 Update 4

QZ35Q motherboards

Table 33. General specifications: QZ35Q

Item		Description
Physical	Dimensions	12" x 9.6"
	Form Factor	ATX revision 2.2
Processor	–	▪ These processors are supported: ▪ Intel Core 2 Duo E8400 ▪ Intel Core 2 Duo E6400 ▪ Intel Core 2 Duo E4300 ▪ Intel Pentium Dual-Core E2160 ▪ Intel Celeron 440 ▪ Intel Core 2 Quad processors (future) ▪ FSB frequency at 800/1066/1333 MHz ▪ LGA775 socket
Chipset	–	Intel Q35 Express GMCH chipset and ICH9DO chipset
Memory	Type	Four 240-pin DIMM slots for single or dual channel non-ECC unbuffered DDR2 667/800 MHz memory
	Capacity	Maximum 8GB, minimum 256MB
Video	–	▪ VGA output for analog display, with a maximum VGA resolution of 2048x1536 with 32-bit color at 75Hz ▪ One PCI Express x16 graphics slot and one PCI Express x4 (x16 physically) slot for PEG graphics cards, with a maximum digital display 1920x1200@60Hz ▪ Support for dual independent displays ▪ Support for ADD2 and Media Expansion Cards
Audio	–	▪ Intel High Definition Audio using Realtek ALC883 eight channel CODEC ▪ Three audio jacks on rear I/O panel, with two hardware configuration options for two jacks (Microphone, Line Out) and three jacks (Microphone, Line Out, Line In) ▪ Audio enable header capable of enabling onboard audio connections ▪ One CD-ROM header for audio CD playback
Network	–	▪ Single or dual Intel Gigabit Ethernet: Intel 82566DM PHY controller for Ethernet 0 and Intel 82573L MAC/PHY controller for Ethernet port 1 ▪ Two Ethernet LEDs for Ethernet link and activity indication ▪ PXE boot and Wake-On-LAN support on either Ethernet port ▪ One or two RJ45 Ethernet connectors on rear I/O panel

Table 33. General specifications: QZ35Q

Item		Description
I/O	USB	▪ Support for12 USB 2.0 ports with a speed of up to 480Mbps: six ports on the rear I/O panel, two onboard ports, and two onboard dual USB headers ▪ 13 general purpose I/O lines (model QZ2G03-0-0 only)
	SATA	6 devices supported with 5 SATA ports and 1 eSATA port (identified by a blue connector)
	IDE	One Ultra ATA100 interface via PCI controller
	Serial ports	Four Fast UART 16500 compatible serial ports: one on the rear I/O panel and three onboard headers
	CPLD	Watchdog timer, GPIO, and BIOS write protect (model QZ2G03-0-0 only)
	Miscellaneous	▪ One onboard parallel printer port header ▪ PS/2 mouse and keyboard on rear I/O panel
Expansion capabilities	PCI Express	▪ One PCI Express x16 slot ▪ One PCI Express x4 interface (x16 slot physically)
	PCI	Five PCI 2.3 32-bit at 33MHz slots
BIOS		▪ 2MB Firmware SPI Phoenix® TrustedCore™ BIOS including video BIOS, network boot, and PXE ▪ Clear CMOS jumper selection header capable of restoring factory defaults ▪ Customizable logo during boot BIOS default settings
System management		▪ Voltage, temperature, and fan monitoring (3 fans) ▪ Lithium cell voltage monitoring ▪ Automatic fan speed control (3 fans) ▪ Programmable watchdog timer ▪ SMBus header ▪ Chassis intrusion detection ▪ Watchdog time-out for SMI interrupt and system reset
Power	Requirement	▪ Standard 24-pin ATX power supply connector and 4-pin +12V ATX power supply connector ▪ Hard-switched or soft-switched power supplies
	Management	ACPI 3.0 supporting states S0, S3, S4, S5, and C0, C1, C2, C3, C4
OS support		▪ Windows XP® Professional SP2 ▪ Windows XP® Embedded SP2 ▪ Windows Vista Premium ▪ Red-Hat® Enterprise Linux® 5.0 AS ▪ Novell SUSE Linux Enterprise Server 10 ▪ Knoppix Linux 5.1.1 ▪ Solaris 10 Update 4

Block diagrams

Figure 7. JD35Q block diagram

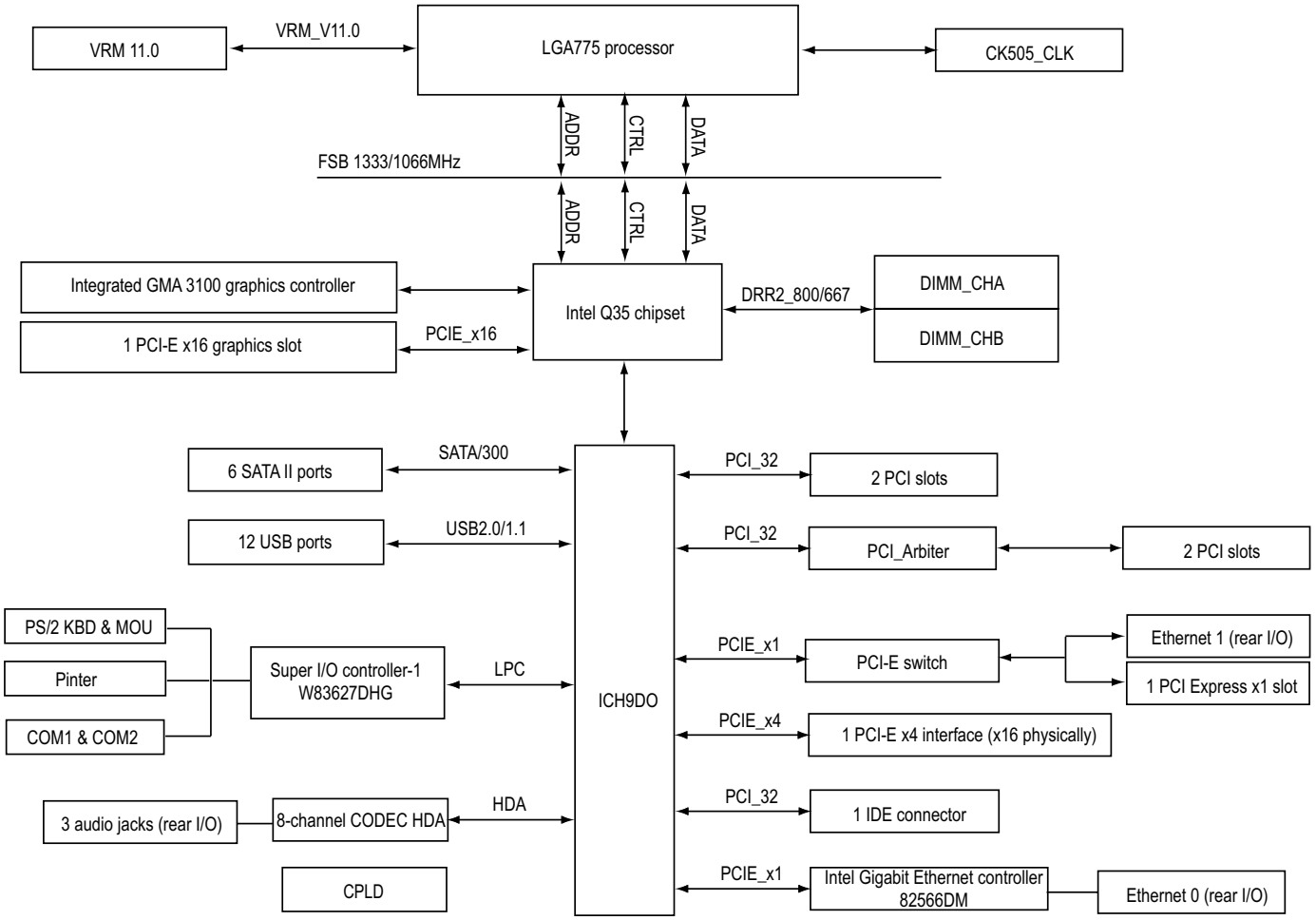
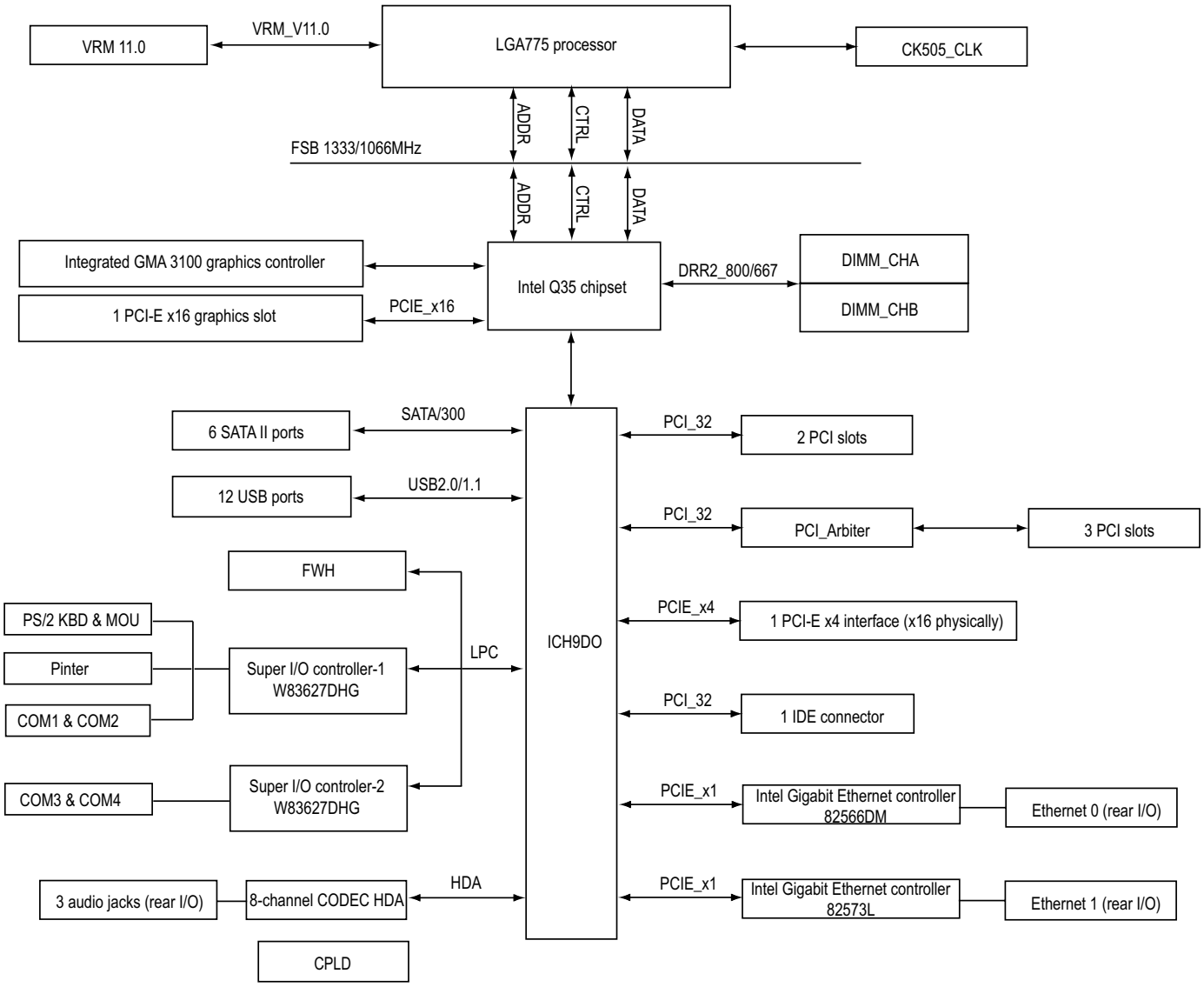


Figure 8. QZ35Q block diagram



Power supply

Q35 motherboards support soft-switched and hard-switched ATX power supplies. The standard 24-pin ATX power connector provides +12V, -12V, +5V standby, +5V, +3.3V power rails and an extra 4-pin ATX power connector provides +12V for CPU use only.

A 20-pin ATX power connector can also be used. In this case, plug the 20-pin cable in on the pin #1 side of the connector and leave the two pairs of pins on the other side exposed. No adaptor is required.

WARNING! The power supply must be approved by a third-party agency for use in IEC/EN/UL/CSA 60950 applications.

Voltage requirements

Table 34 shows the maximum load currents on all ATX power rails. Ensure that the power supply can support the required load current on all rails, otherwise, it can cause damage to the power supply or the motherboard.

A 5V standby power rail is optional, but if not provided, the soft-switched power supply control features of the motherboard cannot be used. When there is a standby rail, make sure it can provide sufficient current for the motherboard, taking into account the Ethernet controllers and any adapter card that draws current from the auxiliary 3.3V supply. The ATX -5.0V rail is not used by the Q35 motherboards.

Table 34. Maximum load currents on ATX power rails

Power Rail	Maximum Load Current
+12V	12A
-12V	0.1A
+5V	18.75A
+3.3V	6.72A
+5V standby	1.25A

Processor

Q35 motherboards support Intel Celeron, Pentium Dual-Core, and Core 2 Duo processors in a socketable LGA775 package.

For support of other processors, refer to the *Procelerant Endura Q35 Supported Processors List* on the RadiSys Web site.

Table 35. Supported processors

Processor Branding	Process	CPU#	Clock Speed MHz	FSB MHz	L2 Cache	TDP	Number of Cores
Core 2 Duo	45nm	E8400	3.0	1333	3M	65W	2
Core 2 Duo	65nm	E6400	2.13	1066	2M	65W	2
Core 2 Duo	65nm	E4300	1.80	800	2M	65W	2
Pentium Dual-Core	65nm	E2160	1.80	800	1M	65W	2
Celeron	65nm	440	2.0	800	512K	35W	1

Voltage requirements

The power supply connects to a standalone 4-pin ATX +12V power connector on the motherboard to provide power for the processor.

An onboard DC-to-DC voltage regulator generates the processor core voltages from the +12V power supply, and core PLLs and processor I/O from the +5V power rail. Both the processor voltage and the operating frequency are automatically adjusted by the motherboard to suit the installed processor.

Thermal requirements

The Intel Celeron, Pentium Dual-Core, and Core 2 Duo processors support the THERMTRIP# signal for catastrophic thermal protection. An external thermal monitor, Winbond Super IO W83627DHG (www.winbond.com/), is also implemented to protect the processor and the system against excessive temperature. If the external thermal monitor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMATRIP# signal is asserted, the voltage supply to the processor will be turned off within 500ms to prevent permanent silicon damage due to thermal runaway of the processor.

The thermal monitor feature and the Thermal Control Circuit (TCC) will be enabled in the CPU by the board BIOS. The CPU temperature can be read over the SMbus at any time.

See *Table 35* on page 34 for the thermal design power (TDP) values for each processor type, for which the junction temperature (Tj) specifications fall within 0°C — 100°C. The processor must remain within the minimum and maximum junction temperature.

Memory

Q35 motherboards have four 240-pin DIMM sockets to support up to 8GB of 64-bit, unbuffered non-ECC DDR2 800/667MHz dual-channel memory modules. Each socket can accept either single channel mode or dual-channel interleaved mode.

In general, compatible memory modules must:

- Support 512Mb and 1Gb memory technology in x8 and x16 organization.
- Supports maximum memory bandwidth of 6.4 GB/s in single channel or dual channel asymmetric mode, or 12.8 GB/s in dual channel symmetric mode assuming DDR2 800 MHz.
- Using 512 Mb device technologies, the smallest memory capacity possible is 256 MB, assuming Single Channel Mode with a single x16 single sided un-buffered non-ECC DIMM memory configuration.
- Using 1 Gb device technologies, the largest memory capacity possible is 8 GB, assuming Dual Channel Mode with four x8 double sided un-buffered non-ECC DIMM memory configuration.

The BIOS automatically configures the motherboard for the correct size, speed, and type. For a list of qualified memory modules, refer to the *Procelerant Endura Q35 Qualified Memory List* on the RadiSys Web site.

Chipset

Graphics and Memory Controller Hub

The Intel 82Q35 graphics and memory controller hub (GMCH) includes four interfaces:

- Host interface
- System memory interface
- External graphics interface
- I/O controller through DMI interface

For further information, refer to the *Intel 3 Series Express Chipset Family Datasheet for the Intel 82Q35 Graphics and Memory*.

I/O Controller Hub

The Intel ICH9 and ICH9DO I/O provide extensive I/O support:

- Direct Media Interface (DMI) support for chip-to-chip connection between the GMCH and ICH
- PCI Express Base Specification, Revision 1.1 support
- PCI Local Bus Specification, Revision 2.3 support for 33 MHz PCI operations
- ACPI Power Management Logic Revision 3.0b support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation up to six ports and AHCI support
- USB host interface with support for up to 12 USB ports, 6 UHCI host controllers, and 2 EHCI high-speed USB 2.0 host controllers
- Integrated 10/100/1000 Mbps Gigabit Ethernet MAC with system defense
- System Management Bus (SMBUs) Specification, Revision 2.0 with additional support for I2C devices
- Intel High Definition Audio support
- Intel Matrix Storage Technology support
- Intel Active Management Technology support (ICH9 Digital Office only)
- Intel Virtualization Technology for directed I/O support
- Intel Trusted Execution Technology support
- Low Pin Count (LPC) interface support
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- Intel Quiet System Technology support

For further information, refer to the *Intel 3 Series Express Chipset Family Datasheet for the Intel 82Q35 Graphics and Memory Controller Hub*.

Video

The GMCH provides an integrated graphics device (IGD) delivering cost-competitive 3D, 2D and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, 2D operations, motion compensation, overlay, and display control. The GMCH's video engines support video conferencing and other video applications.

The GMCH also has the capability to support external graphics accelerators via the PCI Express graphics (PEG) port but cannot work concurrently with the integrated graphics device. However, the dual independent display can work via the ADD2/Media Expansion Card attachment.

High bandwidth access to data is provided through the system memory port.

System memory allocation

The GMCH uses a UMA configuration with DVMT for graphics memory. When the onboard video controller is not used, it is recommended to disable it via the BIOS setup utility to prevent unnecessary system memory allocation.

By default, the system BIOS allocates 8MB of system memory to the video controller to support legacy VGA displays. The amount of system memory reported by the BIOS will reflect this reduction when the onboard video controller is enabled. Once the operating system loads, the video driver dynamically allocates further system memory depending on availability and the application requirement. Systems should have at least 256MB of system memory when using these graphics drivers.

PCI Express graphics

The Q35 motherboards support PCI Express graphics acceleration cards via the PCI Express x16 graphics slots. This support includes:

- Two PCI Express x16 graphics slots on the JD35Q motherboard, electrically x16 interface for slot 7 and electrically x4 interface for slot 5
- Two PCI Express x16 graphics slots on the QZ35Q motherboard, electrically x16 interface for slot 7 and electrically x4 interface for slot 5
- PCI Express frequency of 1.25 GHz resulting in 2.5 Gb/s each direction per lane
- Raw bit-rate of 2.5Gb/s on each lane while employing 8b/10b encoding to transmit data across the interface.
- Maximum theoretical bandwidth of 4GB/s in each direction simultaneously, for an aggregate bandwidth of 8GB/s when using 16 lanes.
- ADD2/media expansion cards support with capabilities of dual independent displays with the integrated graphics devices.

VGA

Q35 motherboards provide a standard DA15F VGA connector on the rear I/O panel. The integrated Intel GMA 3100 video controller supports:

- 350MHz integrated 24-bit RAMDAC
- Resolution up to 2048x1536 pixels at 75Hz refresh
- DDC2B Compliant Interface

Dual DVI MEC

Use this procedure to set up dual DVI monitors using a dual DVI MEC (model PLV03-0-0 only).

1. Start the system and press the Delete key when prompted to enter the BIOS setup utility.
2. In the BIOS setup, navigate to the Advanced menu, then the Advanced Chipset Control menu. Set the DVMT 4.0 Mode option to DVMT. Save this change and exit, and allow the system to restart.
3. Visit the Intel download center Web site, www.dowloadcenter.intel.com, and download the Intel Embedded Graphics Driver (IEGD) with CED, version 8.0.0. Also download and review the IEGD Release Notes.
4. ***IMPORTANT!*** Uninstall the existing graphics driver on the motherboard. (If you are running Windows, go to the Control Panel and select Add or Remove Programs.)
5. Install the IEGD according to the instructions provided in the IEGD User's Guide. This will disable the onboard video.
6. Install the dual DVI MEC in the PCI Express x16 slot. The bottom DVI port on the MEC is the primary port, and should be functional immediately.
7. Use the IEGD Configuration Editor to set up your monitors as required (Clone, Extended, etc.)

Audio

The Q35 motherboards support:

- Intel High Definition Audio using the Realtek ALC883 eight-channel stereo CODEC
- Triple 3.5mm audio jacks on the rear I/O panel for surround sound.
- One 1x4-pin CD-ROM header to support onboard sound for audio CD playback

Note: An onboard PC speaker is not provided, but it is recommended that you connect an external speaker to the front panel I/O header to hear the beep signals.

Network

The JD35Q and QZ35Q motherboards provide single or dual Gigabit Ethernet controllers as build options (see *Product codes* on page 9).

Ethernet port 0 uses the Intel 82566DM PHY controller, which connects to the ICH9/ICH9DO LAN (the MAC integrated on the ICH9/ICH9DO chipset) through a dedicated interconnect.

On motherboards with the second Ethernet port build option, Ethernet port 1 uses the Intel 82573L MAC/PHY controller, which operates its integrated Gigabit Ethernet MAC and PHY functions via the ICH9/ICH9DO's PCI Express x1 interface.

Ethernet features include:

- Standard IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T applications (802.3, 802.3u, and 802.3ab)
- Remote boot and PXE via BIOS configuration
- Wake-On-LAN support via BIOS configuration with the option to use the native operating system, as well as support for legacy operating systems
- Onboard RJ45 connector with 2 integrated programmable LEDs showing link speed and speed.

Table 36. Ethernet LEDs

LED color	LED state	Ethernet link and activity
Green/Amber	Off	10Mbps link speed
	Green steady on	100Mbps link speed
	Amber steady on	1000Mbps link speed
Yellow	Off	No link established
	Yellow steady on	Link established; communication activity not detected
	Yellow blinking	Link established; communication activity detected

I/O

Parallel ports

The Q35 motherboards support one LPT header via the Winbond W83627EHG super I/O chip. Parallel ATA features include:

- Compatible with IBM parallel port
- Supports PS/2 compatible bi-directional parallel port
- Supports Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Supports Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

SATA

The Q35 motherboards incorporate the ICH9/ICH9DO I/O controller, which provides support for both AHCI and RAID functionality on six SATA ports. BIOS options allow operation of AHCI and RAID modes. RAID 0, 1, 5, and 10 are supported. The blue SATA connector supports eSATA for use with external devices at a distance of up to 2m.

Note: SATA interface transfer rates are independent of Ultra DMA mode settings in the BIOS setup utility. SATA interface transfer rates will operate at the maximum bus speed, regardless of the Ultra DMA mode reported by the SATA device or the system BIOS.

UART

Q35 motherboards support two or four Fast UART serial ports, depending on product options, via the Winbond W83627DHG Super I/O controller(s). COM1 on the rear I/O panel has a standard DE9M connector; the other serial ports are headers for serial port connectors on the chassis.

Serial port support includes:

- High-speed, 16550-compatible UARTs with 16-byte send/receive FIFOs
- Fully programmable serial interface characteristics
- Maximum baud rate for clock source 14.769MHz is up to 921Kbps. The baud rate at 24MHz is 1.5Mbps.

IDE

The Q35 motherboards provide a standard IDE connector to support IDE hard disks and ATAPI devices via the ICH9DO's PCI controller.

USB

Q35 motherboards support 12 USB 2.0/1.1 ports at a speed of 480 Mbps:

- Six USB ports on the rear I/O panel
- Two onboard USB ports and two onboard dual USB headers.

All USB ports support high-speed, full-speed, and low-speed operations. The ICH9/ICH9DO chipset determines whether a USB port is controlled by a UHCI controller or by an EHCI controller.

The BIOS provides emulations of standard USB keyboards and mice using SMI-based routines to intercept traffic. Operating systems that do not support USB devices suffer performance degradation due to this activity. Legacy support is automatically switched off once a USB-aware operating system loads.

PS/2 mouse and keyboard

With the Winbond® W83627DHG Super I/O controller, the Q35 motherboards support the PS/2 keyboard and mouse interfaces on the rear I/O panel.

Mouse and keyboard features include:

- 8042-based keyboard controller with support for PS/2 mouse and keyboard
- Fast Gate A20 and hardware keyboard reset
- User options for the clock frequency of 6, 8, 12, and 16MHz via the BIOS setup utility configuration.

General Purpose I/O

Model JD2G03-0-0 and QZ2G03-0-0 motherboards provide 13 general-purpose pins and a PWM signal pin via a 2x10-pin GPIO header that is compliant with the *Intel General Purpose I/O Connector Specification*:

- 10 input and output lines
- 2 input-only lines
- 1 output-only line

To control these lines for your specific system applications, see *Control logic and registers* on page 75.

Super I/O

The Winbond W83627EHG Super I/O controllers is capable of supporting a wide range of I/O functions with the LPC (Low Pin Count) interface. The Q35 motherboards support the following legacy devices via this super I/O chip:

- LPT device (page 58)
- UART ports (page 40)
- PS/2 mouse and keyboard (page 41)

Note: Though the W83627EHG super I/O chip is capable of supporting 40 GPIO lines by itself, these GPIO lines are unavailable on the Q35 motherboards.

Expansion interfaces

PCI

PCI slots are compliant with the *PCI Local Bus Specification Version 2.3*. The number of PCI slots varies according to the model of Q35 motherboard.

- QZ35Q: Five 32-bit, 33MHz, 3.3V PCI slots
- JD35Q: Four 32-bit, 33MHz, 3.3V PCI slots

PCI Express

All PCI Express interfaces on the Q35 motherboards are compliant with the *PCI Express Base Specification Version 1.1*.

- One PCI Express x16 graphics interface
- One PCI Express x4 interface (x16 physically)
- One PCI Express x1 interface.

  Note: On the JD35Q motherboard, this PCI Express x1 slot is multiplexed with the Ethernet port 1 (LAN 2). The motherboard automatically detects when a card is inserted into slot 4 (PCI Express x1), and enables slot 4 and disables LAN 2. When no card is present in slot 4, LAN 2 is enabled.

CMOS RAM and RTC

The chipset integrates real-time clock (RTC) and 256 bytes of CMOS RAM that is used by the BIOS to store configuration information. A replaceable lithium cell battery (type CR2032) backs up both the RTC and the CMOS RAM, and provides approximately 5 years of un-powered backup.

When available, the RTC and CMOS RAM are powered from the +3.3V standby power rather than the lithium battery cell. The system management hardware can monitor the lithium cell voltage directly.

One 1x3-pin Clear CMOS jumper is available to clear the CMOS from the BIOS RAM. By default, pins 1 and 2 are jumpered for normal system operation. To clear the CMOS, jumper pins 2 and 3.

WARNING! For an ATX power supply, you must completely shut down the system, remove the AC power cord and then clear the CMOS.

Firmware hub (FWH)

Q35 motherboards provide a 2MB Firmware Hub (FWH) via the SPI bus. The FWH uses the Intel FWH protocol and does not require an ISA bus. The BIOS ROM is stored in a 2MB flash memory chip. The system BIOS provides support for all functions and devices present on the Q35 motherboards.

Power management

ACPI power states

Table 37 shows the Advanced Configuration and Power Interface (ACPI) 3.0 power states that the Q35 motherboards support.

Table 37. Supported ACPI power states

	VCC state		Supported ACPI states				
	12V/-12V/5V/3.3V	5V standby	G0/S0[1]	G1/S3[2]	G1/S4[3]	G2/S5[4]	G3[5]
Full power	On	On	Yes	-	-	-	-
Standby	Off	On	-	Yes	Yes	Yes	-
Power off	Off	Off	-	-	-	-	Yes
Hard-switched power supply	On	N/A	Yes	-	-	-	-
Hard-switched power supply	Off	N/A	-	-	-	-	Yes

1 G0/S0 – Fully operational; working

2 G1/S3 – Standby (Suspend to RAM). Main memory is still powered. This state allows the resumption of work exactly where it was left at the start of standby.

3 G1/S4 – Non-volatile sleep (Suspend to disk). System context is saved to disk and power removed from all circuits except those required to resume.

4 G2/S5 – Soft off. All devices are un-powered. Memory contents and context are lost.

5 G3 – Mechanical off. System is un-powered with no standby rails. No wake-up is possible.

For information about power consumption of major sources and power supply requirements, see *Electrical specifications* on page 15.

ACPI wake-up

Q35 modules are capable of supporting these wake-up events from S3 and S5 sleep states by configuring the BIOS setup utility:

- Power button
- Onboard LAN. To wake on LAN, make sure that the embedded Ethernet is enabled in the BIOS setup utility and the Ethernet connection is available.
- PS/2 mouse and keyboard
- USB device wake up

System management

The Q35 motherboard includes hardware system management functions using the Winbond W83627DHG chipset. These functions include monitoring system voltages, monitoring temperatures, and monitoring and controlling the system fan.

Voltage monitoring

Table 38 identifies the motherboard voltage rails that are monitored and explains how they are used.

Table 38. Monitored voltage rails

Voltage rail	Usage on motherboard
+12V	Fans, expansion slots
-12V	
+5V	Processor voltage regulator, internal voltage regulator for chipset and system memory, internal logic, USB and video ports, expansion slots
+3.3V	Internal voltage regulator for chipset and processor interface, firmware hub (FWH), clock generator, system monitor, audio, internal logic, expansion slots
3.3Vsb	3.3V standby
VBat_RTC	CMOS battery voltage
V_{core}	Processor core voltage
V_DIMM	Memory voltage

Temperature monitoring

Up to three thermal sensors can be used to monitor temperatures in the system.

- The first sensor measures the motherboard temperature, and is contained within the W83627DHG chipset. This is a localized reading dominated by the motherboard surface temperature around the component.
- The second sensor is located on the processor die to accurately measure the local die temperature. Since the local die temperature fluctuates rapidly with activity, the controller within the W83627DHG filters the signal to produce an average temperature.

  There are temperature deviations across the processor die that cannot be observed by this sensor. See Intel's processor datasheet for further information.
- The third sensor can be connected to the remote thermal sensor header. This sensor should be a silicon diode or transistor connected as a diode, such as a Fairchild MMBT3904 and is used to measure temperatures of the external device connected to the motherboard.

Note: In the BIOS setup utility, you can set a CPU temperature overheat threshold in the Advanced Features > Hardware Monitor menu. When this threshold temperature is reached, the system BIOS will activate the alarm system.

Fan control

The Q35 motherboards support three fan monitors that check the fan tachometer signals to determine the fan's rotational speed. The three monitors are assigned to the processor fan, system fan 1, and system fan 2.

Fan speed modes are controlled in the BIOS setup utility, Advanced Features > Hardware Monitor menu. By default, all fans run at the full speed.

Note: To configure the fan speed modes, be sure to use all 3-pin fans or all 4-pin fans.

Front panel connections and indicators

The Front panel I/O provides support for power switches and LED indicators via an internal 2x8-pin header. See *Front panel I/O header* on page 56 for the pinout definitions of this header.

Power switch

If a soft-switched power supply is used, a momentary switch should be connected between pins 1 and 2 of the power connector. When the switch is closed for more than about 4 seconds, the motherboard powers off—regardless of the state of the operating system. (The action of the switch is configurable in the BIOS.) This power off will cause any system context information to be lost.

See *ATX power connector (24-pin, 12V))* on page 55 and *BIOS customization* on page 50 for the power connector pinouts.

Reset switch

If the reset switch is used, a momentary switch connected between pins 3 and 4 causes the motherboard to restart when the switch is closed.

Power LED

Connect either a single-color LED (usually green) or a two-terminal dual-color LED (usually green/yellow) to indicate the powered status of the Q35 motherboard. In both cases, the "green" cathode should be attached to pin 16 of the front panel I/O header.

Table 39 describes how the indicator is driven when operating with both single and dual-color devices assuming the +5V standby power is available.

Table 39. Power state indicators

LED indicator	LED state	Description
Single-color	Off	The motherboard is powered down or in one of the ACPI sleep states.
	On	The motherboard is fully powered up.
Dual-color (green/ yellow)	Off	The motherboard is powered down (S5).
	Green	The motherboard is fully powered up (S0).
	Yellow	The motherboard is in standby (S3) or hibernating (S4) state.

Hard disk LED

To indicate disk activity on any of the SATA or ATA channels, connect a single-color LED between pins 13 (anode) and 14.

Overheat/fan failure LED

To indicate an overheat of the CPU or a fan failure, connect a single-color LED between pins 7 (anode) and 8.

LAN activity LED

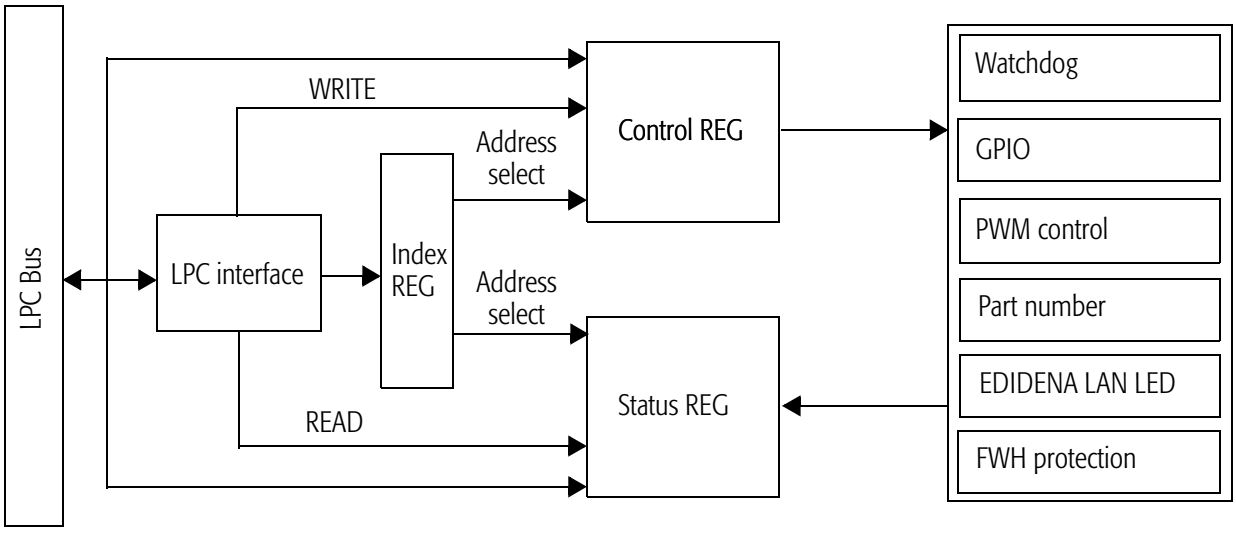
To indicate LAN activity on LAN1, connect a single-color LED between pins 11 (anode) and 12. For LAN2 (if equipped), connect a single-color LED between pins 9 (anode) and 10.

CPLD interfaces

The JD2G03-0-0 and QZ2G03-0-0 motherboards use the Lattice LC4256ZC-75TN00C CPLD to provide the LPC interface, watchdog, power-on sequence control, PWM control, GPIO control, and FWH or SPI flash write-protection control.

Figure shows the Erasable Programmable Logic Device (EPLD) block diagram of these motherboards. For detailed information about control logic and registers, see *Control logic and registers* on page 75.

EPLD block diagram



BIOS CONFIGURATION AND OS SUPPORT 4

BIOS overview

The Q35 system BIOS uses the Phoenix TrustedCore BIOS with RadiSys extensions. BIOS features include:

- Core multi-processing for Intel Core 2 Duo and Pentium Dual-Core processors
- ACPI 3.0 wake up from S3, S4, and S5
- CMOS saving and restoration via BIOS setup utility
- Pre-boot Execution Environment (PXE) boot
- Wake on LAN
- High-performance, power-saving Intel SpeedStep™ technology and CPU throttling
- High-resolution, GUI-based, customizable splash screen
- Intel Vanderpool virtualization technology

The system BIOS stores the system parameters such as types of disk drives and video displays, in the CMOS RAM to initialize the system during boot. The CMOS memory requires very little electrical power. When the system is powered off, a backup RTC battery provides power to the CMOS logic, enabling it to retain system parameters. Each time the system is powered on, the BIOS configures the system with the values stored in the CMOS RAM.

Using the BIOS setup utility, you can display and modify the system configurations.

POST and boot process

The system BIOS performs a Power On Self Test (POST) upon power-on or reset, which attempts to determine whether further operation is possible:

- If a warning occurs, a message is displayed on the primary display device but the boot process does not stop.
- If an error is detected, the boot process is halted.

Failures during POST can be indicated by POST checkpoint codes on the BIOS setup screen or POST card that is installed on the motherboard I/O connector. For detailed information, see *POST checkpoint codes* on page 84.

After POST completes, the system BIOS will search for boot devices in the order configured by the BIOS setup utility and load an operating system from the first boot device found. Control is then passed to the operating system and the system BIOS plays no further part in the boot process except to provide run-time services.

BIOS setup

To enter the BIOS setup utility, press the Delete key during system boot. The system BIOS setup screens and menu options are the standard Phoenix TrustedCore BIOS screens with Q35 extensions. Use the up, down, left, and right arrow keys on your keyboard to navigate through the menu options. Online help is provided in the BIOS setup screens to explain options.

After you have completed the BIOS settings, press F10 or use the commands on the Exit menu to save changes. Press Esc to go immediately to the Exit menu.

For detailed instructions on BIOS configuration, refer to the *Procelerant Endura Q35 BIOS Setup Utility Specification*.

Update and recovery

BIOS release packages are periodically available on the RadiSys Web site to address known issues or to add new features. The release packages include detailed instructions for updating the BIOS.

WARNING! BIOS updates should be undertaken with care and only when necessary. The BIOS can be corrupted if the update is interrupted by a loss of power before it is complete, which will require factory repair of the motherboard. Use the instructions provided with the BIOS update to make sure the BIOS update is successful.

BIOS customization

The splash screen logo and default BIOS settings can be customized using the Phoenix BIOSEdit tool. Contact your Phoenix sales representative for further information.

Operating system support

The following operating systems have been validated by RadiSys for Q35 motherboards:

- Microsoft Windows XP Professional
- Windows XP Embedded
- Windows Vista
- Red Hat Enterprise Linux
- Solaris 10 Update 4

For instructions on installing the operating system, refer to the *Procelerant Endura Q35 Motherboard Quick Start Guide.*

Drivers and utilities

The operating system you select may require you to install device drivers in order to make the system operational. Visit the RadiSys Web site for device drivers and utilities

Onboard connector part numbers

Table 40. Onboard connector part numbers

Onboard connector	Part number	Description
CD-ROM header	HDR-012L	CNT, box/header, 1*4, DIP/2.54/M/11.4*12.75, black, BRASS/PBT, protect.PBF
ATX power connector, 4-pin	SKT-092L	CNT, power-conn, 2*2pin, DIP/M/3,5A/250V, BRASS/LCP, with post, half transpare, Au:15u-in
ATX power connector, 24-pin	SKT-0135L	ATX 2X12 power conn enhance lock, Pb-Free
Chassis intrusion jumper	HDR-001L-2	Header 1X2 Pb-Free
Fan power header	HDR-0027L	Header 4 pin 0.1" straight lock Pb-Free
Front panel I/O header	HDR-003-16	CNT, pin/header, 2*8, DIP/2.54/M, black, brass/PBT
GPIO header	HDR-003L-20	Pin header 2X10, DIP/2.54MM black, Pb-Free
IDE connector	HDR-018L	2X20 shrouded head IDE PC99 (blue), Pb-Free
Lithium cell holder	BTR-006L	Battery socket, Pb-Free
LPT header	HDR-008L	2X13 shrouded header Pb-Free
PCI slot	SKT-BU-PCI SLOTS	CNT, SLOT, PCI, 120pin, DIP/1.27, white, continue pin/2.54, Tail Length:3.18mm, Gold Flash
Memory sockets: DIMM1, DIMM3	SKT-0151-Blue	CNT, memory socket, DDRII 1.8V, 240pin, DIP/1, modulelock/3.18, P-B/NYLON66, blue, Au:11.2-in
Memory sockets: DIMM2, DIMM4	SKT-0151L	DDRII connector, CEDG, 240P, VT062ST Pb-Free
PCI Express x1 slot	SKT-0156L	PCI Express connector, X2, 36pin, Pb-Free
PCI Express x16 slot	SKT-0224L	PCI-E X16 with right side board lock, Pb-Free
PS/2 mouse and keyboard	SKT-079L	STACK Mini-DIN (K/M) PC99 Pb-Free
SATA header	SKT-0169L	SATA vertical DIP, 1.27MM pitch, Pb-Free
SMBus header	HDR-021L	IPMB connector, 4-PIN, 22436040, Pb-Free
USB headers (internal)	SKT-0256L	USB connector, 1port, vertical, Pb-Free
Rear I/O panel – Triple audio jacks	JA33331-H11P-4F	HD audio phone jack vertical 1X3 port, Pb-Free (JA33331-H11P-4F)
Rear I/O panel – RJ45 Gigabit Ethernet port	SKT-0262L	CNT, RJ45/dual USB, P35-152-19W9, Pb-Free
Rear I/O panel –USB ports	SKT-0135L	CNT, I/o-conn, usb*4/16pin, DIP/M/2, black, P-B/PBT
Rear I/O panel –VGA/DVI connector	SKT-0268L	DSUB24P-VGA-COM with screw lock, Pb-Free
Rear I/O panel – UART ports	HDR-013L	Box header 5*2/1 DZP/2.54/M black Pb-FREE

Jumper settings

Speaker (J9)

Setting	Definition
Pins 3-4 jumpered	Internal Speaker
Pins 1-4	External Speaker

The speaker connector pins are for use with an external speaker. To use the onboard speaker, close pins 3-4 with a jumper.

CMOS clear (JRTC1)

Setting	Definition
Pins 1-2 jumpered	Normal operation
Pins 2-3 jumpered	Clear CMOS

To clear CMOS:

1. Power off the system and remove the AC power cord.
2. Move the JRTC1 jumper to pins 2-3 for approximately five seconds.
3. Place JRTC1 jumper back on pins 1-2 to resume normal operation.

PCI slots to system management bus speeds (JI^{2}C1)

Setting	Definition
Jumpered	Enabled
No jumper	Disabled (default)

This jumper allows you to connect PCI/PCI-Express slots to the System Management Bus. The default setting is open to disable the connection.

PCI Express slots to system management bus speeds (JI^{2}C2)

Setting	Definition
Jumpered	Enabled
No jumper	Disabled (default)

This jumper allows you to connect PCI/PCI-Express slots to the System Management Bus. The default setting is open to disable the connection.

USB wake-up (JPUSB1/JPUSB2)

Setting	Definition
Pins 1-2 jumpered	Enabled
Pins 2-3 jumpered	Disabled (default)

Use the JPUSB jumpers to enable the function of system wake-up via USB devices. This allows you to "wake-up" the system by pressing a key on the USB keyboard or by clicking the USB mouse.

JPUSB1 is for back panel USB ports 1/2/3/4/5/6.
JPUSB2 is for front panel USB ports 7/8/9/10 and front accessible USB ports: 11/12.

Notes:

- Before allowing the system to go into standby mode, be sure to remove all USB devices from USB ports that have been disabled.
- The JPUSB jumper settings must match the USB wake-up settings in the BIOS.

Watch dog (JWD)

Setting	Definition
Pins 1-2 jumpered	Reset (default)
Pins 2-3 jumpered	NMI
Open	Disabled

Watch dog is a system monitor that can reboot the system when a software application hangs. Close Pins 1-2 to reset the system if an application hangs. Close Pins 2-3 to generate a non-maskable interrupt signal for the application that hangs. Watch dog must also be enabled in the BIOS. If this jumper is set to Disabled, the Watch Dog Settings listed in the BIOS will be ignored.

Audio (JP5)

Setting	Definition
Pins 1-2 jumpered	Enabled (default)
Pins 2-3 jumpered	Disabled

Gigabit LAN (JPL1, JPL2)

Setting	Definition
Pins 1-2 jumpered	GLAN enabled (default)
Pins 2-3 jumpered	GLAN disabled

The JPL jumpers enable or disable Gigabit LAN ports 1 and 2 on the motherboard.

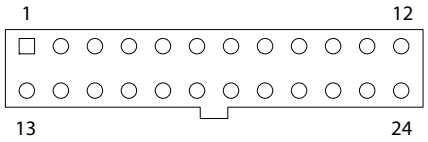
ITE IDE (JP2)

Setting	Definition
Pins 1-2 jumpered	Enabled (default)
Pins 2-3 jumpered	Disabled

Internal device connectors

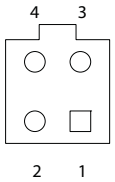
Pin #1 of most internal connectors and headers are marked with an asterisk (*) on the PCB of Q35 motherboards.

ATX power connector (24-pin, 12V))



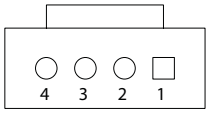
Pin #	Signal	Pin #	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON#
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	Power_GOOD	20	{NC}
9	+5V (standby)	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

ATX power connector (4-pin, 12V)



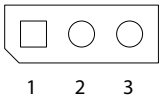
Pin #	Signal	Pin #	Signal
1	GND	2	GND
3	+12V	4	+12V

CD-ROM header



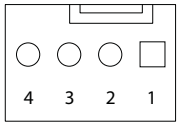
Pin #	Signal	Pin #	Signal
1	Left Stereo	2	GND
3	GND	4	Right Stereo

Clear CMOS jumper



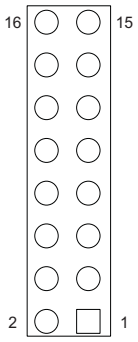
Jumper setting	Configuration
Pins 1 &2 jumpered (default)	Normal operation
Pins 2 & 3 jumpered	Clear CMOS

Fan header



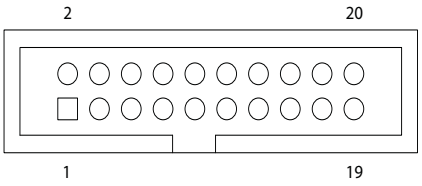
Pin #	Signal	Pin #	Signal
1	GND	2	+12V
3	Tachometer	4	FAN_PWM

Front panel I/O header



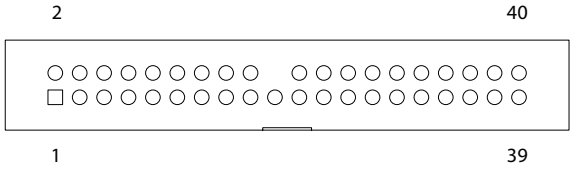
PIN#	Description	PIN#	Description	Wiring Notes
16	Power LED	15	LED_Anode+	Connect pins 15 and 16 to the power LED
14	HDD LED	13	LED_Anode+	Connect pins 13 and 14 to the hard disk drive (HDD) LED to display disk activity
12	NIC1 LED	11	LED_Anode+	Connect pins 11and 12 to the NIC1 (network interface controller) LED to display network activity
10	NIC2 LED	9	LED_Anode+	Connect pins 9 and 10 to the NIC2 LED to display network activity
8	OH/Fan fail LED	7	LED_Anode+	Connect pins 7 and 8 to the overheat/fan failure LED
6	—	5	—	Not connected
4	Ground	3	Reset button	Connect pins 3 and 4 to the hardware reset button
2	Ground	1	Power button	Connect pins 1 and 2 to the power button

GPIO header



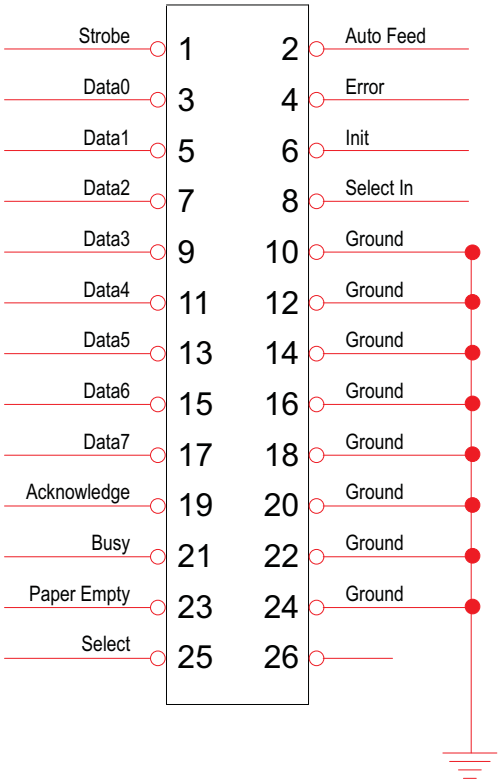
Pin #	Signal	Pin #	Signal
1	GND	2	+5V fused
3	GPIO_PWM	4	GPIO20
5	GPIO21	6	GPIO22
7	GPIO10	8	GPIO11
9	GPIO12	10	GPIO13
11	GPIO14	12	GPIO15
13	GPIO16	14	GPIO17
15	{NC}	16	KEY
17	GND	18	GPI23
19	GND	20	GPI24

IDE connector



Pin #	Signal	Pin #	Signal
1	Reset#	2	GND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	Key pin
21	DMARQ	22	GND
23	DIOW#	24	GND
25	DIOR#	26	GND
27	IORDY	28	CSEL
29	DMACK#	30	GND
31	INTRQ	32	Reserved
33	DA1	34	PDIAG#
35	DA0	36	DA2
37	CS0#	38	CS1#
39	DASP#	40	GND

LPT



Pin #	Signal	Pin #	Signal
1	Strobe	2	Auto Feed
3	Data0	4	Error
5	Data1	6	Init
7	Data2	8	Select In
9	Data3	10	Ground
11	Data4	12	Ground
13	Data5	14	Ground
15	Data6	16	Ground
17	Data7	18	Ground
19	Acknowledge	20	Ground
21	Busy	22	Ground

Pin #	Signal	Pin #	Signal
23	Paper Empty	24	Ground
25	Select	26	{Omitted}

PCI Express x1 slot

The PCI Express x1 slot is available on the JD35Q in lieu of the second gigabit Ethernet LAN port (LAN2). When no card is present in the PCI Express x1 slot, LAN2 is enabled.

Note: The signals for hot plug presence detection in the table below are not supported on Q35 motherboards.

Pin #	Side B		Side A	
	Signal	Description	Signal	Description
1	+12V	12V power	PRSNT1#	Hot plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMDAT	SMBus (System Management Bus) data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for link reactivation	PERST#	fundamental reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair Lane 0	REFCLK-	Reference clock (differential pair)
15	PETn0	Transmitter differential pair Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential pair Lane 0
17	PRSNT2#	Hot plug presence detect	PERn0	Receiver differential pair Lane 0
18	GND	Ground	GND	Ground

PCI Express x4 slot

The signals for hot plug presence detection in the table below are not supported on Q35 motherboards.

Pin #	Side B		Side A	
	Signal	Description	Signal	Description
1	+12V	12V power	PRSNT1#	Hot plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMDAT	SMBus data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	3.3V power
10	3.3Vaux		+3.3V	3.3V power
11	WAKE#	Signal for link reactivation	PERST#	fundamental reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair Lane 0	REFCLK-	Reference clock (differential pair)
15	PETn0	Transmitter differential pair Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential pair Lane 0
17	PRSNT2#	Hot plug presence detect	PERn0	Receiver differential pair Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair Lane 1	RSVD	Reserved
20	PETn1	Transmitter differential pair Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential pair Lane 1
22	GND	Ground	PERn1	Receiver differential pair Lane 1
23	PETp2	Transmitter differential pair Lane 2	GND	Ground
24	PETn2	Transmitter differential pair Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential pair Lane 2
26	GND	Ground	PERn2	Receiver differential pair Lane 2
27	PETp3	Transmitter differential pair Lane 3	GND	Ground
28	PETn3	Transmitter differential pair Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential pair Lane 3
30	RSVD	Reserved	PERn3	Receiver differential pair Lane 3
31	PRSNT2#	Hot plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

PCI Express x16 slot

The signals for hot plug presence detection in the table below are not supported on Q35 motherboards.

Pin #	Side B		Side A	
	Signal	Description	Signal	Description
1	+12V	12V power	PRSNT1#	Hot plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMDAT	SMBus (System Management Bus) data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	3.3V power
10	3.3Vaux		+3.3V	3.3V power
11	WAKE#	Signal for link reactivation	PERST#	Fundamental reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair Lane 0	REFCLK-	Reference clock (differential pair)
15	PETn0	Transmitter differential pair Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential pair Lane 0
17	PRSNT2#	Hot plug presence detect	PERn0	Receiver differential pair Lane 0
18	GND	Ground	GND	Ground
End of X1 connector				
19	PETp1	Transmitter differential pair Lane 1	RSVD	Reserved
20	PETn1	Transmitter differential pair Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential pair Lane 1
22	GND	Ground	PERn1	Receiver differential pair Lane 1
23	PETp2	Transmitter differential pair Lane 2	GND	Ground
24	PETn2	Transmitter differential pair Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential pair Lane 2
26	GND	Ground	PERn2	Receiver differential pair Lane 2
27	PETp3	Transmitter differential pair Lane3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair Lane 3
30	RSVD	Reserved	PERn3	Receiver differential pair Lane 3

Pin #	Side B		Side A	
	Signal	Description	Signal	Description
31	PRSNT2#	Hot plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
End of X4 connector				
33	PETp4	Transmitter differential pair Lane 4	RSVD	Reserved
34	PETn4	Transmitter differential pair Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential pair Lane 4
36	GND	Ground	PERn4	Receiver differential pair Lane 4
37	PETp5	Transmitter differential pair Lane 5	GND	Ground
38	PETn5	Transmitter differential pair Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential pair Lane 5
40	GND	Ground	PERn5	Receiver differential pair Lane 5
41	PETp6	Transmitter differential pair Lane 6	GND	Ground
42	PETn6	Transmitter differential pair Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential pair Lane 6
44	GND	Ground	PERn6	Receiver differential pair Lane 6
45	PETp7	Transmitter differential pair Lane 7	GND	Ground
46	PETn7	Transmitter differential pair Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential pair Lane 7
48	PRSNT2#	Hot plug presence detect	PERn7	Receiver differential pair Lane 7
49	GND	Ground	GND	Ground
End of x8 connector				
50	PETp8	Transmitter differential pair Lane 8	RSVD	Reserved
51	PETn8	Transmitter differential pair Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential pair Lane 8
53	GND	Ground	PERn8	Receiver differential pair Lane 8
54	PETp9	Transmitter differential pair Lane 9	GND	Ground
55	PETn9	Transmitter differential pair Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential pair Lane 9
57	GND	Ground	PERn9	Receiver differential pair Lane 9
58	PETp10	Transmitter differential pair Lane 10	GND	Ground
59	PETn10	Transmitter differential pair Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential pair Lane 10
61	GND	Ground	PERn10	Receiver differential pair Lane 10
62	PETp11	Transmitter differential pair Lane 11	GND	Ground
63	PETn11	Transmitter differential pair Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential pair Lane 11
65	GND	Ground	PERn11	Receiver differential pair Lane 11
66	PETp12	Transmitter differential pair Lane 12	GND	Ground
67	PETn12	Transmitter differential pair Lane 12	GND	Ground

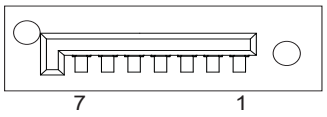
Pin #	Side B		Side A	
	Signal	Description	Signal	Description
68	GND	Ground	PERp12	Receiver differential pair Lane 12
69	GND	Ground	PERn12	Receiver differential pair Lane 12
70	PETp13	Transmitter differential pair Lane 13	GND	Ground
71	PETn13	Transmitter differential pair Lane 13	GND	Ground
72	GND	Ground	PERp13	Receiver differential pair Lane 13
73	GND	Ground	PERn13	Receiver differential pair Lane 13
74	PETp14	Transmitter differential pair Lane 14	GND	Ground
75	PETn14	Transmitter differential pair Lane 14	GND	Ground
76	GND	Ground	PERp14	Receiver differential pair Lane 14
77	GND	Ground	PERn14	Receiver differential pair Lane 14
78	PETp15	Transmitter differential pair Lane 15	GND	Ground
79	PETn15	Transmitter differential pair Lane 15	GND	Ground
80	GND	Ground	PERp15	Receiver differential pair Lane 15
81	PRSNT2#	Hot plug presence detect	PERn15	Receiver differential pair Lane 15
82	GND	Ground	GND	Ground

PCI slot

Pin #	Side B signal	Side A signal
1	-12V	TRST#
2	TCK	+12V
3	GND	TMS
4	TDO	TDI
5	+5V	+5V
6	+5V	INTA#
7	INTB#	INTC#
8	INTD#	+5V
9	PRSNT1#	Reserved
10	Reserved	+3.3V (I/O)
11	PRSNT2#	Reserved
12	CONNECTOR KEY	
13	CONNECTOR KEY	
14	Reserved	3.3Vaux
15	GND	RST#
16	CLK	+3.3V (I/O)
17	GND	GNT#
18	REQ#	GND
19	+3.3V (I/O)	PME#
20	AD[31]	AD[30]
21	AD[29]	+3.3V
22	GND	AD[28]
23	AD[27]	AD[26]
24	AD[25]	GND
25	+3.3V	AD[24]
26	C/BE[3]#	IDSEL
27	AD[23]	+3.3V
28	GND	AD[22]
29	AD[21]	AD[20]
30	AD[19]	GND
31	+3.3V	AD[18
32	AD[17]	AD[16]
33	C/BE[2]#	+3.3V
34	GND	FRAME#
35	IRDY#	GND
36	+3.3V	TRDY#
37	DEVSEL#	GND

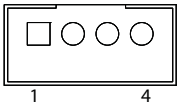
Pin #	Side B signal	Side A signal
38	PCIXCAP	STOP#
39	LOCK#	+3.3V
40	PERR#	SMBCLK
41	+3.3V	SMBDAT
42	SERR#	GND
43	+3.3V	PAR
44	C/BE[1]#	AD[15]
45	AD[14]	+3.3V
46	GND	AD[13]
47	AD[12]	AD[11]
48	AD[10]	GND
49	M66EN	AD[09]
50	GND	GND
51	GND	GND
52	AD[08]	C/BE[0]#
53	AD[07]	+3.3V
54	+3.3V	AD[06]
55	AD[05]	AD[04]
56	AD[03]	GND
57	GND	AD[02]
58	AD[01]	AD[00]
59	+3.3V (I/O)	+3.3V (I/O)
60	ACK64#	REQ64#
61	+5V	+5V
62	+5V	+5V

SATA header



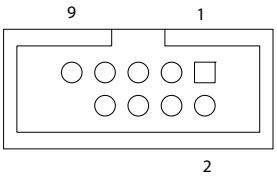
Pin #	Signal	Pin #	Signal
1	GND	2	SATA_TXP
3	SATA_TXN	4	GND
5	SATA_RXN	6	SATA_RXP
7	GND	8	{Omitted}

SMBus header



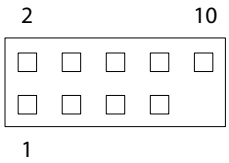
Pin #	Signal	Pin #	Signal
1	+3.3V_STANDBY	2	SMB_DATA
3	SMB_CLK	4	GND

UART port (internal)



Pin #	Signal	Pin #	Signal
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	NC

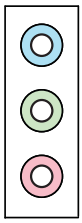
USB header (internal)



Pin #	Signal	Pin #	Signal
1	USB +5V Power	2	USB +5V Power
3	USB1-	4	USB2-
5	USB1+	6	USB2+
7	GND	8	GND
9	{Omitted pin}	10	GND

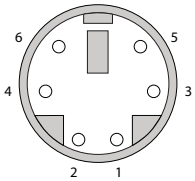
External Device Connectors

Audio jacks (triple, build option)



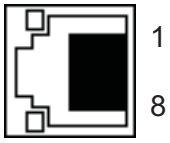
Port	Configuration
Blue	Line in
Green	Line out
Pink	Microphone input

PS/2 mouse and keyboard



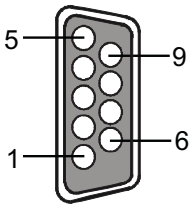
Pin #	Signal	Pin #	Signal
1	Data	4	VCC
2	NC	5	Clock
3	Ground	6	NC

RJ45 Gigabit Ethernet port



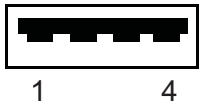
Pin #	Signal	Pin #	Signal
1	MDI0+	5	MDI2+
2	MDI0-	6	MDI2-
3	MDI1+	7	MDI3+
4	MDI1-	8	MD3-

UART port (rear I/O)



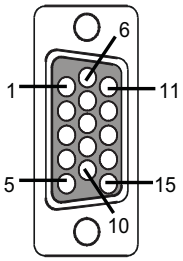
Pin #	Signal	Pin #	Signal
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	{Omitted}

USB ports (rear I/O)



Pin #	Signal	Pin #	Signal
1	+5V	3	PO+
2	PO-	4	GND

VGA connector



Pin #	Signal	Pin #	Signal
1	RED	2	GREEN
3	BLUE	4	ID2
5	GND	6	RED GND
7	GREEN GND	8	BLUE GND
9	+5V (optional)	10	SYNC GND
11	ID0	12	ID1 or SDA
13	HSYNC	14	VSYNC
15	ID3 or SCLK	16	

I/O map

Address (HEX)	Description
0000 – 000F	DMA controller 1
0020 – 0021	Interrupt controller 1
002E – 002F	Super I/O controller
0040 – 0043	Timer controller
004E – 004F	TPM controller
0060, 0064	Keyboard controller emulation register (returns zero)
0068, 006C	CPLD port
0070 – 0073	RTC and CMOS RAM
0080 – 008F	DMA controller page registers (for channels 1 and 2)
0092	PC compatible port 92 (fast A20 and PIC)
00A0 – 00A1	Interrupt controller 2
00B2 – 00B3	APM controller register
00C0 –00DF	DMA controller 2
00F0	Floating point error register
0170 – 0177	Secondary IDE controller (map to SATA or PATA interface)
01F0 – 01F7	Primary IDE controller (map to SATA or PATA interface)
0374 – 0376	Secondary IDE controller (map to SATA or PATA interface)
x3B0 – x3BB	VGA controller
X3C0 – X3DA	CGA controller registers
03F6 – 03F7	Primary IDE controller (map to SATA or PATA interface)
03F8 – 03FF	COM1 port
04D0 – 04D1	Interrupt controller
0CF8 – 0CFF	PCI configuration address and data registers
1000 – 105F	ACPI registers
1060 – 107F	TCO controller
1200 – 12FF	Audio mixer
1300 – 133F	Audio master
8000 – 802F	Glue functions in Super I/O controller
FFA0 – FFA7	Primary IDE bus master registers
FFA8 – FFAF	Secondary IDE bus master registers

Address (HEX)	Description
Dynamically assigned	Four USB controllers (32 locations on a 32-byte boundary)
Dynamically assigned	SMBus controller (16 locations on a 16-byte boundary)
Dynamically assigned	LAN controller (4096 locations on a 4096-byte boundary)

PCI bus topology

Physical Device		Bus	Dev	Fun	AdSel	Ints
Intel Q35 (GMCH)	Host bridge /DRAM controller	0 Host	00	0	Internal	
	Host-PCI Express bridge	0 Hub Link	01	0	Internal	
	Integrated graphics device	0 Hub Link	02	0	Internal	
	Integrated graphics device	0 Hub Link	02	1	Internal	
ICH9/ICH9DO (ICH)	Intel high definition audio	0 Hub Link	27	0	Internal	
	PCI Express port 1	0 Hub Link	28	0	Internal	
	PCI Express port 2	0 Hub Link	28	1	Internal	
	PCI Express port 3	0 Hub Link	28	2	Internal	
	PCI Express port 4	0 Hub Link	28	3	Internal	
	PCI Express port 5	0 Hub Link	28	4	Internal	
	PCI Express port 6	0 Hub Link	28	5	Internal	
	USB UHCI controller 1	0 Hub Link	29	0	Internal	
	USB UHCI controller 2	0 Hub Link	29	1	Internal	
	USB UHCI controller 3	0 Hub Link	29	2	Internal	
	USB UHCI controller 4	0 Hub Link	29	3	Internal	
	USB 2.0 EHCI controller	0 Hub Link	29	7	Internal	
	PCI-to-PCI bridge	0 Hub Link	30	0	Internal	
PCI Express	PCI Express x16 graphics card	1 PCIE	0	0	External	INTA
	PCI Express x1 LAN	2 PCIE	0	0	External	INTA
	PCI Express x1 LAN	3 PCIE	0	0	External	INTB
	Not connected	4 PCIE	0	0	-	-
	Not connected	5 PCIE	0	0	-	-
	Not connected	6 PCIE	0	0	-	-
	Not connected	7 PCIE	0	0	-	-
PCI bus	Mini PCI socket	8 PCI	4	0	AD 20	INTA & INTB
	PCMICIA controller TI PCI1510	8 PCI	5	0	AD 21	INTC
	PCI to UART bridge EXAR XR17D152	8 PCI	6	0	AD 22	INTD
	Intel integrated LAN	8 PCI	7	0	Internal	Disable

SMBus resource allocation

Device	Address
ICS 9LPRS511	1101001X
DIMM 0 Slot	10100000
DIMM 1 Slot	10100010
DIMM 2 Slot	10100100
DIMM 3 Slot	10101000
SIO H/W Monitor	01011010

ISA interrupt allocation

Interrupt	Function
IRQ0	System timer (internal ICH7-M connection)
IRQ1	Keyboard controller via SERIRQ
IRQ2	Cascade interrupt input (internal ICH7-M connection)
IRQ3	COM2 via SERIRQ, PIRQ#
IRQ4	COM1 via SERIRQ, PIRQ#
IRQ5	PCI pool
IRQ6	PCI pool
IRQ7	PCI pool
IRQ8	RTC
IRQ9	PCI pool/Option for SCI, TCO
IRQ10	PCI pool/Option for SCI, TCO
IRQ11	PCI pool/Option for SCI, TCO
IRQ12	PS/2 mouse (if present and enabled)
IRQ13	Numeric coprocessor ~FERR (internal ICH7-M connection)
IRQ14	IDEIRQ (legacy mode, non-combined or combined mapped as primary), SATA primary (legacy mode)
IRQ15	IDEIRQ (legacy mode, combined, mapped as secondary), SATA secondary (legacy mode)
NMI	ICH7-M when ~SERR or ~IOCHK is asserted (software controlled)
SMI	System management interrupt
PIRQA	Internal devices are routable
PIRQB	Internal devices are routable
PIRQC	Internal devices are routable
PIRQD	Internal devices are routable
PIRQE	Option for SCI, TCO, HPET#0, 1, 2; other internal devices are routable
PIRQF	Option for SCI, TCO, HPET#0, 1, 2; other internal devices are routable
PIRQG	Option for SCI, TCO, HPET#0, 1, 2; other internal devices are routable
PIRQH	Option for SCI, TCO, HPET#0, 1, 2; other internal devices are routable

ISA DMA channel allocation

The motherboard does not have an ISA bus, but uses a faster ISA-compatible DMA controller for compatibility with the AT architecture.

DMA channel	Description
Channel 0	Unassigned 8-bit channel
Channel 1	Unassigned 8-bit channel
Channel 2	Unassigned 8-bit channel
Channel 3	Unassigned 8-bit channel
Channel 4	Cascade channel
Channel 5	Unassigned 16-bit channel
Channel 6	Unassigned 16-bit channel
Channel 7	Unassigned 16-bit channel

Control logic and registers

Index register

I/O location: 062h

Default: 0000 0000b

Index:

00h	Watchdog control (write-only)
00h	Watchdog kick (write-only)
00h	Watchdog status (read-only)
01h	Watchdog time period
02h	General Purpose I/O port 1
03h	General Purpose I/O port 2 and control
04h-07h	Reserved
08h	PWM control
09h	Reserved
0Ah	Miscellaneous status and control
0Bh-11h	Reserved
12h	Hardware version
13h	Port80 decoder
14h-17h	Reserved
18h	Part number, xxx-xxxxx-xxYY
19h	Part number, xxx-xxxxx-YYxx
1Ah	Part number, xxx-xxxYY-xxxx
1Bh	Part number, xxx-xYYxx-xxxx
1Ch	Part number, xxY-Yxxxx-xxxx
1Dh	Part number, YYx-xxxxx-xxxx
1Eh-1Fh	Reserved

Watchdog control

7	6	5	4	3	2	1	0
Prescale				RES	SMI	WEN	0
W	W	W	W	W	W	W	W

I/O location: 066h

Index: 00h

Default: N/A

Prescale: 4-bit value to set the watchdog counter period

0..15	16..1s period (a value of 1010b gives a period of 6 seconds)
1	Description

RES: Watchdog reset after second timeout

0	No reset
1	Force system reset after second watchdog timeout

SMI: Generate SMI after first timeout[1]

0	No SMI
1	Generate SMI after first watchdog timeout

WEN: Watchdog timer enable

0	Disable watchdog timer
1	Enable and start watchdog timer

Watchdog kick

7	6	5	4	3	2	1	0
Do not care							1
W	W	W	W	W	W	W	W

I/O location: 066h

Index: 00h

Default: N/A

1. Use of this feature normally requires a custom BIOS. The standard BIOS does not route the SMI and thus ignores the event, which causes a system reset after the second timeout unless the timer is restarted. For further information, see *BIOS customization* on page 50.

Watchdog status

7	6	5	4	3	2	1	0
Prescale				TO2	TO1	WEN	0
RO	RO	RO	RO	RO	RO	RO	RO

I/O location: 066h
Index: 00h
Default: N/A
Prescale: 4-bit value to set the watchdog counter period (copy of the data written)
WEN: Watchdog timer enable
0 Watchdog timer is disabled
1 Watchdog timer is enabled
TO1: First timeout
0 First timeout has not occurred
1 Watchdog timer has expired at least once
TO2: Second timeout
0 Second timeout has not occurred
1 Watchdog timer has expired at least twice

Watchdog timeout period

7	6	5	4	3	2	1	0
Watchdog timeout period							
RW	RW	RW	RW	RW	RW	RW	RW

I/O location: 066h
Index: 01h
Default: 1111 1111b
Time period:
0 Do not use (it causes immediate timeout)
1-255 Timeout period in units of prescale value seconds

Note: Timeout periods load only after the watchdog kick occurs.

General Purpose I/O port

The GPIO port is a 20-pin header directly connected to the CPLD. For pinout definitions of the GPIO header, see *GPIO header* on page 57. When used for a character LCD display interface, the lower 14 pins are connected directly to the display with a separate backlight supply.

The character LCD display logic in the PLD is driven purely by the BIOS. There is no automatic generation of the interface control signals (Table 41).

The PWM signal from the CPLD requires an inverting low-pass filter in order to correctly drive the contrast voltage to the display.

Table 41. Character LCD display interface control signals

Pin	Display name	GPIO pin	GPIO name	Description
1	VSS	1	GND	Digital ground reference
2	VDD	2	+5V	+5V power supply to display
3	VO	3	PWM	Contrast voltage between 0 and +5V
4	RS	4	GPIO20	Register selection
5	R/W	5	GPIO21	Read/Write#
6	E	6	GPO22	Enable
7	DB0	7	GPIO10	Data bit 0
8	DB1	8	GPIO11	Data bit 1
9	DB2	9	GPIO12	Data bit 2
10	DB3	10	GPIO13	Data bit 3
11	DB4	11	GPIO14	Data bit 4
12	DB5	12	GPIO15	Data bit 5
13	DB6	13	GPIO16	Data bit 6
14	DB7	14	GPIO17	Data bit 7
15	A (+)	N/A	N/A	Backlight anode (connect to backlight supply)
16	A (-)	N/A	N/A	Backlight anode (connect to backlight supply)

General Purpose I/O port 1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
RW	RW	RW	RW	RW	RW	RW	RW

I/O location: 066h

Index: 02h

Default: xxxx xxxxb, where x is the status of inputs

P17-P10, GPIO port 1 data:

- When programmed as an output, the GPIO port 1 bit reflects the value that has been written into this register.
- When programmed as inputs, writes are ignored and a read follows the state of the GPIO port 1 signal. Direction control is via the GPIO port 2 and control register.

General Purpose I/O port 2

7	6	5	4	3	2	1	0
D201	D157	D104	P24	P23	P22	P21	P20
RW	RW	RW	RO	RO	RW	RW	RW

I/O location: 066h

Index: 03h

Default: 000x x0xxb, where x is the status of inputs

P21 — P20, GPIO port 2 data:

- When programmed as an output, the GPIO port 2 bit reflects the value that has been written into this register. When programmed as inputs, writes are ignored and a read follows the state of the GPIO port 2 signal. Direction control is via the D201 control.

P22, GPIO port 2 data:

- This bit is output only. GPIO port 2 bit 2 reflects the value that has been written into this register.

P24 — P23, GPIO port 2 data:

- These bits are input only. Writes to these bits have no effect; reads reflect the state of the GPIO port 2 bits 4 and 3 respectively.

D104, GPIO port 1 bits 0 — 4 direction control:

- 0: GPIO bits 10 — 14 are inputs
- 1: PIO bits 10 — 14 are outputs

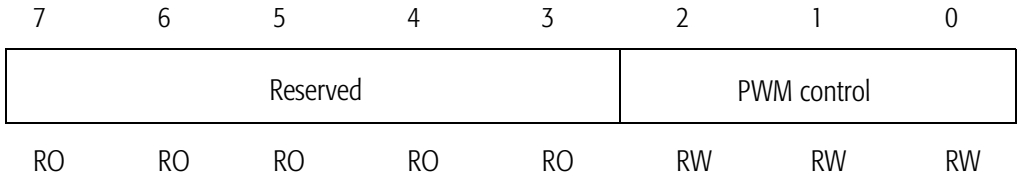
D157, GPIO port 1 bits 5 — 7 direction control:

- 0: GPIO bits 15 — 17 are inputs
- 1: GPIO bits 15 — 17 are outputs

D201, GPIO port 2 bits 0 — 1 direction control:

- 0: GPIO bits 20 — 21 are inputs
- 1: GPIO bits 20 — 21 are outputs

PWM control



I/O location: 066h

Index: 08h

Default: 00000000b

PWM control: Determines the pulse width of the PWM output. (0% results in the display Vo being driven to 0V, 100% results in the display Vo being driven to 5V).

Description:

000	0%
001	12%
010	25%
011	37%
100	50%
101	62%
110	75%
111	100%

FWH/SPI flash write protection

When the CPLD write protect pins are connected directly to the FWH, the write protection capability can be managed through the CPLD. When the BIOS ROM on the board is implemented via an SPI flash device, the FWHWP# should be connected to the SPI flash WP# pin.

7	6	5	4	3	2	1	0
Reserved						TBE	BBE
RO	RO	RO	RO	RO	RO	RW	RW

I/O location: 066h

Index: 0Ah

Default: 1111 1100b

BBE: FWH top block enable

0 Writes to top 64kB of FWH are disabled

1 Writes to top 64kB of FWH are enabled

TBE: FWH bottom block enable/SPI flash enable

0 Writes to FWH/SPI flash (except top block) are disabled

1 Writes to FWH/SPI flash (except top block) are enabled

Hardware version

Four pins are dedicated to the hardware version feature. To implement this feature, the hardware should connect strapping resistors to each of the four HW_VERn pins to pull them high or low. Each board revision (or bill of materials revision) would then encode a unique binary value onto these pins. Software can read back the value encoded onto these pins to determine the board revision.

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSV	Hardware version			
RO	RO	RO	RO	RO	RO	RO	RO

I/O location: 066h

Index: 12h

Default: 0010 vvvvb

Hardware version: Determines hardware version using strapping resistors.

Port80 display

The CPLD supports a BIOS-assisted four-LED display of PORT80 codes. The CPLD register is designed to hold an 8-bit value that is mapped onto four bi-color LEDs. The expectation is that the system BIOS is modified to add a write to this register as part of the port80 POST display. The CPLD does not automatically decode writes to I/O address 080h.

Each of the four LEDs is a bi-color red/green (both together shows orange) and encodes two bits of the 8-bit POST code value: one from the upper four bits (red element) and one from the lower four bits (green element). Some examples are listed below (R=red, G=green, O=orange, F=off).

POST code 20h = FFRF

POST code 02h = FFGF

POST code 33h = FFOO

To implement this, connect the four bi-color common anode LEDs as shown in the table below.

LED	Red cathode	Anode	Green cathode
3[1]	PORT80_7	LED supply through resistor	PORT80_3
2	PORT80_6	LED supply through resistor	PORT80_2
1	PORT80_5	LED supply through resistor	PORT80_1
0[2]	PORT80_4	LED supply through resistor	PORT80_0

[1] LED 3 is most significant.

[2] LED 0 is least significant.

7	6	5	4	3	2	1	0
Port80 MSB				Port80 LSB			
RW	RW	RW	RW	RW	RW	RW	RW

I/O location: 066h

Index: 13h

Default: 0000 0000b

Port80 LSB: Display port80 least significant bytes.

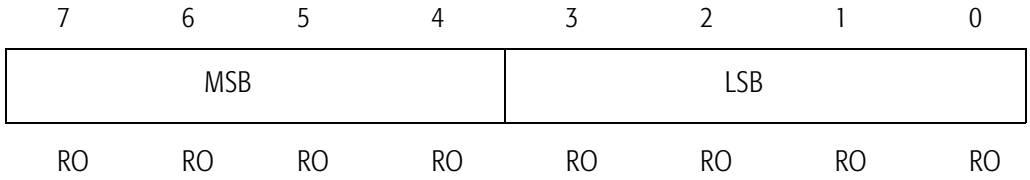
Port80 MSB: Display port80 most significant bytes.

Note: The CPLD pins invert port80 data to drive LEDs.

CPLD code part number

The JTAG interface to the CPLD should be connected to ICH GPO pins to enable software updates to the CPLD. If the board is designed to allow programming via ICT, then the ICH should be connected to the four JTAG pins through 1kohm resistors. It is recommended to follow the ICH GPIO pin usage in the table below.

ICH GPIO	JTAG pin	Description
GPO14	TCK	JTAG programming interface data clock
GPO15	TDI	JTAG programming interface data input
GPI10	TDO	JTAG programming interface data out
GPO25	TMS	JTAG programming interface mode select



I/O location: 066h

Index: 18h, 19h, 1Ah, 1Bh, 1Ch, 1Dh

Default: N/A

LSB: Least significant bytes.

MSB: Most significant bytes.

Note: To read CPLD code part number, data stored in indexes 18, 19, 1A, 1B, 1C, 1D must be read.

POST checkpoint codes

POST 80 codes

The tables that follow list the POST checkpoint codes that the system BIOS may send to I/O port 80h during POST. They are presented in an alphabetically ascending order and are not necessarily in order of execution.

If an error occurs at any of the listed checkpoints, the system attempts to generate beeps to indicate where the error occurred. To hear the beeps, connect a speaker (not included) to the speaker pin on the front panel I/O header. Beep codes are derived from the checkpoint code in the following way:

1. The 8-bit hexadecimal checkpoint code is converted to binary, then the binary number is divided into four 2-bit groups. For example:

   Checkpoint code 20h = 00100000 = 00-10-00-00

2. Each 2-bit group is converted to a one-based number, and 1 is added to indicate the number of beeps:

3. 00 10 00 00 = 1-3-1-1 beeps

Note: Only standard Phoenix TrustedCore BIOS POST 80 codes are listed in the tables below. If you encounter other POST 80 codes, contact RadiSys for further assistance.

Phoenix TrustedCore BIOS checkpoint codes

Checkpoint Code	Description
01h	IPMI Initialization.
02h	Verifies that CPU is in real mode from cold start.
03h	Disables NMIs.
04h	Gets CPU type from CPU registers.
06h	Miscellaneous hardware initialization.
07h	Disables system ROM shadow and start to execute from the flash device.
08h	Initializes chipset registers to power-on defaults.
09h	Sets In-POST bit in CMOS.
0Ah	Completes any implementation-specific CPU initialization.
0Bh	Enables L1 cache during POST.
0Ch	Initializes cache(s).
0Fh	Disables IDE operation.
11h	Alternates register initialization.
12h	Restores contents of CR0 following CPU reset
13h	Resets PCI devices in early POST.
14h	Initializes and configures the keyboard controller.
16h	Verifies ROM BIOS checksum.
17h	Initializes external cache before memory auto size.

Checkpoint Code	Description
18h	Initializes the timers.
1Ah	Tests the DMA registers.
1Ch	Initializes interrupt controllers for some shutdowns.
20h	Verifies DRAM refresh.
22h	Initializes the Keyboard Controller for Keyboard Test.
24h	Sets 4GB segments for DS,ES,FS,GS,SS.
28h	Sizes DRAM.
29h	Initializes the POST Memory Manager.
2Ah	Zeroes the RAM up to the minimum RAM specified in the chipset RAM table.
2Ch	Tests address lines of the RAM.
2Eh	Tests the first 4MB of RAM.
2Fh	Initializes external cache before shadowing.
32h	Computes CPU clock speed in MHz.
33h	Initializes the Phoenix Dispatch Manager.
34h	Tests the CMOS RAM and RTC (S2D)
36h	Vector to the proper shutdown routine.
38h	Shadows system BIOS ROM.
3Ah	Auto sizes the external cache.
3Ch	Advanced chipset configuration.
3Dh	Alternates register configuration.
42h	Initializes interrupt vectors.
45h	POST device initialization.
46h	Verifies that the copyright message is intact.
48h	Verifies the hardware configuration and notes whether the system has color or monochrome video.
49h	Initializes the Plug and Play, and PCI.
4Ah	Initializes the video device.
4Bh	Initializes QuietBoot (splash screen).
4Ch	Shadows video BIOS ROM.
4Eh	Displays the copyright message.
4Fh	Allocates storage for Multiboot tables.
50h	Displays the CPU type and speed.
52h	Initializes and Configures the Keyboard & PS/2 Mouse.
55h	Configures USB devices.
58h	Tests hot interrupts
59h	Initializes the POST display service.
5Ah	Displays “Press F2 for Setup“prompt.
5Bh	Disables L1 cache.
5Ch	Determines size of conventional memory.
60h	Performs memory tests on extended RAM.

Checkpoint Code	Description
62h	Preforms address tests on extended RAM.
66h	Configures MTRR for extended memory caching.
67h	Initializes the non-primary processors.
68h	Enables cache(s).
69h	Initializes SMM, SMRAM and SMI code.
6Ah	Displays cache size.
6Ch	Displays BIOS shadow status.
6Eh	Zeroes un-initialized extended memory with cache on.
70h	Displays any errors found.
72h	Checks bad configuration.
76h	Reports if there was a Keyboard or Controller failures.
7Ch	Initializes hardware interrupt vectors.
7Eh	Coprocessor initialization.
81h	POST device initialization.
82h	Initializes RS232 devices.
83h	Configures non-MCD IDE controllers.
84h	Initializes parallel port(s).
85h	Configures PC Compatible Plug and Play ISA devices.
87h	Initializes MCDs (motherboard configurable devices).
88h	Initializes time-outs, key buffer, soft reset flag, and shadow RAM.
89h	Enables NMIs.
8Ah	Initializes extended BIOS data area.
8Bh	Sets up PS/2 mouse interrupt & initialize extended BDA.
8Ch	Initializes legacy floppy disk drive(s).
90h	Tests hard disks.
91h	Programs timing registers according to PIO modes.
93h	Creates MP tables.
95h	Tests CDROM.
96h	Exits big real mode.
97h	Fixes up the MP table physical pointer and checksum.
98h	Configures non-PC-compatible Plug and Play ISA devices, PCI IRQs, enable PCI devices and ROM-scan.
99h	Checks SMART status.
9Ch	Late SMM (system memory mode) initialization.
9Dh	Initializes the system security engine.
9Eh	Enables the proper hardware interrupts.
A0h	Sets time of day.
A2h	Tests if key lock or keyboard controller password is on.
A8h	Removes the “Press F2 for Setup“prompt.
AAh	Checks if User has requested to enter setup.

Checkpoint Code	Description
ACh	Checks to see if setup should be executed.
AEh	Clears ConfigFailedBit and InPostBit in CMOS.
B0h	Checks for POST errors.
B2h	Clears CMOS bits to indicate that POST is complete.
B3h	Stores enhanced CMOS values in non-volatile area.
B5h	Terminates QuietBoot (splash screen).
B6h	Queries for password before boot.
B7h	Configures ACPI tables for OS use.
B9h	Prepares to boot.
BAh	Executes DMI handlers.
BCh	Clears the parity error latch, set correct NMI state.
BDh	Displays the "boot first"menu.
BEh	Clears the screen.
BFh	Checks the reminder features (virus, backup).
C0h	Boots to operating system via Int19.
C1h	Initializes PEM (Phoenix Error Manager) data structures
C2h	Saves the current boot type into CMOS.
C2h	Invokes error logging function for all registered error handlers.
C3h	Checks the requested boot type.
C3h	Invokes error handler(s) for asserted errors.
C4h	Initializes (clears) the system error flags.
C4h	Installs the IRQ1 vector.
C5h	Marks the fact that BIOS is no longer in POST.
C6h	Installs console redirection module.
C7h	Removes the COM port address used by console redirection from BDA.
C8h	Performs A20 Test.
C9h	Checksum the entire BIOS and do a flash recovery if necessary.
CCh	Restores the memory configuration.
CDh	Reclaims console vectors after HW vectors initialized.
D1h	Initializes BIOS stack space for runtime usage.
D3h	Finds space for memory WAD and zero it.
D4h	Gets the CPU brand string.

Boot block checkpoint codes

Checkpoint Code[1]	Description
080h	Chipset initialization.
081h	Bridge initialization.
082h	CPU initialization.
083h	System timer initialization.
084h	System I/O initialization.
085h	Checks force recovery boot.
086h	Checks BIOS checksum.
087h	Enters BIOS.
088h	Initializes Multi-Processor if present.
089h	Sets Hugh Segments.
08Ah	Original Equipment Manufacturer (OEM) special initialization.
08Bh	Initializes PIC and DMA.
08Ch	Initializes memory type.
08Dh	Initializes memory size.
08Eh	Shadows Boot block.
08Fh	Initializes SMM.
090h	System memory test.
091h	Initializes interrupt vectors.
092h	Initializes RTC.
093h	Initializes Video.
094h	Initializes Beeper.
095h	Initializes Boot.
096h	Clears Huge Segments.
097h	Boots to the operating system.

[1] Checkpoint codes 088h – 097h are executed only when the force recovery jumper has been detected at Checkpoint 085h.

Intel memory initialization checkpoint codes

Checkpoint Code	Description
A0h	Detects GMCH device.
A1h	Progress meter inside routine: DDRProgRCOMP
A2h	Progress meter inside routine: DDRProgRCOMP
A3h	Progress meter inside routine: DDRProgRCOMP
A4h	Progress meter inside routine: DDRProgRCOMP
A5h	Progress meter inside routine: DDRProgRCOMP
A6h	Progress meter inside routine: DDRProgRCOMP
A8h	Progress meter inside routine: DDRProgRCOMP
AAh	Begin Common Initialization.
ABh	ProgDRADRBs
ACh	Init_Chipset_For_ECC
B0h	Program DRAM timing register.
B1h	Bad CAS latency.
C0h	Executes JEDEC init.
C1h	Executes JEDEC1 init.
D0h	Programs the Chipset ECC functionality.
D1h	Programs the CKE Tristate bits for unpopulated rows.
D2h	Programs the FSB Slew Rate Lookup Table.
D3h	Programs the DVO Slew Rate Lookup Table.
D5h	Programs the MMAC register.
D6h	Programs the MMAC register (completed)
E1h	Not all memory sticks present are DDR.
E2h	Not all memory sticks present are unbuffered.
E3h	No DIMMS are detected.
E4h	No DIMMs detected with good CAS latencies.
E5h	Too many performance grades detected.
E6h	Cannot find least common TRAS for all DIMMS present.
E7h	Cannot find least common TRP for all DIMMS present.
E8h	Cannot find least common TRCD for all DIMMS present.
E9h	Cannot determine highest common refresh rate for all DIMMs present.
EAh	A coding error has been detected.
EBh	Not all memory sticks present have the same sided-ness.
ECh	At least one DIMM stick present is in neither x8 nor x16 format.
EDh	Invalid memory configuration (generic).

Error message codes

Once the video is enabled, errors or warnings are sent to the video display as text messages shown in this table.

Note: These messages are always displayed unless the board is configured for quiet boot or headless operation.

Class	Number	Name
Disk errors	200h	ERR_DISK_FAILED
Keyboard errors	210h	ERR_KBD_STUCK
	211h	ERR_KBD_FAILED
	212h	ERR_KBD_KCFAIL
	213h	ERR_KBD_LOCKED
Video errors	220h	ERR_VIDEO_SWITCH
Memory errors	230h	ERR_SYS_MEM_FAIL
	231h	ERR_SHAD_MEM_FAIL
	232h	ERR_EXT_MEM_FAIL
	233h	ERR_MEM_TYPE_MIX
	234h	ERR_MEM_ECC_SINGLE
	235h	ERR_MEM_ECC_MULTIPLE
	236h	ERR_MEM_DECREASED
	237h	ERR_DMI_MEM_FAIL
POS/Timeout errors	240h	ERR_POS
CMOS errors	250h	ERR_CMOS_BATTERY
	251h	ERR_CMOS_CHECKSUM
Timer errors	260h	ERR_TIMER_FAILED
Real time clock errors are x70h	270h	ERR_RTC_FAILED
Invalid date time	271h	ERR_RTC_INV_DATE_TIME
Configuration errors	280h	ERR_CONFIG_FAILED
	281h	ERR_CONFIG_MEMORY
NVRAM errors	290h	ERR_NVRAM
COP errors	2A0h	ERR_COP
Diskette errors	2B0h	ERR_FLOPPYA_FAILED
	2B1h	ERR_FLOPPYB_FAILED
	2B2h	ERR_FLOPPYA_INCORRECT
	2B3h	ERR_FLOPPYB_INCORRECT
Load errors	2C0h	ERR_LOADED
Cache errors	2D0h	ERR_CACHE_FAILED

Class	Number	Name
I/O errors	2E0h	ERR_IO_ADDRESS
	2E1h	ERR_IO_COM
	2E2h	ERR_IO_LPT
	2E3h	ERR_IO_CONFLICT
	2E4h	ERR_IO_UNSUPPORTED
	2E5h	ERR_IO_IRQ
	2E6h	ERR_IO_IDE
	2E7h	ERR_IO_FDD
	2F0h	ERR_OTHER_CPUID
	2F1h	ERR_OTHER_BIST
	2F2h	ERR_OTHER_BSP
	2F3h	ERR_OTHER_AP
	2F4h	ERR_OTHER_CMOS
	2F5h	ERR_OTHER_DMA
	2F6h	ERR_OTHER_NMI
	2F7h	ERR_OTHER_FAILSAFE

INDUSTRY STANDARD REFERENCES C

Architecture	Specification	Location
Form factor	ATX Specification Version 2.2	www.formfactors.org/formfactor.asp
	ATX form factor	
Processor	Intel Core 2 Duo processor	www.intel.com/products/processor/core2duo/index.htm
	Intel Pentium Dual-Core processor	www.intel.com/products/processor/pentium_dual-core/index.htm
	Intel Celeron processor	www.intel.com/products/processor/celeron/index.htm
Chipset	Intel Q35 GMCH chipset	www.intel.com/products/chipsets/Q35_Q33/index.htm
	Intel ICH9/ICH9DO chipset	www.intel.com/design/chipsets/datashts/316972.htm
ACPI	Advanced Configuration and Power Interface (ACPI) Specification, Revision 3.0	www..acpi.info
DDR2 SO-RDIMM	*JEDEC Specification*	www.jedec.org
PCI	▪ *PCI Local Bus Specification Revision 2.3*: PCI SIG, March 29, 2002 ▪ *PCI Firmware Specification Revision 3.0*: PCI SIG, June 20, 2005	www.pcisig.com
PCI Express	*PCI Express Base Specification Revision 1.1*: PCI SIG, March 28, 2005	www.pcisig.com
PCI Express Card	*PCI Express Card Electromechanical Specification Revision 1.1*: PCI SIG, March 28, 2005	www.pcisig.com
SATA	*High Speed Serialized AT Attachment Revision 1.0a*: PIGMG, July 10, 2005	www.pcisig.com
SMBus	*System Management Bus Specification, Revision 1.1*: December, 1998	www.smbus.org
	System Management Bus BIOS Interface Specification Revision 1.0: February 15, 1995	www.smbus.org
USB	*Universal Serial Bus Specification Revision 2.0*: USB Implementers Forum, April 27, 2000	www.usb.org/developer