HDCC-708TX

(CEA-608/CEA-708 Encoder Card)

Multi-Purpose, HD/SD-SDI Closed Caption Card: Encoder, Bridge, and Transcoder

Configuration Guide

Software Version: V2.33

PIC Code Version: V1.11

Part Number 821142, Revision A

Wohler CONFIDENCE.

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CHAPTER 1
Setting the Switches

Introduction

Overview

Thank you for purchasing Wohler's HDCC card, a product that provides a variety of closed-captioning functions. This chapter explains how to install, set up, and use your card.

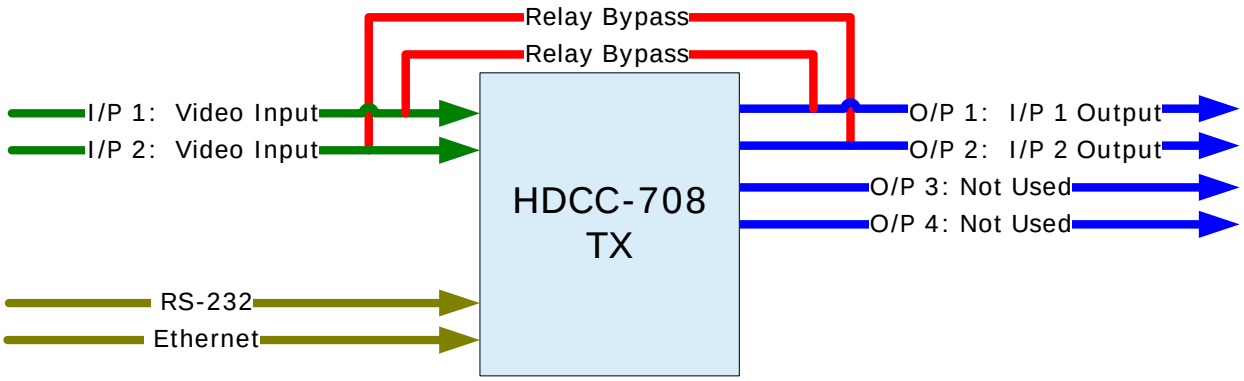
Topics

Basic Functionality

Inputs and Outputs

Figure 1–1 illustrates the basic inputs and outputs of the HDCC. In the event of a power failure, or when the system is powered down, the bypass relays engage and the outputs on O/P 1 and O/P 2 are identical to the input signals on I/P 1 and I/P 2 respectively.

Figure 1–1 I/O Functionality - No Power



Note: For Figure 1–1 above through Figure 1–6 on page 9, the illustrations depict either a Codan or Evertz rear panel adapter. The IRT has two RS-232 ports and no Ethernet port.

Processes

Encoding

Encoding allows the broadcaster to embed, or encode, caption text from a separate source into the SDI video/audio stream. For example, the SDI video/audio stream would come in on I/P 1, and the caption data would come in on the serial port from a PC on which an operator keys in the text of the caption data. Then the encoded SDI video/audio/data stream would come out on O/P 1. O/P 3 provides burnt-in captions, literally superimposing the text of the caption data on the video display. Refer to Figure 1–2 on page 4 for a summary of settings for Switch 1 (SW1).

Bridging / Transcoding

Bridging is the process of extracting closed captioning data from one SDI data stream and inserting it into another. For example, a video stream with embedded text would come in on I/P 1 and a clean video stream would come in on I/P 2. In this scenario, the HDCC card would copy the closed caption text data coming in on I/P 1 and embed it into the video stream of I/P 2. Note that the closed captioned text is not removed from the source input video stream. If the two signals are different, say SD and HD, then this scenario also exemplifies transcoding.

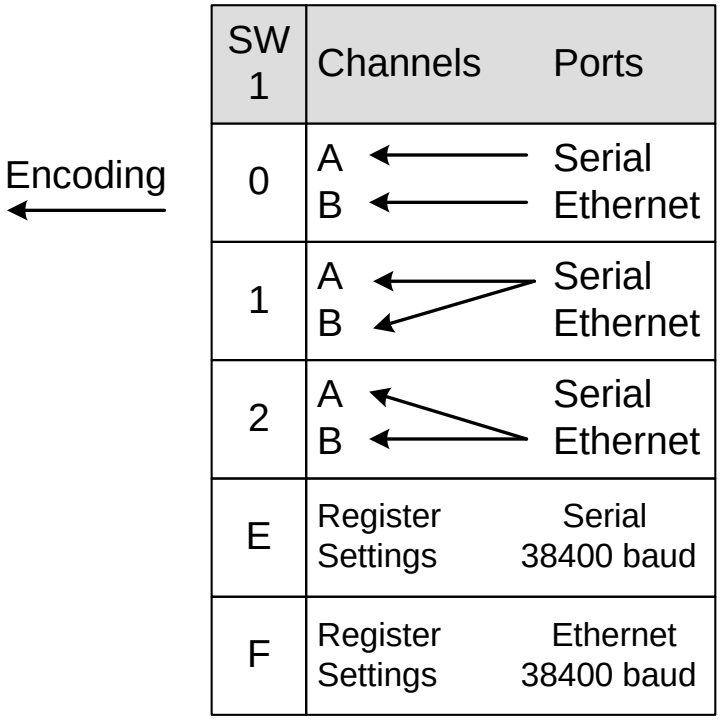
Table 1–1 Valid Switch Settings Switch 2 (SW2)

Switch 2	Bridge Operation
0	None
1	A→ B (both fields)
2	B→ A (both fields)
3	A→ B (Field 1)
4	B → A (Field 1)
5	A→ B (Field 2)
6	B → A (Field 2)
7 thru F	None

Ethernet and Serial Communications Summary

Figure 1–2 illustrates the direction of communications between the input channels (I/P 1 and I/P 2, aka Channel A and Channel B) and the serial and Ethernet ports, depending on the settings of SW1.

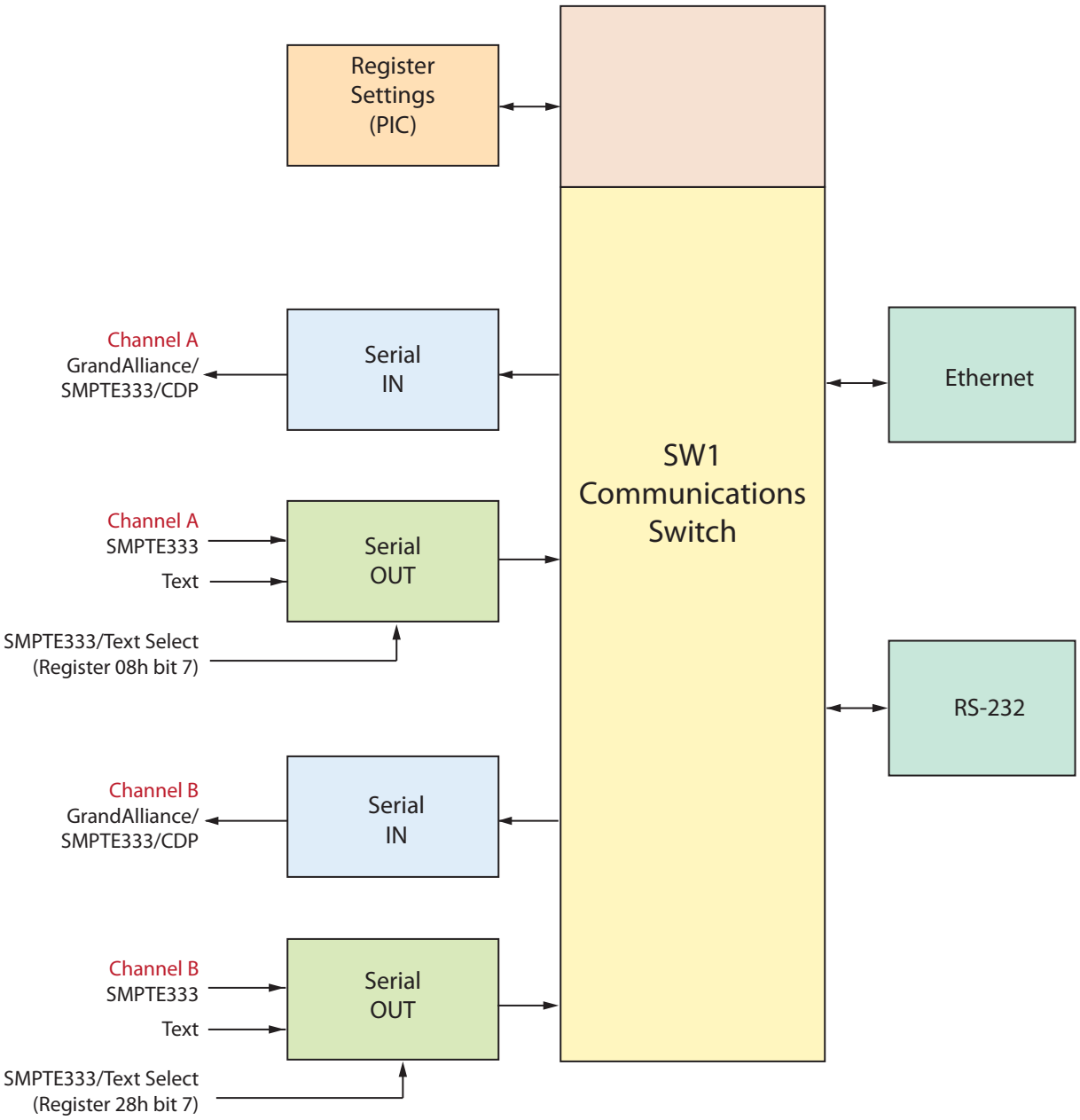
Figure 1–2 Serial and Ethernet Communications for SW1 Settings)



Communications Paths

Figure 1–3 below illustrates the serial and Ethernet communication as it relates to the SMPTE333 handshake settings in Registers 08h and 28h.

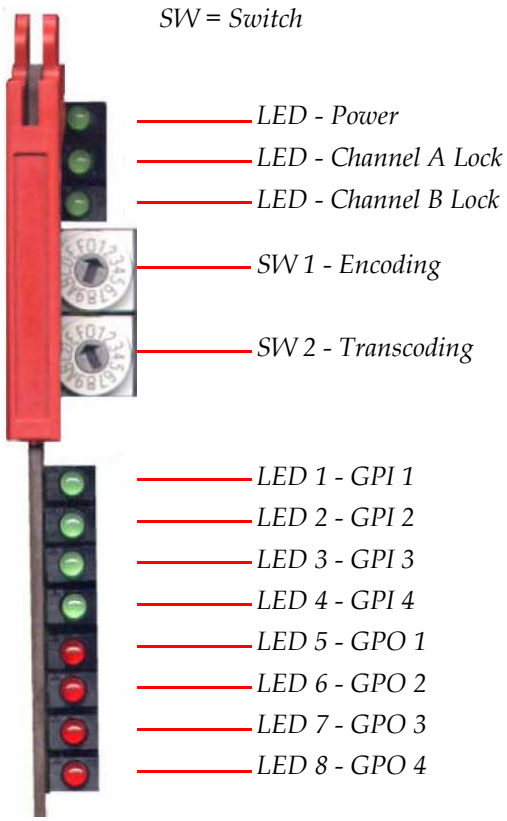
Figure 1–3 Serial and Ethernet Communications



Using the Card

Using the HDCC card amounts to little more than setting the switches, attaching the I/O cables, and connecting a PC through either an Ethernet or a serial port to encode or decode. (But a PC connection is not needed for bridging or transcoding.)

Figure 1–4 HDCC Front Panel



Note: The general purpose input and/or output (GPI/O) functions and pin outs are described in Connector Pin Assignments on page 46.

Refer to Register 0Eh for LED assignments: Figure 2–2 on page 16 and Table 2–5 on page 17.

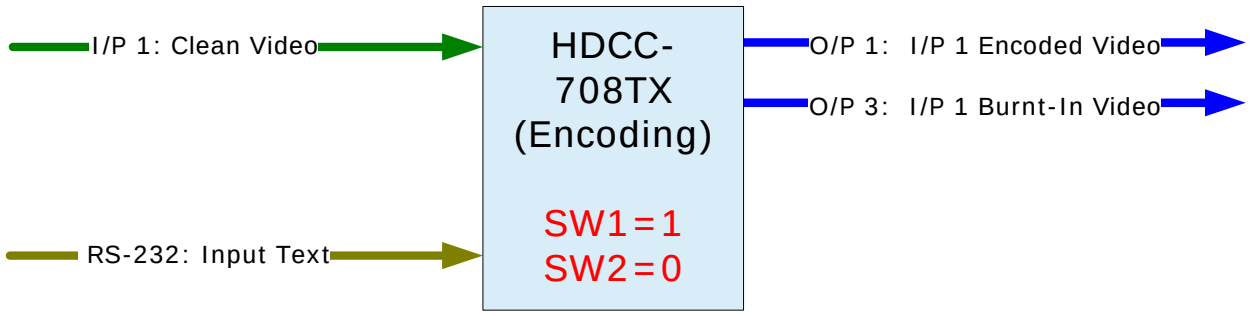
- **Switch 1 (SW 1)** controls whether the card is set to **encoding** (settings 0 through 2). This is the communications router.
- **Switch 2 (SW 2)** controls whether the card performs the **bridging** and **transcoding** functions (settings 1 to 6).

Also refer to Figure 1–2 on page 4.

Encoding

When encoding, a signal that comes in on I/P 1 goes out on the odd-numbered outputs, and a signal that comes in on I/P 2 goes out on the even-numbered outputs. See Figure 1–5 below.

Figure 1–5 Typical Scenario for Encoding Only



Example: This simple example demonstrates the encoding feature.

I/P 1: Input clean video stream.

I/P 2: NC

O/P 1: Output video stream with encoded closed captions.

O/P 2: NC

O/P 3: Monitor video output with burnt-in (OSD) decoded captions.

O/P 4: NC

Serial: Closed caption data input.

Ethernet: NC

1. Connect a clean video source to I/P 1.
2. Connect an output cable to O/P 1.
3. Connect a video monitor to O/P 3.
4. Connect a data source for closed captioned text to the RS-232 port.

Note: To use the Ethernet port as a virtual serial port, refer to Appendix A of the *Installation Guide* (PN 821135) to download, install, and configure the Ethernet connectivity application.

5. Set SW 1 according the port through which you will insert the closed caption text. For our example, set SW 1 to 1. See Table 1–2 below a list of additional options.

Table 1–2 Switch 1 Settings - Encoding Only

SW 1	Insert Text From
0	Inserts captions on I/P 1 from the RS-232 port. Inserts captions on I/P 2 from the Ethernet port.
1	Inserts captions on I/P 1 and on I/P 2 from the RS-232 port.
2	Inserts captions on I/P 1 and on I/P 2 from the Ethernet port.

6. Set SW 2 to 0.

7. Launch the closed caption text insertion application and verify that you have connected to the HDCC using the correct com port at the correct baud rate.

8. Begin sending text from your closed caption text insertion application.

Providing the HDCC card is locked on an video signal, as soon as it receives closed caption data, it will immediately encode this closed caption data into the output video streams O/P1 and O/P 3.

Note: You can repeat the previous steps 1 through 5 (using I/P 2, O/P 2, and O/P 4 in Steps 1 through 3 respectively) to encode a second video stream with either the same or a different text source/communications port since the HDCC is a dual-channel card. Moreover, the signals need not be synchronous.

Important: If you have difficulty getting the correct results on the ouput connectors/ports, you may need to modify some of the register settings to fit your particular installation. Refer to Chapter 2: Setting the Engineering Registers on page 11 for more information.

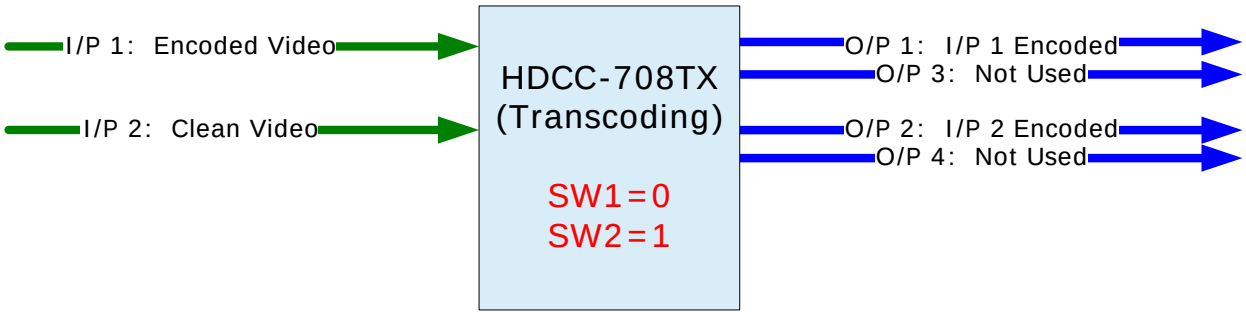
Bridging

Bridging means that encoded closed captions are copied from one video stream to the other, *transcoding* them on-the-fly if the two video streams are of a different format.

Note: It is not necessary to match the resolutions and/or refresh rates when using multiple inputs, with one exception: the target video frame rate must match or be faster than the source video stream.

For example, you can bridge and transcode from a SD-50Hz to a HD-60Hz signal but not the other way around.

Figure 1–6 I/O Functionality - Bridging Only



1. Connect the encoded video signal to I/P 1.
2. Connect the clean video signal to I/P 2.
3. Connect the output cables to O/P 1 and O/P 2.
4. Connect monitor cables to O/P 3 and/or O/P 4.
5. For our example, set SW 2 to 1.

As soon as the HDCC card is locked on the two video signals, it should begin to bridge and if necessary transcode closed caption data from channel A (I/P 1) to channel B (O/P 2 and O/P 4).

Important: If you have difficulty getting the correct results on the ouput connectors/ports, you may need to modify some of the register settings to fit your particular installation. Refer to Chapter 2: Setting the Engineering Registers on page 11 for more information.

CHAPTER 2
Setting the Engineering Registers

Introduction

Overview

This chapter explains how to access the engineering registers to configure the HDCC card for your particular system.

Topics

Connecting to the Card

To perform this procedure you will need:

- A PC or laptop with a serial port and/or Ethernet port
- Either of the following:
  - A serial cable (connected from the serial port of the PC to the serial port on the HDCC). Refer to Accessing the Configuration on page 12 for more information.
  - An Ethernet cable (connected to the Ethernet ports of the HDCC card and the PC)

Accessing the Configuration

The card has a number of registers to allow easy configuration of various card parameters that can be accessed from both the RS-232 interface and the Ethernet interface.

Note: An active SDI (SD or HD) signal connected to one of the input interfaces (I/P-1 or I/P-2) is required to activate the Ethernet port.

To access the configuration registers:

1. Determine whether you want to access the engineering menu from the Ethernet port or from the RS-232 port.
2. Depending how you will access the menu, turn SW 1 to either E or F according to Table 2–1 below.

Table 2–1 Switch 1 Settings - Encoding

SW 1	Insert Text From
E	Access engineering menu through RS232 port.
F	Access engineering menu through Ethernet port.

3. Connect the serial or Ethernet cable from the host computer's port to the port on the rear panel adaptor.

   Note: IRT adaptors do not provide an Ethernet port.

4. Launch your **HDCCRegEdit** program. Refer to the *HDCCRegEdit Guide* (PN 821174) for instructions for using this application.

5. Verify that your communication settings are 38400, n, 8, 1.

Modifying the Register Settings

Table 2–2 Register Table Summary

Channel		Description
A	B	
00h	20h	HD Line for CEA-708 Insertion
01h	21h	Not Used
02h	22h	SD Line for CEA-608 Insertion
03h	23h	Not Used
04h	24h	Not Used
05h	25h	Not Used
06h	26h	Not Used
07h	27h	Not Used
08h	28h	Transmission Features
09h	29h	Reserved for future use
0Ah	2Ah	SD Line for GPI Data Insertion and Decoding
0Bh	2Bh	HD Line for GPI Data Insertion and Decoding
0Ch	2Ch	Not Used
0Dh	2Dh	Not Used
0Eh		GPI LED Settings
0Fh	2Fh	GPI Rx/Tx Polarity Control
10h	30h	Special Features 2
11h	31h	Reserved for future use
12h	32h	GPI Data Insertion Control and Encoder Timeout
13h	33h	GPI Mapping for Tx
14h	34h	Reserved for future use
15h	35h	Not Used
16h	36h	Not Used
17h	37h	Not Used
18h	38h	Not Used
19h	39h	Not Used
1Ah	3Ah	Not Used
1Bh	3Bh	Not Used
1Ch	3Ch	Not Used
1Dh	3Dh	Not Used
1Eh	3Eh	Not Used
1Fh	3Fh	Not Used
FEh		GPO 1 and 2 Mapping
FFh		GPO 3 and 4 Mapping

Table 2–3 Register Setting Descriptions

Ch A Reg #	Ch B Reg #	Description
00h	20h	HD Line for CEA-708 Insertion
02h	22h	SD Line for CEA-608 Insertion

Figure 2–1 Registers 08h and 28h (Transmission Features)

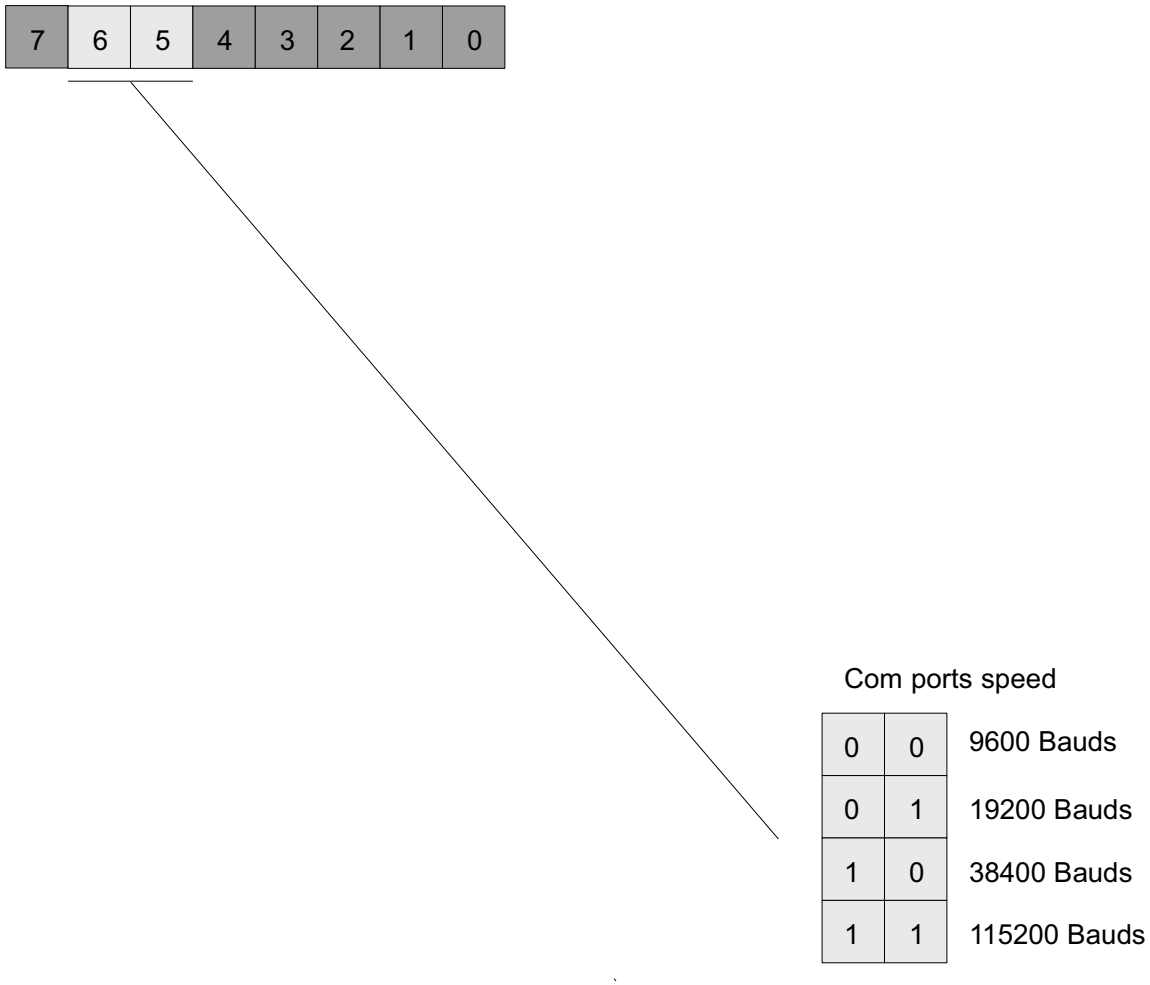
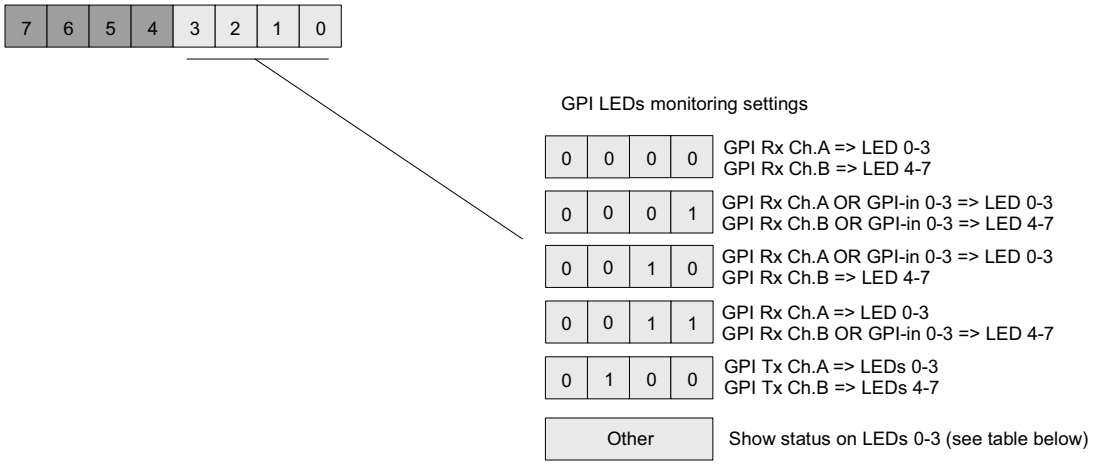


Table 2–4 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>08h</td><td>28h</td><td>Transmission Features
Min: N/A – Max: N/A
<table><tr><th>Bit(s)</th><th>Function</th></tr><tr><td>7</td><td>Enable SMPTE 333 Protocol:
0 = Disabled
1 = Enabled</td></tr><tr><td>6:5</td><td>Com Port Speed:
00 = 9600 baud
01 = 19200 baud
10 = 38400 baud
11 = 115200 baud</td></tr></table></td></tr>
<tr><td>0Ah</td><td>2Ah</td><td>SD Line for GPI Data</td></tr>
<tr><td>0Bh</td><td>2Bh</td><td>HD Line for GPI Data</td></tr>
</table>

Figure 2–2 Register 0Eh ONLY —Register 2Eh Not Used



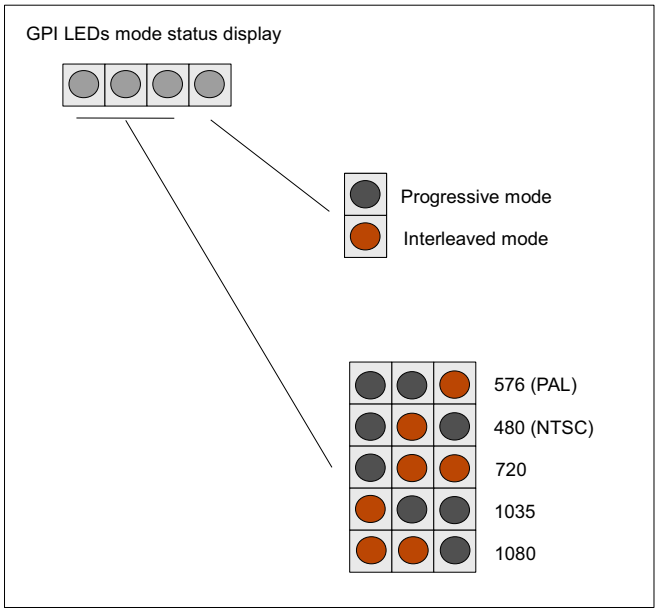


Table 2–5 Register Setting Descriptions

<table>
<tr><th>Ch A & Ch B</th><th>Description</th></tr>
<tr><td>0Eh</td><td>
GPI LED Settings
Min: N/A – Max: N/A
<table>
<tr><th>Bits</th><th>Function</th></tr>
<tr><td>0:3</td><td>
<table>
<tr><th colspan="2">GPI 4</th></tr>
<tr><th>LED</th><th>Description</th></tr>
<tr><td>0000</td><td>GPI Rx Ch A on LEDs 0 to 3
GPI Rx Ch B on LEDs 4 to 7</td></tr>
<tr><td>0001</td><td>GPI Rx Ch A OR GPI-In 0 to 3 on LEDs 0 to 3
GPI Rx Ch B OR GPI-In 0 to 3 on LEDs 4 to 7</td></tr>
<tr><td>0010</td><td>GPI Rx Ch A on LEDs 0 to 3
GPI Rx Ch B OR GPI-In 0 to 3 on LEDs 4 to 7</td></tr>
<tr><td>0011</td><td>GPI Rx Ch A on LEDs 0 to 3
GPI Rx Ch B OR GPI-In 0 to 3 on LEDs 4 to 7</td></tr>
<tr><td>0100</td><td>GPI Tx Ch A on LEDs 0 to 3
GPI Tx Ch B on LEDs 4 to 7</td></tr>
<tr><td>Else</td><td>Show status on LEDs 0 to 3. See tables below.</td></tr>
</table>
<table>
<tr><th>LED</th><th>LED 4 Description</th></tr>
<tr><td>0</td><td>Interleaved Mode</td></tr>
<tr><td>1</td><td>Progressive Mode</td></tr>
</table>
<table>
<tr><th rowspan="2">Description</th><th colspan="3">LED</th></tr>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td>576 (PAL)</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>480 (NTSC)</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>720</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1035</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Not Used</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1080</td><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>4:7</td><td>Not Used</td></tr>
</table>
</td></tr>
</table>

Figure 2–3 Registers 0Fh and 2Fh

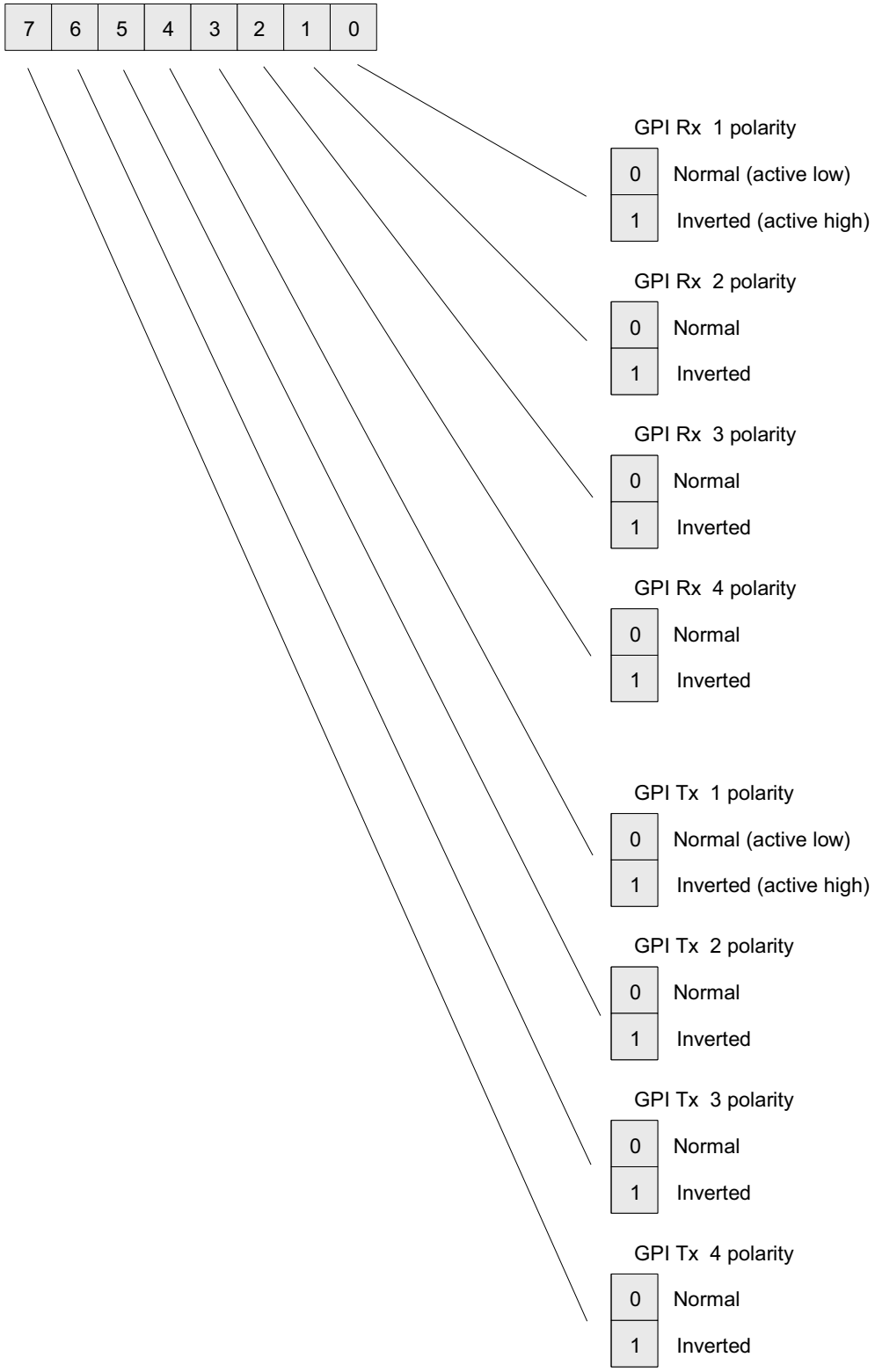


Table 2–6 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>0Fh</td><td>2Fh</td><td>
GPI Tx/Rx Polarity
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>0</td><td>GPI Rx 1</td><td rowspan="8">0 = Normal (Active Low)
1 = Inverted (Active High)</td></tr>
<tr><td>1</td><td>GPI Rx 2</td></tr>
<tr><td>2</td><td>GPI Rx 3</td></tr>
<tr><td>3</td><td>GPI Rx 4</td></tr>
<tr><td>4</td><td>GPI Tx 1</td></tr>
<tr><td>5</td><td>GPI Tx 2</td></tr>
<tr><td>6</td><td>GPI Tx 3</td></tr>
<tr><td>7</td><td>GPI Tx 4</td></tr>
</table>
</td></tr>
</table>

Figure 2–4 Registers 10h and 30h

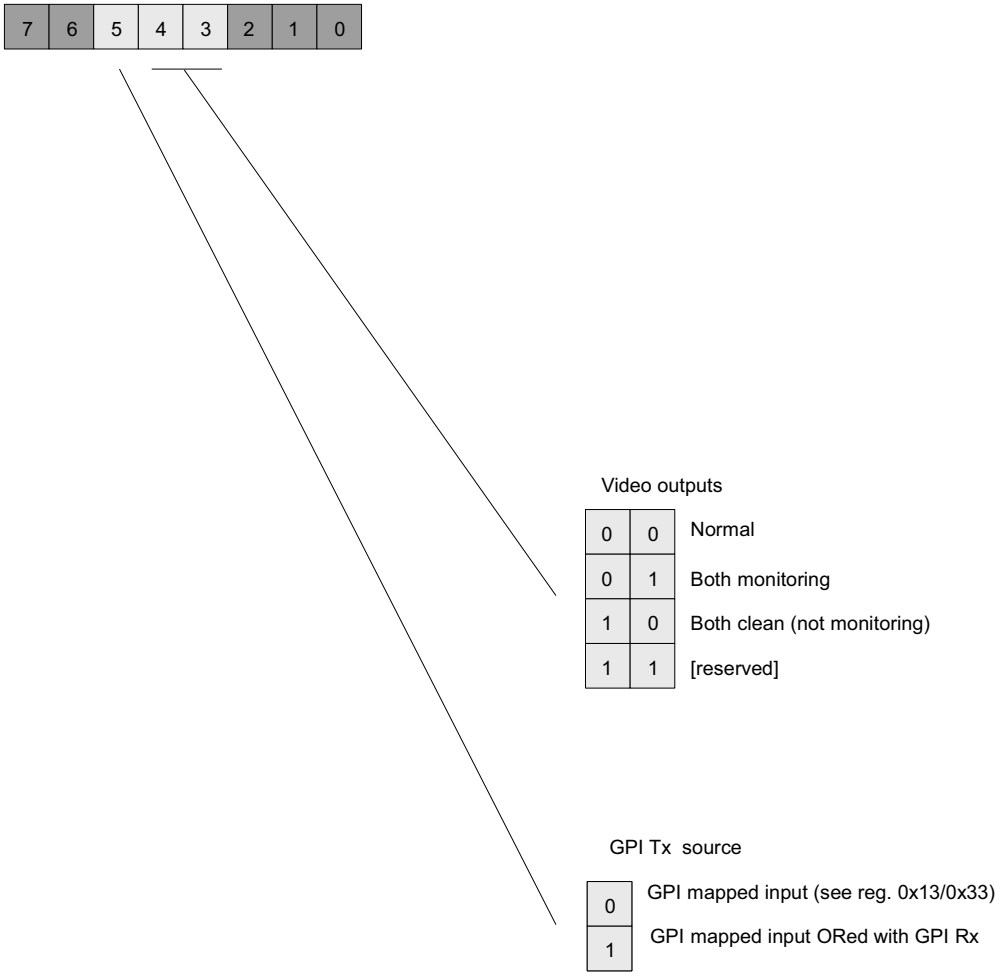


Table 2–7 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>10h</td><td>30h</td><td>
Special Features—2
Min: N/A – Max: N/A

This register controls miscellaneous functions on the card including the video outputs.
<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>3:4[a]</td><td>Video Output Mode:
00 = Normal
01 = Both outputs set to monitoring
10 = Both outputs are clean
11 = Not Used</td></tr>
<tr><td>5</td><td>GPI Tx Source:
0 = GPI mapped input (See Registers 13h and 33h.)
1 = GPI mapped input ORed with GPI Rx</td></tr>
</table>
a Normal (default) = Monitoring O/Ps are 3 and 4; Clean O/Ps are 1 and 2
Monitoring = Burned-in captions on all O/Ps
Clean = No burned-in captions on any O/Ps
</td></tr>
</table>

Figure 2–5 Registers 11h and 31h

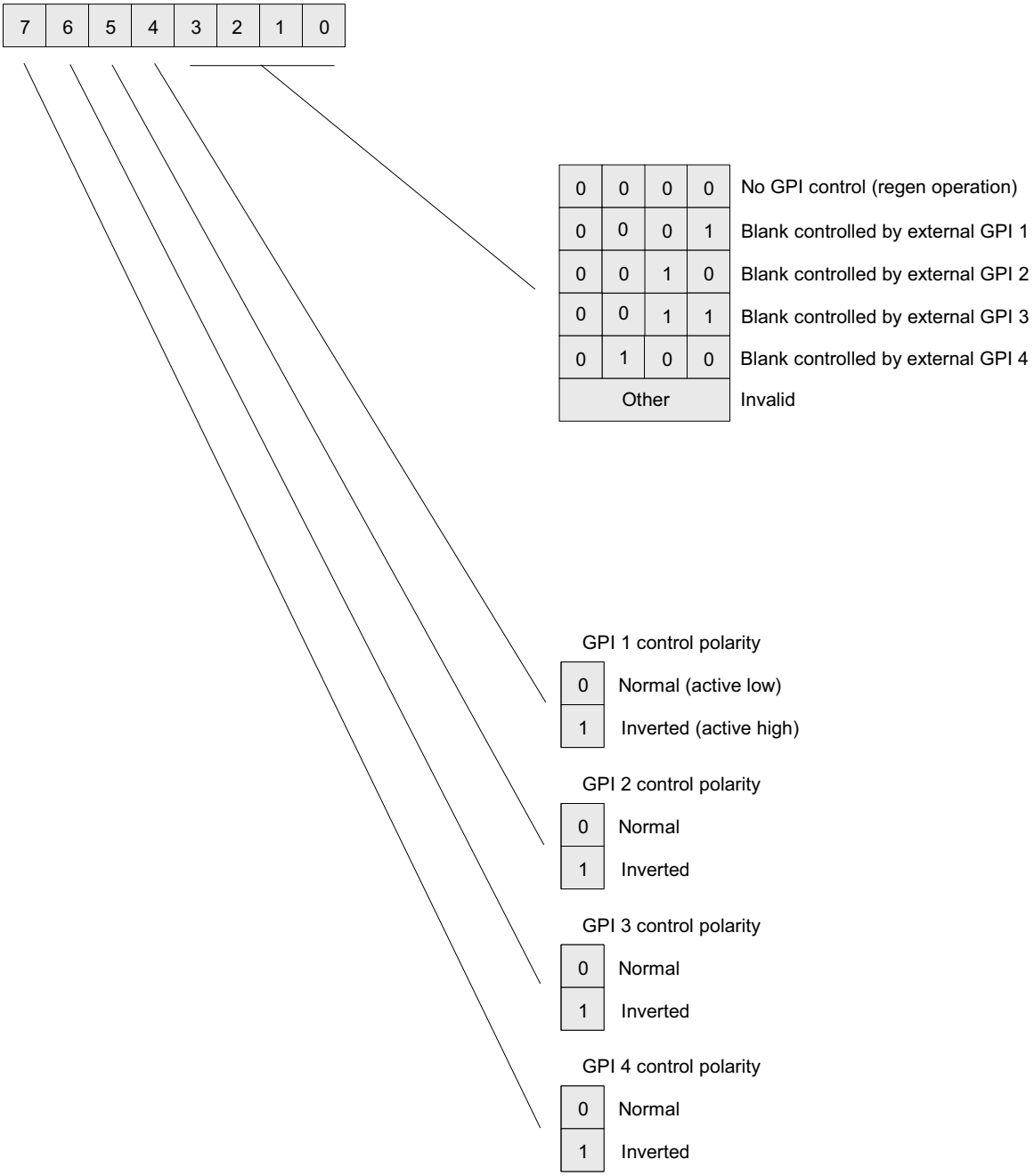


Table 2–8 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>11h</td><td>31h</td><td>
Regen/Blank Control with External GPI
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Value</th><th>Blank Controlled by...</th></tr>
<tr><td rowspan="5">0:3</td><td>0000</td><td>GPI Control (Regen Operation)</td></tr>
<tr><td>0001</td><td>External GPI 1</td></tr>
<tr><td>0010</td><td>External GPI 2</td></tr>
<tr><td>0011</td><td>External GPI 3</td></tr>
<tr><td>0100</td><td>External GPI 4</td></tr>
</table>
<table>
<tr><th>Bit(s)</th><th>Polarity Control</th><th>Function</th></tr>
<tr><td>4</td><td>GPI 1</td><td rowspan="4">0 = Normal (Active Low)
1 = Inverted (Active High)</td></tr>
<tr><td>5</td><td>GPI 2</td></tr>
<tr><td>7</td><td>GPI 3</td></tr>
<tr><td>7</td><td>GPI 4</td></tr>
</table>
</td></tr>
</table>

Figure 2–6 Registers 12h and 32h

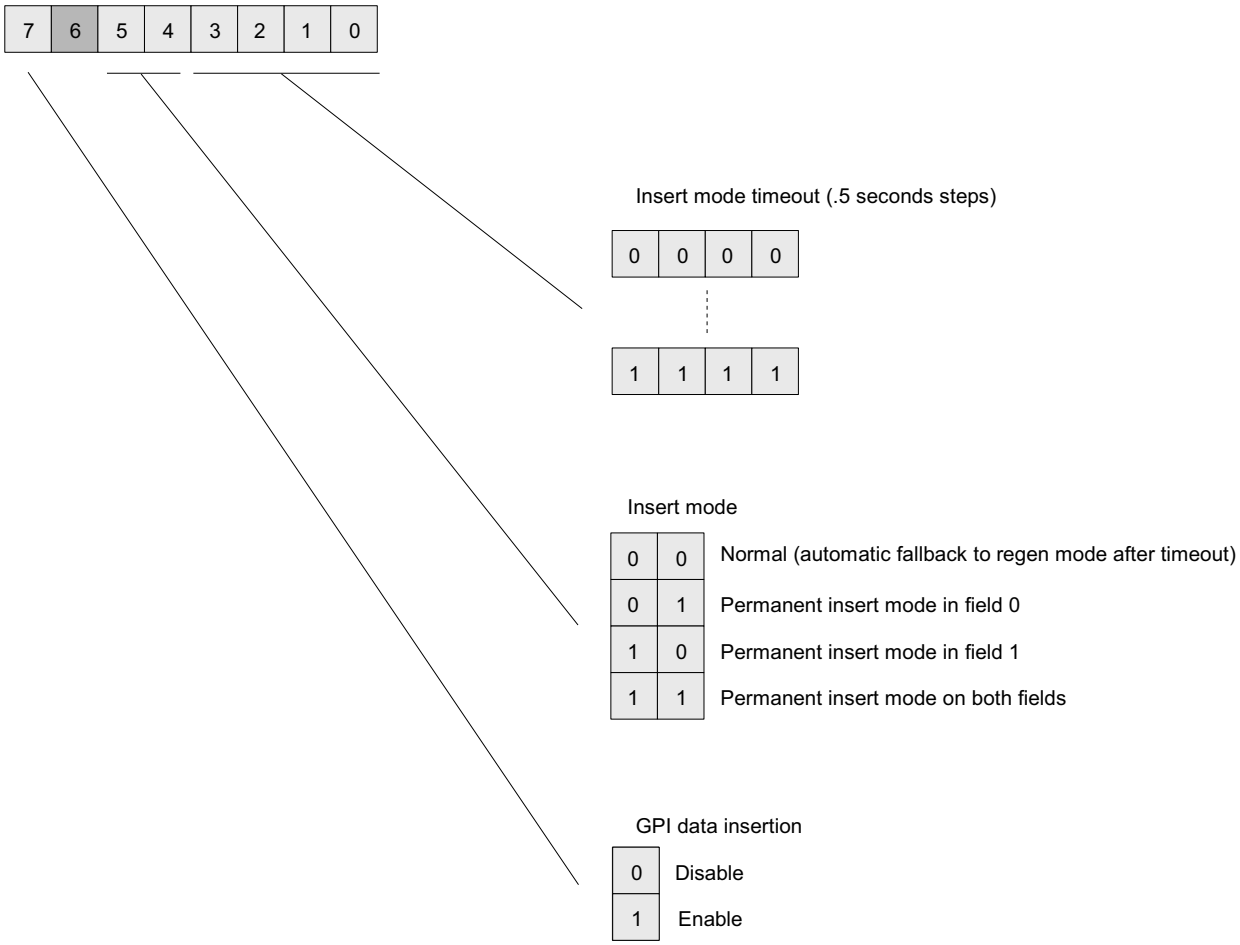


Table 2–9 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>12h</td><td>32h</td><td>
GPI Insertion Control and Insert Mode Timeout
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>0:3</td><td>Insert Mode Time Out (0.5 second intervals):
0000 = 0 seconds
0001 = 0.5 seconds
0010 = 1.0 seconds
.
.
.
1111 = 7.5 seconds</td></tr>
<tr><td>4:5</td><td>Time Out:
00 = Normal (automatic fall back to regen mode after timeout)
01 = Permanent insert mode in field 0
10 = Permanent insert mode in field 1
11 = Permanent insert mode in both fields</td></tr>
<tr><td>6</td><td>Not Used</td></tr>
<tr><td>7</td><td>GPI Data Insertion:
0 = Off
1 = On</td></tr>
</table>
</td></tr>
</table>

Figure 2–7 Registers 13h and 33h

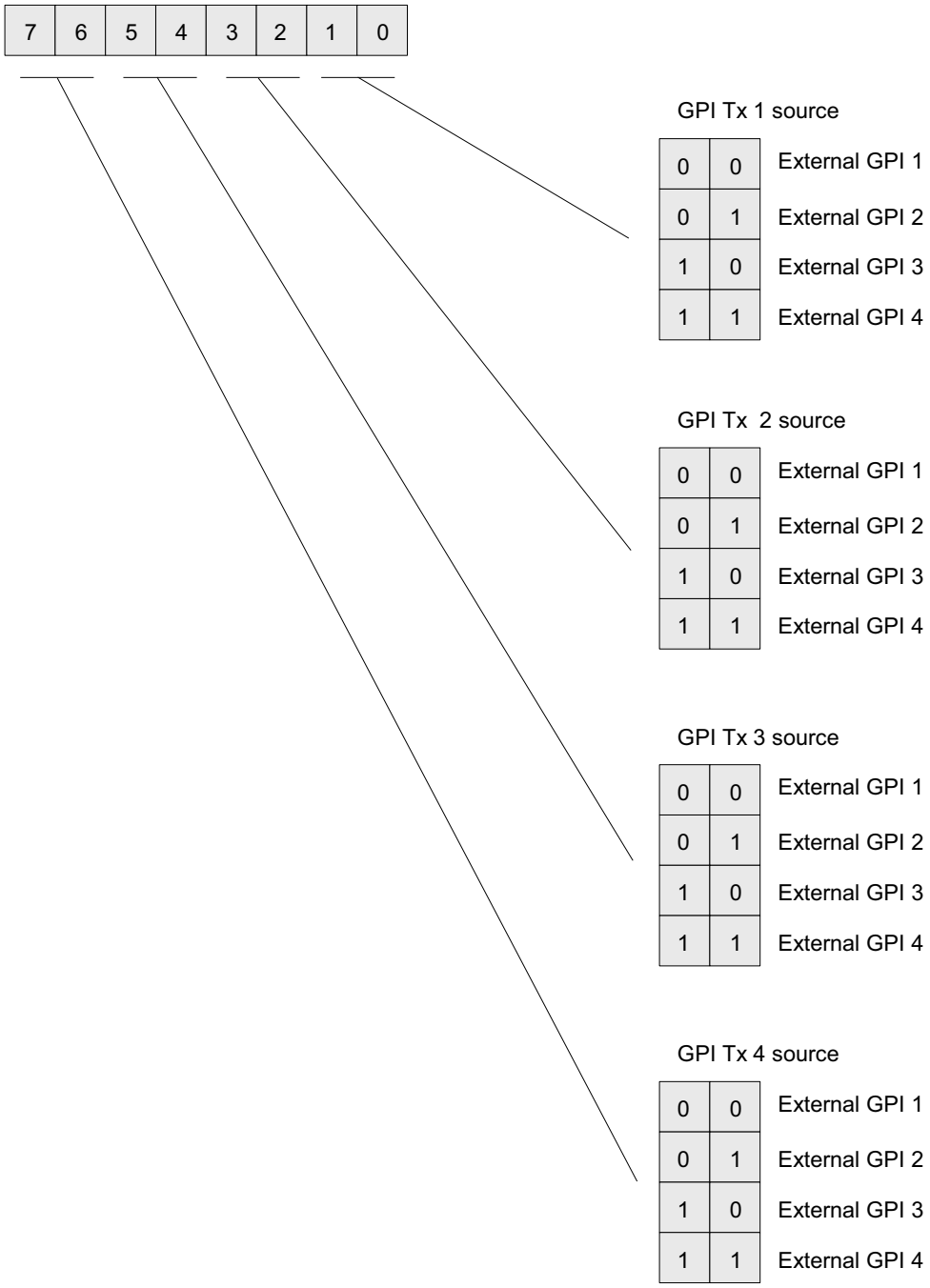


Table 2–10 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>13h</td><td>33h</td><td>GPI Mapping for Tx
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>GPI Tx Source</th><th>Function</th></tr>
<tr><td>0:1</td><td>1</td><td rowspan="4">External GPIs:
00 = GPI 1
01 = GPI 2
10 = GPI 3
11 = GPI 4</td></tr>
<tr><td>2:3</td><td>2</td></tr>
<tr><td>4:5</td><td>3</td></tr>
<tr><td>6:7</td><td>4</td></tr>
</table></td></tr>
</table>

Figure 2–8 Register FEh

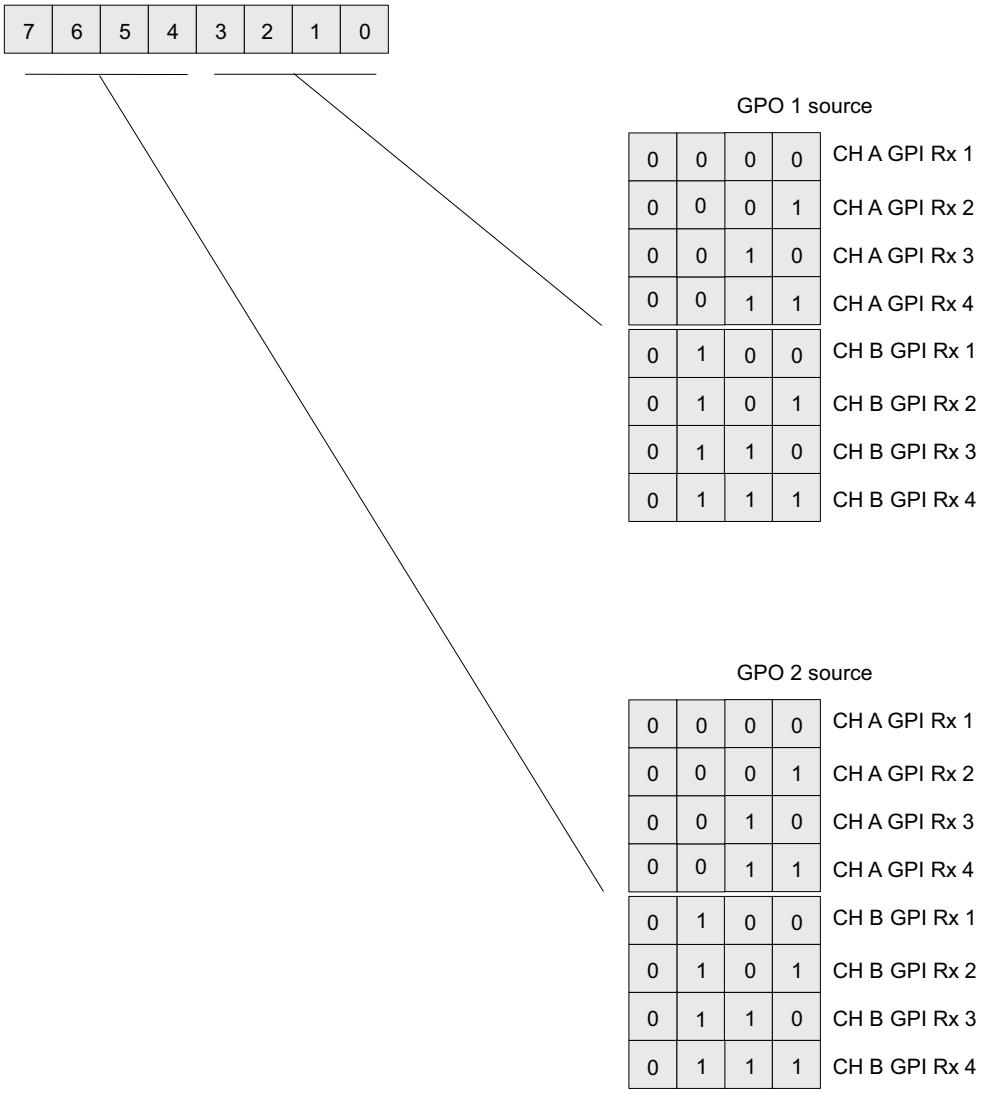


Table 2–11 Register Setting Descriptions

<table>
<tr><th>Both Channels</th><th>Description</th></tr>
<tr><td>FEh</td><td>
GPO 1 and 2 Source
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>0:3</td><td>GPO 1 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
<tr><td>4:7</td><td>GPO2 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
</table>
</td></tr>
</table>

Figure 2–9 Register FFh

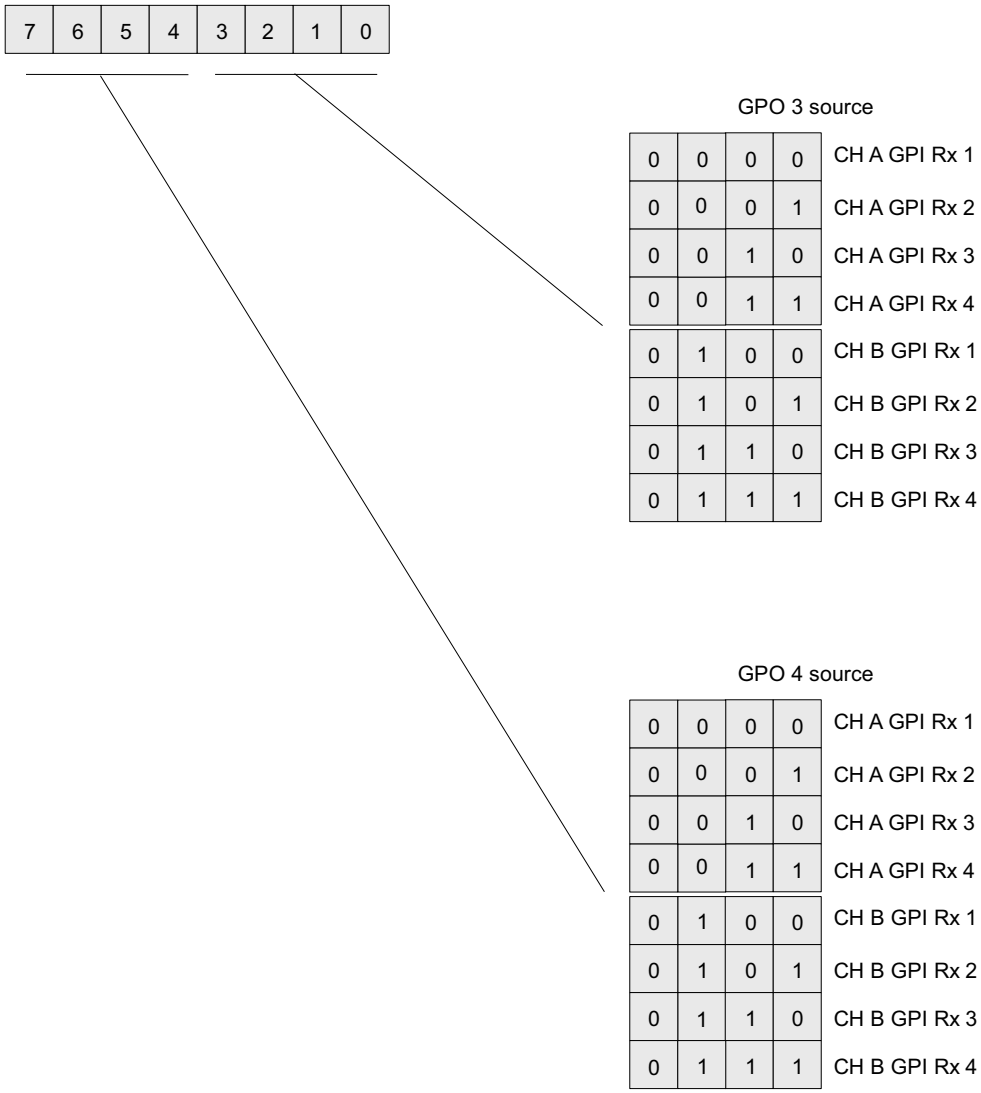


Table 2–12 Register Setting Descriptions

<table>
<tr><th>Both Channels</th><th>Description</th></tr>
<tr><td>FFh</td><td>GPO 3 and 4 Source
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>0:3</td><td>GPO 3 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
<tr><td>4:7</td><td>GPO 4 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
</table></td></tr>
</table>

CHAPTER 3
Using the General Purpose Inputs/Outputs

Introduction

Overview

This chapter describes the functionality of the GPI/O connectors on the adaptors.

Topics

Functionality

The GPI interface allows the user to encode contact closure triggers into a HD or SD video stream frame accurately. The encoded data uses a proprietary algorithm designed to withstand severe degradation and prevent false triggering or releasing of GPIs. Error checking information is embedded within the GPI data stream which accomplishes this task and is far more advanced than simple CRC.

Typical triggers that users can encode from automation include (but are not limited to:

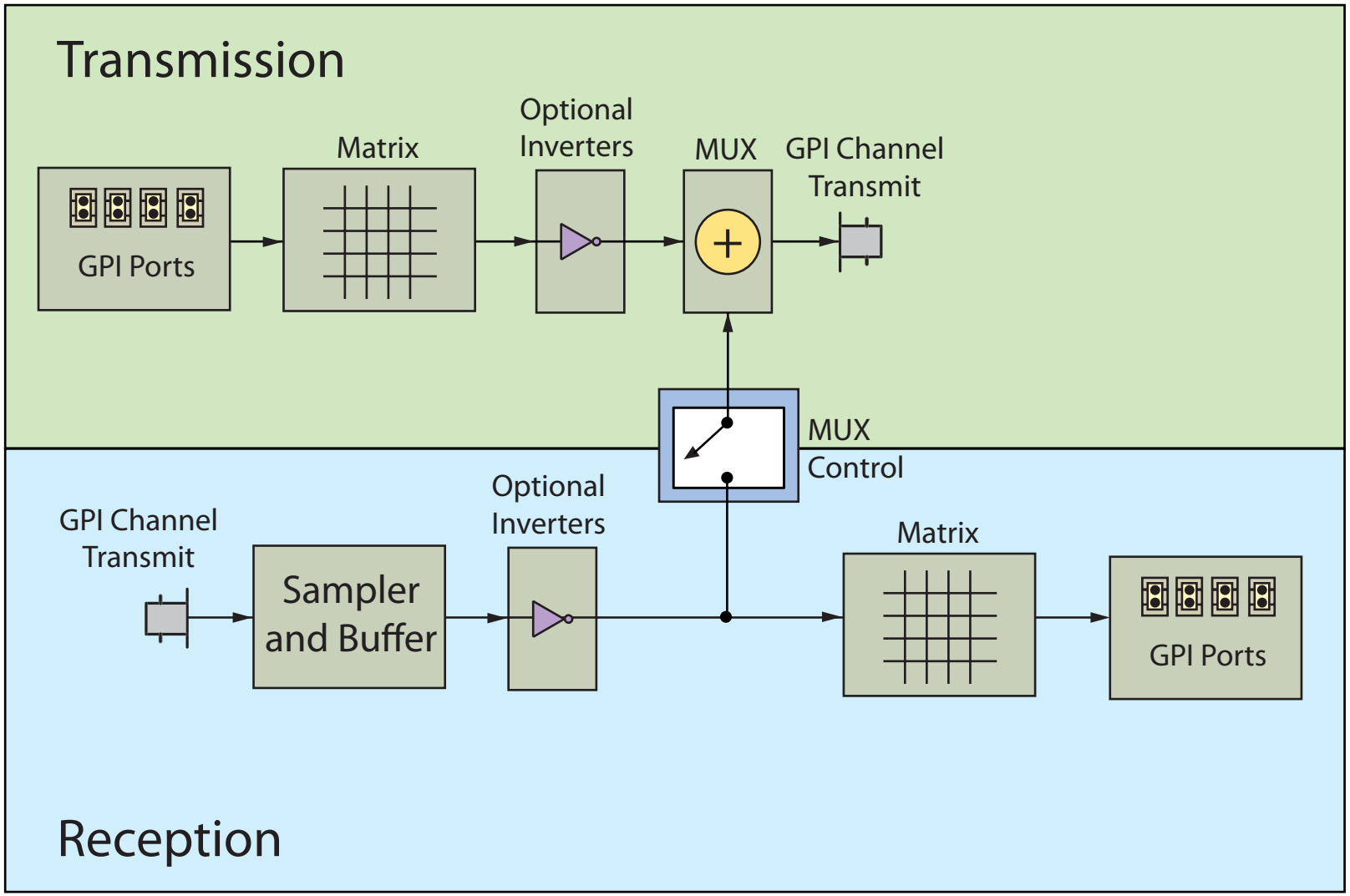
- ARC switching
- Commerical cue triggers (more accurate than the antiquated cue tone system)
- Machine control
- Regional commercial insertion cards

Typically the GPI data is encoded on Line 13 for both the HD-SDI signals and the SD-SDI signals. However, the HDCC is flexible enough to allow you to assign the lines on which you want the GPI data. See Modifying the Register Settings on page 13 for details.

You can also use the GPI interface to control other operational aspects of the card.

Figure 3–1 on page 35 illustrates the GPI-I/O signal flow through the HDCC. For our purposes, a GPI Input (often simply called a GPI) is an input signal to the HDCC card supplied by the user through the physical GPI-I/O port that can activate certain modes in the HDCC card, and/or can be encoded onto the outgoing SDI video stream to notify downstream equipment of some condition, event, or command. A GPI Output (often simply called a GPO) is a signal the HDCC card receives on the incoming SDI video stream that is output to the physical GPI-I/O port to signify some condition, event, or command generated by upstream equipment.

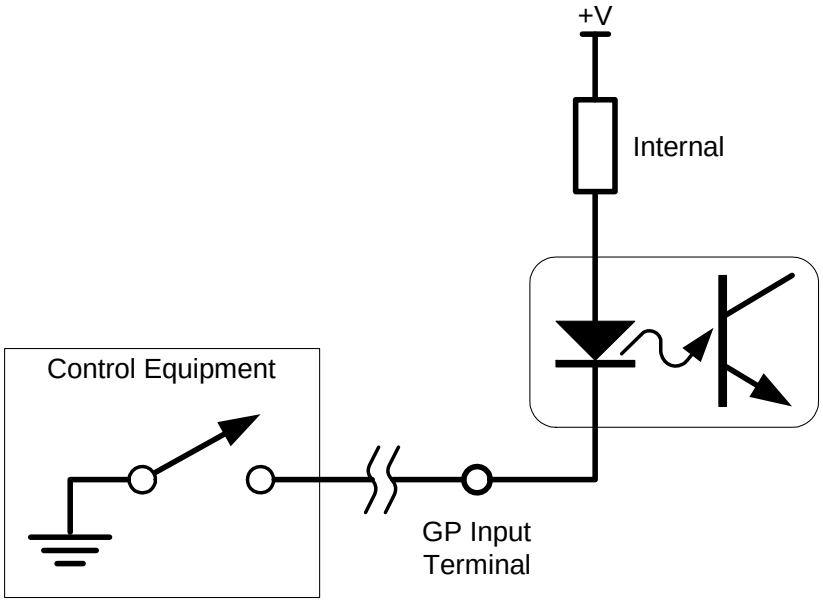
Figure 3–1 GPI/O Functional Diagram



GPIs

The GPI inputs are designed to be asserted by switching the closures to ground. Asserting a GPI input will result in that input state being encoded on the appropriate line of the video signal and/or activate the required function.

Figure 3–2 Input Diagram



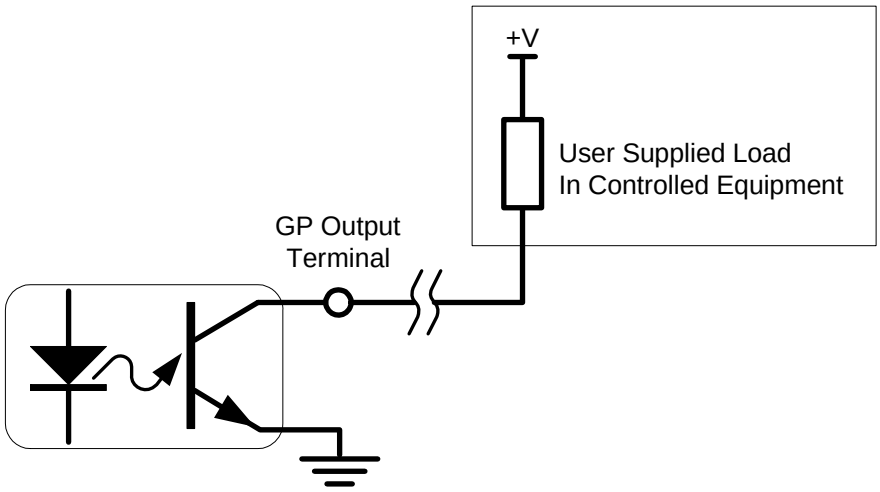
GPOs

If the incoming SDI data stream contains GPI data on the appropriate line of the video signal, the corresponding GPI output on the card will be activated. The GPI output is asserted when its voltage is high.

Important: The GPI outputs are optically isolated and "open collector" so the user must provide the appropriate pull-up resistor for each GPI output. See Figure 3–3 below.

The HDCC provides four GPOs. (See Connector Pin Assignments on page 46 in Chapter 4 for connectivity.)

Figure 3–3 Output Diagram



GPI/O Polarities

You can control the polarities of the encoded GPIs, both at the receiving stage (Rx) and at the encoding stage (Tx).

GPI Encoded Polarity (Rx)

Channel	Register	Bit(s)	Values
A	0Fh	0 through 3	See Table 3–1 below.
B	2Fh	0 through 3	

The polarity settings are listed in Table 3–1 below.

Table 3–1 GPI Assertion Polarity

Bits	GPI	Active Low (default)	Active High
0	GPI-1	0	1
1	GPI-2	0	1
2	GPI-3	0	1
3	GPI-4	0	1

GPI Encoded Polarity (Tx)

Channel	Register	Bit(s)	Values
A	0Fh	4 through 7	See Table 3–2 below.
B	2Fh	4 through 7	

You can set the polarity of the GPI as encoded on the data stream as shown in Table 3–2 below.

Table 3–2 Register 0Fh and 2Fh: Bits 4 through 7

Bits	GPI	Active Low (default)	Active High
4	GPI-1	0	1
5	GPI-2	0	1
6	GPI-3	0	1
7	GPI-4	0	1

Enabling/Disabling GPI Transmission

Channel	Register	Bit(s)	Values
A	12h	7	0=Disable 1=Enable
B	22h	7	

The HDCC can be configured to enable or disable transmission of GPI data by setting bit 7 of register 12h for Channel A, or 32h for Channel B.

CHAPTER 4
Features and Specifications

Introduction

Overview

This chapter explains the features of the HDCC closed caption card and details all of the specifications.

Topics

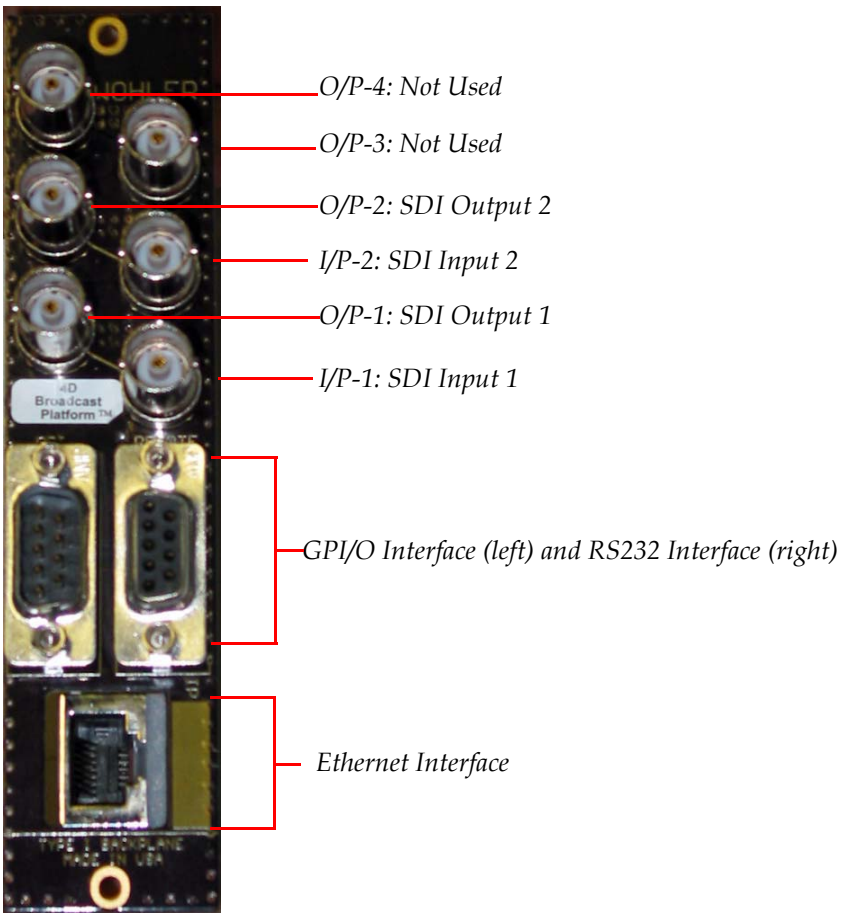
Features

Description

Hardware

The image and call outs in Figure 4–1 provide a reference for the detailed interface descriptions provided below.

Figure 4–1 Codan Adapter and Interface Layout



BNC Interfaces

- **I/P-1 and I/P-2:** These interfaces (Channel A and Channel B, respectively) accept SDI channel inputs that conform to the SMPTE 259M standard for SD and SMPTE 292M standard for HD.

- **O/P-1 and O/P-2:** These SDI outputs provide closed caption data encoded video signal. They are relay bypassed on power failure, card removal, or card failure.

- **O/P-3 and O/P 4:** Not Used.

GPI Interface

Four GPI inputs and four GPI outputs are provided for products that use the GPI I/O functionality. All GPI I/Os are opto-coupled through the card.

Ethernet and Serial Interfaces

The ethernet interface (100BT) and the serial (RS-232) interfaces receive caption data into the card when used as closed caption inserters.

Software

The HDCC is a dual-channel card that delivers closed captioned data and performs a variety of other tasks related to closed captioning or GPI transmission. The card receives closed caption data through an RS-232 serial port and/or an ethernet port. The three functions of the card are:

- HD/SD Closed Caption Encoding/Inserting

- HD/SD Closed Caption Bridging and Transcoding

- GPI-I/O Insertion and Extraction

Functionality

The HD/SD Closed-Caption Inserter (Encoding)

The HD/SD-SDI closed caption inserter can encode two independent SD-SDI sources with identical closed caption data, or two independent HD-SDI sources with unique data where the signal is intended to be used for different markets. The two signals do not need to be synchronous.

The HD/SD Bridge and Transcoder (Bridging and Transcoding)

The SD/HD bridge copies encoded closed caption data from one video channel to the other, transcoding it if required (SD to HD or HD to SD).

Connectivity

Interfaces

A serial port (RS-232) and an ethernet interface (adaptor-dependent) are provided to insert closed caption data. Either interface can be used to control one or both channels of the card as required. Captioning workstations that use GrandAlliance or CDP protocols can be connected to the card through either interface to allow the encoding of closed captions. The Ethernet interface allows you to control the card from virtually any location within the facility as long as you have a network connection.

Data Insertion

Each channel of the card has a “clean” output that carries the encoded closed caption data and which is protected by a bypass relay, as well as an additional, not by-pass relay protected, closed-captioned video output.

Automatic Regen/Insert Changeover

The closed caption inserter automatically switches back from insert to regen mode, depending on the closed caption data being delivered to the serial and/or Ethernet interfaces. This automatic changeover timeout is configurable, and can be forced to either mode, independantly for Field 1 or Field 2.

GPI Interfaces

Four optically isolated GPIs and four optically isolated GPOs are available to control some of the card's features, including inserting and extracting GPI/O data in the VBI or HD-VANC.

Supported Formats

The HDCC supports the following video formats:

- 480i60
- 576i50
- 720p (all field rates)
- 1035i (all field rates)
- 1080i (all field rates)

Advanced Operation

User Controls

Table 4–1 below lists all the values for SW 1.

Table 4–1 Switch 1 Communications Settings[a]

Setting	Function
0	Insert captions on Channel A from the serial port and on Channel B from the ethernet port.
1	Insert captions on Channel A and Channel B from the serial port.
2	Insert captions on both Channel A and Channel B from the ethernet port.
4 thru D	Not Used
E	Access configuration through serial port
F	Access configuration through Ethernet port

a See also Figure 1–2 on page 4.

Table 4–2 below lists the valid settings for SW 2.

Table 4–2 Switch 2 Communications Settings

Setting	Function
0	Not Used
1	Copy captions from Channel A to Channel B
2	Copy captions from Channel B to Channel A
3	Copy captions from Channel A to Channel B (Field 1)
4	Copy captions from Channel B to Channel A (Field 1)
5	Copy captions from Channel A to Channel B (Field 2)
6	Copy captions from Channel B to Channel A (Field 2)
7 thru F	Not Used

Status Indicators

Table 4–3 below describes the LED status indicators on the front of the HDCC card..

Table 4–3 Front Panel Status Indicators

<table>
<tr><th colspan="2">LED #</th><th>Label</th><th>Color</th><th>Function</th></tr>
<tr><td colspan="2">Power</td><td></td><td>Green</td><td>Lights to indicate that the card is receiving power.</td></tr>
<tr><td colspan="2">SDI Channel A Input</td><td></td><td>Green</td><td>Confirms that a valid serial digital input is present. This LED will light only when the signal is present and locked. If the signal input fails or is not stable, the LED will flash at a 1 Hz rate.</td></tr>
<tr><td colspan="2">SDI Channel B Input</td><td></td><td>Green</td><td>Confirms that a valid serial digital input is present. This LED will light only when the signal is present and locked. If the signal input fails or is not stable, the LED will flash at a 1 Hz rate.</td></tr>
<tr><td>LED 1</td><td>GPI-1</td><td rowspan="4">Green</td><td rowspan="8">Refer to Register 0Eh—See Figure 2–2 on page 16 and Table 2–5 on page 17 for details.</td></tr>
<tr><td>LED 2</td><td>GPI-2</td></tr>
<tr><td>LED 3</td><td>GPI-3</td></tr>
<tr><td>LED 4</td><td>GPI-4</td></tr>
<tr><td>LED 5</td><td>GPO-1</td><td rowspan="4">Red</td></tr>
<tr><td>LED 6</td><td>GPO-2</td></tr>
<tr><td>LED 7</td><td>GPO-3</td></tr>
<tr><td>LED 8</td><td>GPO-4</td></tr>
</table>

Specifications

Table 4–4 Physical Specifications

Specification	Value
Dimensions (H x W x D)	4″ x 8.7″x .5″ (101.60 mm x 220.98 mm x 127.00 mm)
Shipping Weight	1 lbs (.45 kg)
Space Requirements	3 RU
Supplied Accessories	Rear panel adaptor for user-specified frame
Power Requirements	Receives power from frame
Power Consumption	Approximately 10 W

Table 4–5 Technical Specifications

Specification	Value
Inputs	2 SD/HD-SDI autosensing on BNC 4 GPI (DB-9) (on 10-pin header on the Evertz rear panel adaptor)
Outputs	2 HD/SD-SDI Closed Captioned (BNC) 2 HD/SD-SDI By-Pass Relay Protected (BNC) 2 HD/SD-SDI Not By-Pass Relay Protected (BNC) 4 GPO (DB-9) (on 10-pin header on the Evertz rear panel adaptor)
Inputs/Outputs	Ethernet (RJ-45) (not available on the IRT rear panel adaptor) 1 RS-232 (DB-9) (on Codan and IRT rear panel adaptors) 1 RS-232 (10-pin header on the Evertz rear panel adaptor)
Frame compatibility	• Codan • Evertz • IRT
Available functions	• HD/SD Closed Caption Encoding/Inserting • HD/SD Closed Caption Bridging and Transcoding • GPI/O Insertion and Extraction
Available communication protocols	• Grand Alliance • SMPTE333 • CDP
Supported closed caption specifications	CEA-608, CEA-708 (both enpsulated 608, and native 708)

Connector Pin Assignments

Table 4–6 GPI DB-9 Pin-Out Assignments (Codan and IRT Adaptors)

Pin	Label	Interface
1	Common GND	GND
2	GPO-4	Open Collector (Emitter to Ground)
3	GPO-3	
4	GPO-2	
5	GPO-1	
6	GPI-4	Active Low
7	GPI-3	
8	GPI-2	
9	GPI-1	

Figure 4–2 GPI DB-9 Male Pin-Out

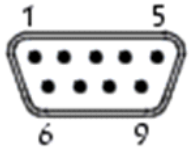


Table 4–7 RS-232 DB-9 Pin-Out Assignments (Codan and IRT Adaptors)

Pin	Label	Function
1	N.C.	Not Connected
2	TXD	RS-232 Tx Data
3	RXD	RS-232 Rx Data
4	Not Connected	
5	Common GND	GND
6	The IRT adaptor has the second serial port available on pins 6 and 7. See table 4-10 below	
7		
8		

Figure 4–3 RS-232 DB-9 Pin-Out

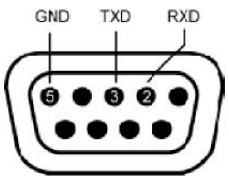


Table 4–8 14-Pin Header Assignments - RS-232 and GPI (Evertz Adaptor)

Pin	Label	Interface
1	GPO-1	Open Collector
2	GPI-1	Active Low
3	GPO-2	Open Collector
4	GPI-2	Active Low
5	GPO-3	Open Collector
6	GPI-3	Active Low
7	GPO-4	Open Collector
8	GPI-4	Active Low
9	RS-232 Rx	RS-232 Rx Data
10	RS-232 Tx	RS-232 Tx Data
11	Common GND	Reference Ground
12		
13		
14		

Figure 4–4 14-Pin Header Assignments

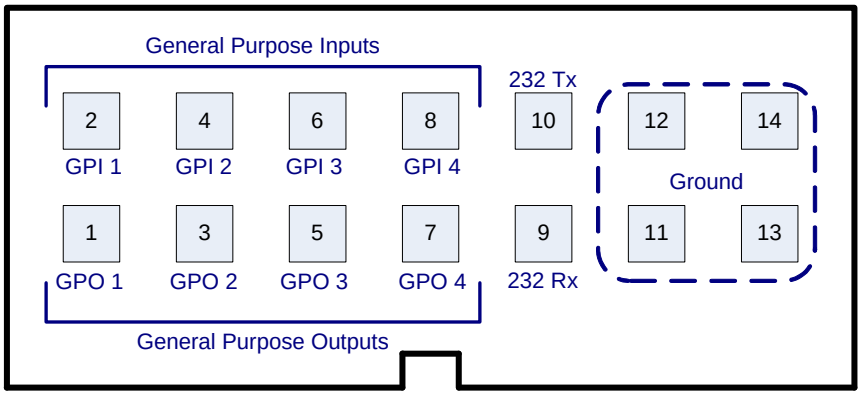


Table 4–9 DB9F Cable Connector Wiring (Codan and IRT Adaptors)

Pin	HDCC (DB9-M) to PC (DB9-F)
1	Do Not Connect.
2	Pin 2
3	Pin 3
4	Do Not Connect.
5	Pin 5

Table 4–9 DB9F Cable Connector Wiring (Codan and IRT Adaptors) (Continued)

Pin	HDCC (DB9-M) to PC (DB9-F)
6	Do Not Connect.
7	
8	
9	

Note: Table 4–10 and Table 4–11 below provide the pin-out for the cable connecting the HDCC to the PC. A straight serial cable (not a null modem cable) will also work.

IMPORTANT: Pins 1, 4, 6, 7, 8, and 9 MUST NOT be connected.

Table 4–10 HDCC (IRT) to PC Interface RS-232 #1 Wiring

HDCC (IRT) DB-9M		PC DB-9F	
Pin	Description	Pin	Description
2	Tx D	2	Rx D
3	Rx D	3	Tx D
5	GND	5	GND
1, 4, 8, and 9: NC		1, 4, 6, 7, 8, and 9: NC	

Table 4–11 HDCC (IRT) to PC Interface RS-232 #2

HDCC (IRT) DB-9M		PC DB-9F	
Pin	Description	Pin	Description
7	Tx D	2	Rx D
6	Rx D	3	Tx D
5	GND	5	GND
1, 4, 8, and 9: NC		1, 4, 6, 7, 8, and 9: NC	

Technical Functional Overview

Figure 4–5 on page 49 illustrates the design of the HDCC.

Figure 4–5 HDCC Block Diagram