HDCC-GPITX

(GPI Cues Transmission Card)

HD/SD-SDI Dual Channel GPI Cues Inserter and Decoder

Configuration Guide

Software Version: V1.03

PIC Code Version: V1.11

Part Number 821145, Revision A

Wohler CONFIDENCE.

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Last Update

Septermber 23, 2011

Table of Contents

CHAPTER 1
Setting the Engineering Registers

Introduction

Overview

This chapter explains how to access the engineering registers to configure the HDCC card for your particular system.

Topics

Connecting to the Card

To perform this procedure you will need:

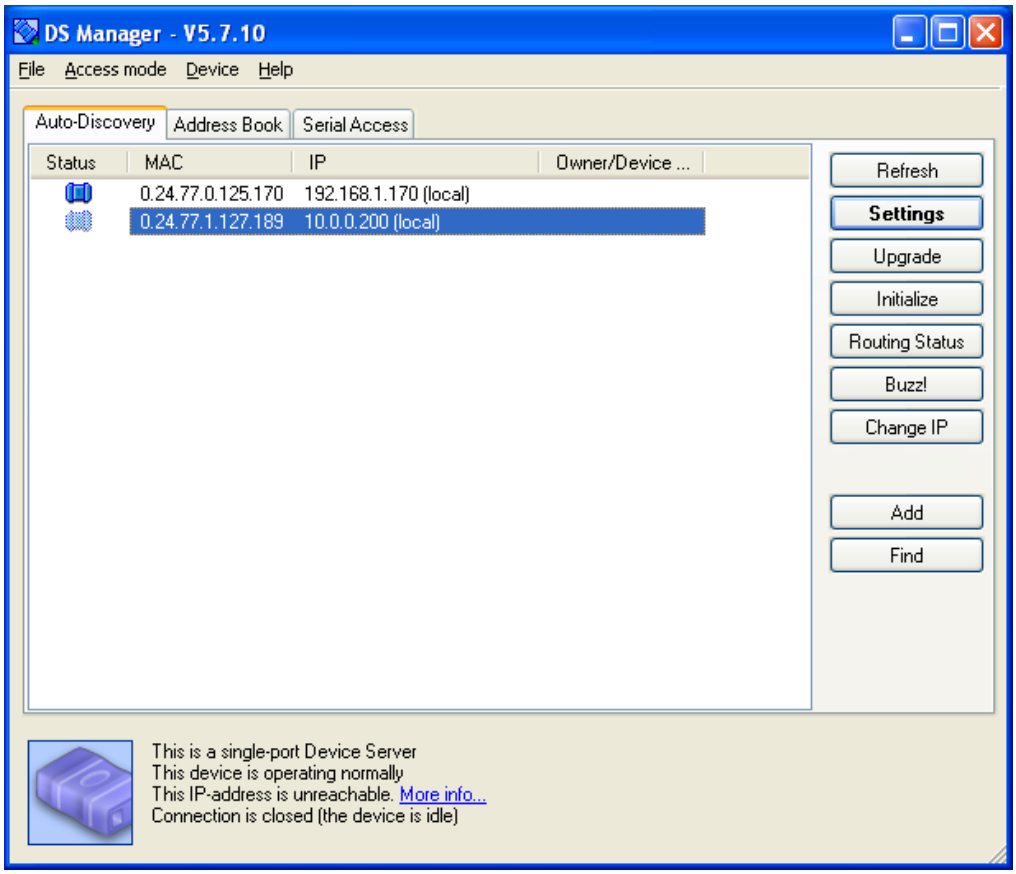
- A PC or laptop with a serial port and/or Ethernet port
- Either or both of the following:
  - A serial cable (connected from the serial port of the PC to the serial port on the HDCC). Refer to Accessing the Configuration on page 5 for more information.
  - An Ethernet cable (connected to the Ethernet ports of the HDCC card and the PC)

Important: You must obtain a valid IP address for your network from your network administrator. In the following example, we'll be using IP address 192.168.1.167 for our HDCC.

To change the IP address on the new HDCC and set-up a virtual serial port connection:

1. Refer to the section entitled "Downloading the Software" in Appendix A of the *Installation Guide* for instructions for downloading the Ethernet configuration application. Continue through the end of "Installing the Software."
2. Launch the DS Manager.
3. Click the **Auto-Discovery** tab if it is not already highlighted.
4. New HDCC cards (with Codan or Evertz backplanes) will have a default IP address of 10.0.0.200. Highlight the HDCC with IP 10.0.0.200.

Figure 1–1 DS Manager Configuration Screen



Note that the color under the **Status** column shows IP 10.0.0.200 disabled (i.e., this card is currently not accessible to the network). The card with IP 192.168.1.170 is an existing HDCC on the network.

5. Click the **Change IP** button.

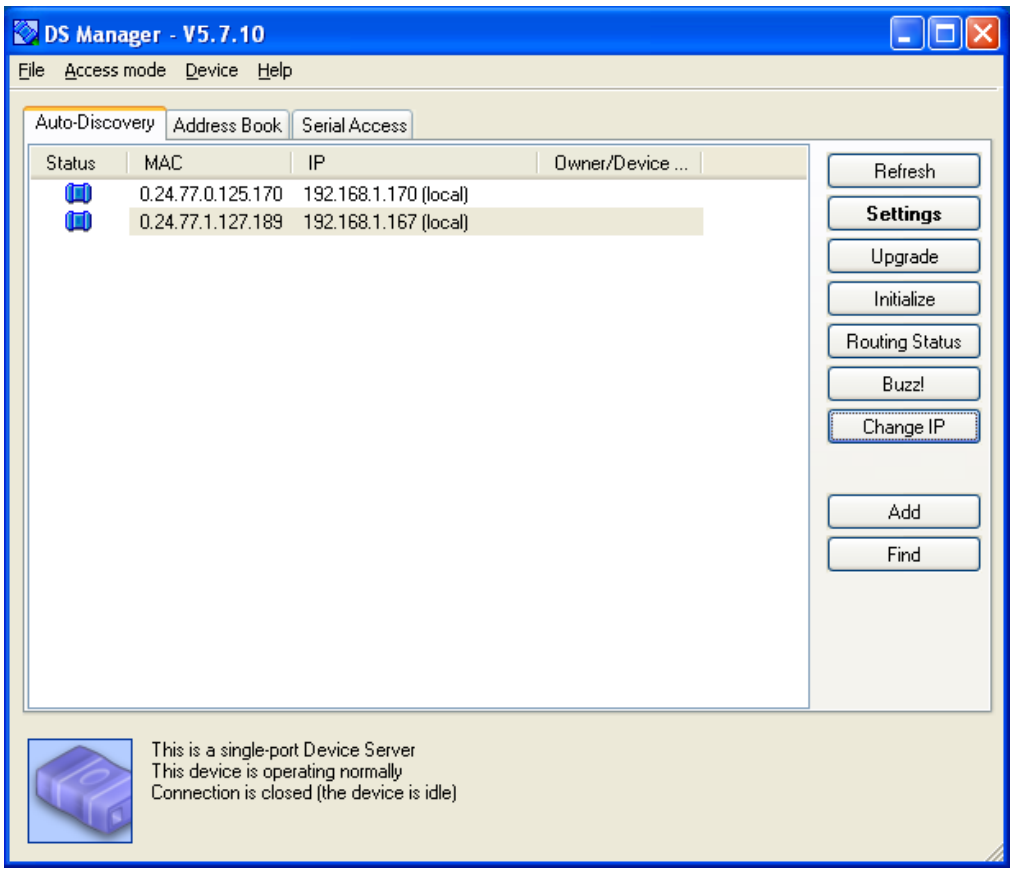
Figure 1–2 Default IP Address Screen

6. In our example we're changing the IP to 192.168.1.167. Type in the address your network administrator gave you.

Figure 1–3 New IP Address Screen

7. Click **OK**.

Figure 1–4 Enabled New IP Address



The new HDCC with IP 192.168.1.167 is now accessible through the network.

8. Close the DS Manager application.

Accessing the Configuration

The card has a number of registers to allow easy configuration of various card parameters that can be accessed from both the RS-232 interface and the Ethernet interface.

To access the configuration registers:

1. Determine whether you want to access the engineering menu from the Ethernet port or from the RS-232 port.

2. Depending how you will access the menu, turn SW 1 to either E or F according to Table 1–1 below.

Table 1–1 Switch 1 Settings - Encoding

SW 1	Insert Text From
E	Access engineering menu through RS232 port.
F	Access engineering menu through Ethernet port.

3. Connect the serial or Ethernet cable from the host computer's port to the port on the rear panel adaptor.

   Note: IRT adaptors do not provide an Ethernet port.

4. Launch your **HDCCRegEdit** program. Refer to the *HDCCRegEdit Guide* (PN 821078) for instructions for using this application.

5. Verify that your communication settings are 38400, n, 8, 1.

Modifying the Register Settings

Table 1–2 Register Table Summary

Channel A	Channel B	Description
00h	20h	Not Used
01h	21h	Not Used
02h	22h	Not Used
03h	23h	Not Used
04h	24h	Not Used
05h	25h	Not Used
06h	26h	Not Used
07h	27h	Not Used
08h	28h	Transmission Features
09h	29h	Reserved for future use
0Ah	2Ah	SD Line for GPI Data Insertion
0Bh	2Bh	HD Line for GPI Data Insertion
0Ch	2Ch	Not Used
0Dh	2Dh	Not Used
0Eh		GPI LED Settings and GPI/O Active Level Settings
0Fh	2Fh	GPI Rx/Tx Polarity Control
10h	30h	Special Features 2
11h	31h	Not Used
12h	32h	GPI Data Insertion Control and Encoder Timeout
13h	33h	GPI Mapping for Tx
14h	34h	Not Used
15h	35h	Not Used
16h	36h	Not Used
17h	37h	Not Used
18h	38h	Not Used
19h	39h	Display Attributes
1Ah	3Ah	Not Used
1Bh	3Bh	Not Used
1Ch	3Ch	Not Used
1Dh	3Dh	Not Used
1Eh	3Eh	Not Used
1Fh	3Fh	Not Used
FDh		Timing Offset—Do Not Change
FEh		GPO 1 and 2 Mapping
FFh		Not Used

Figure 1–5 Registers 08h and 28h (Transmission Features)

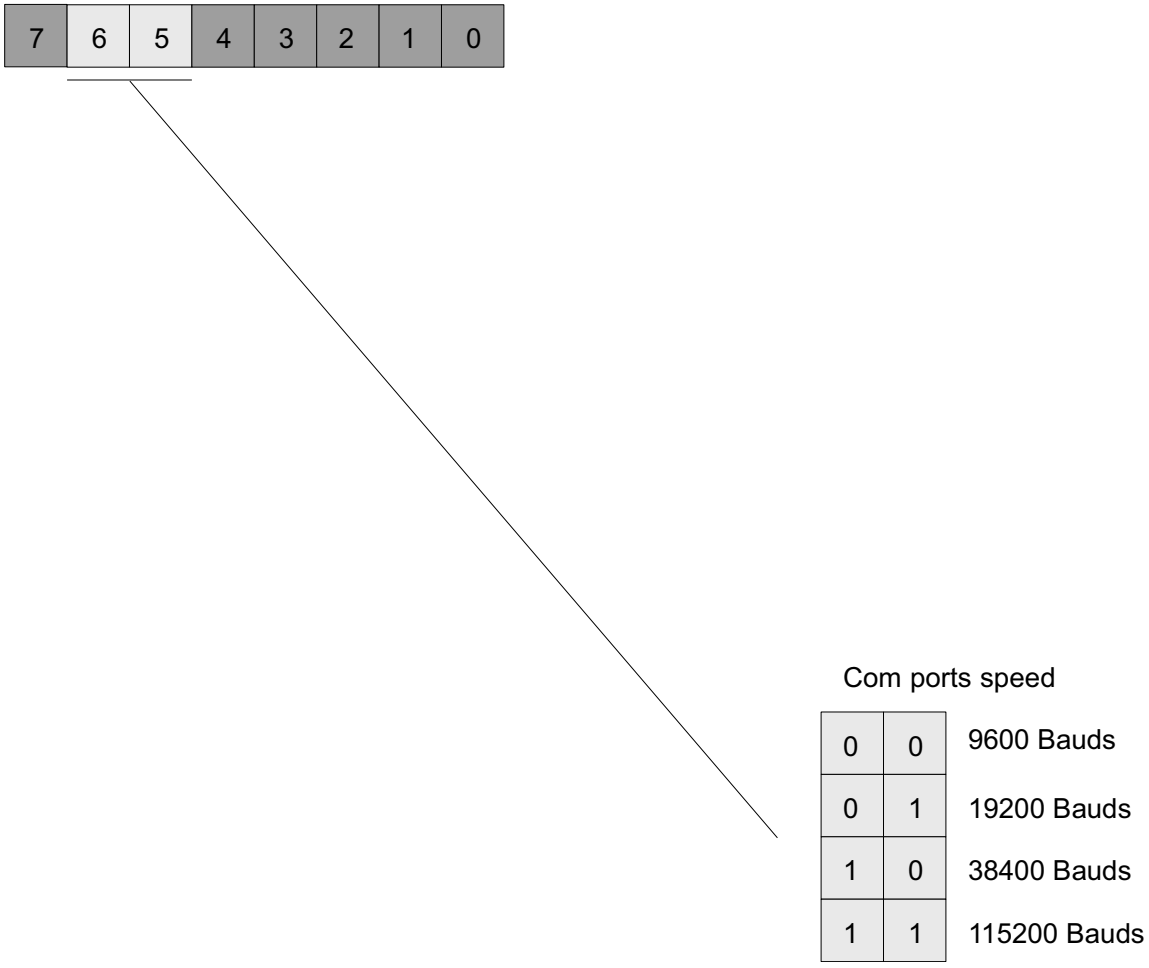
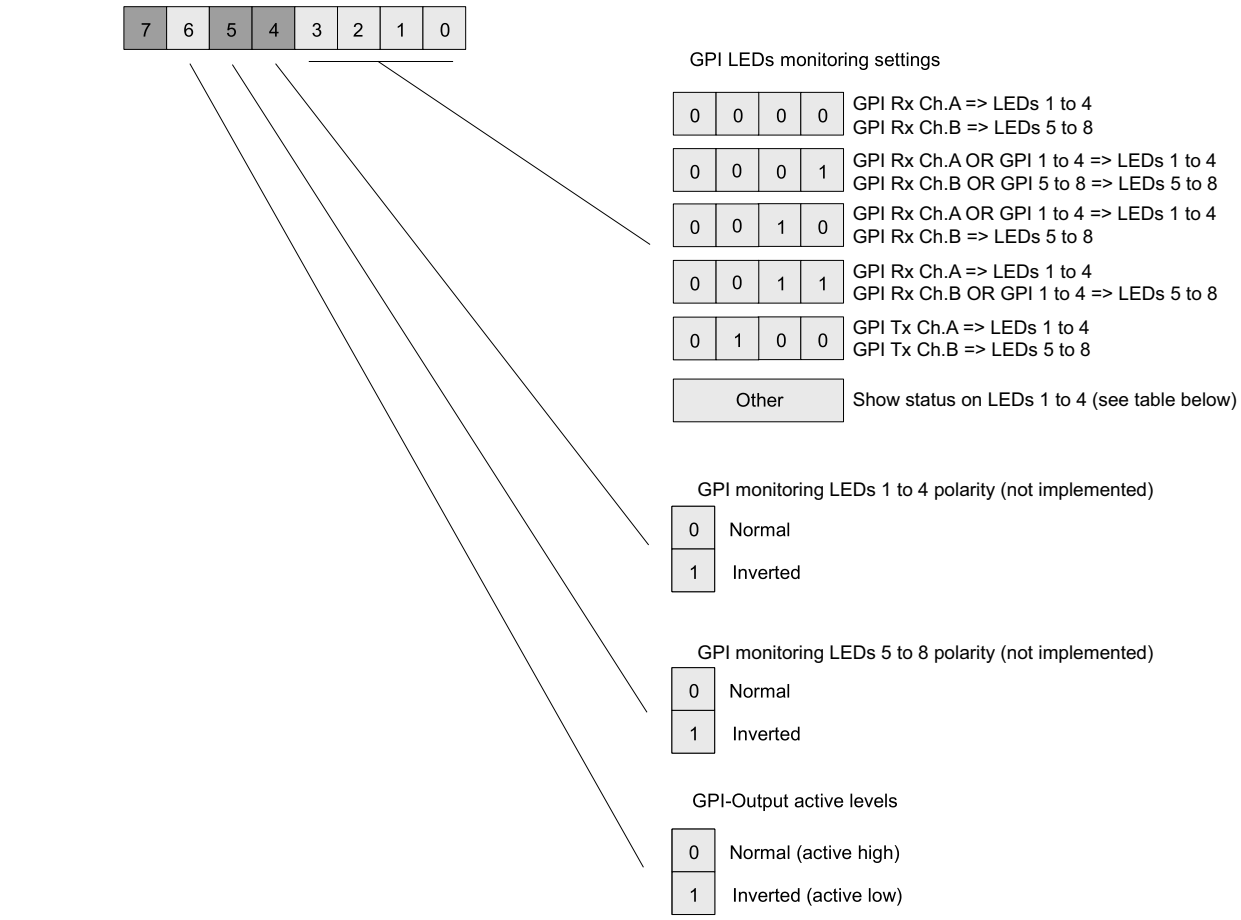


Table 1–3 Register Setting Descriptions

Ch A Reg #	Ch B Reg #	Description
08h	28h	**Transmission Features** *Min: N/A – Max: N/A* Bit(s): 6:5 — Function: Com Port Speed: 00 = 9600 baud 01 = 19200 baud 10 = 38400 baud 11 = 115200 baud
0Ah	2Ah	SD Line for GPI Data
0Bh	2Bh	HD Line for GPI Data

Figure 1–6 Register 0Eh (Register 2Eh Not Used)



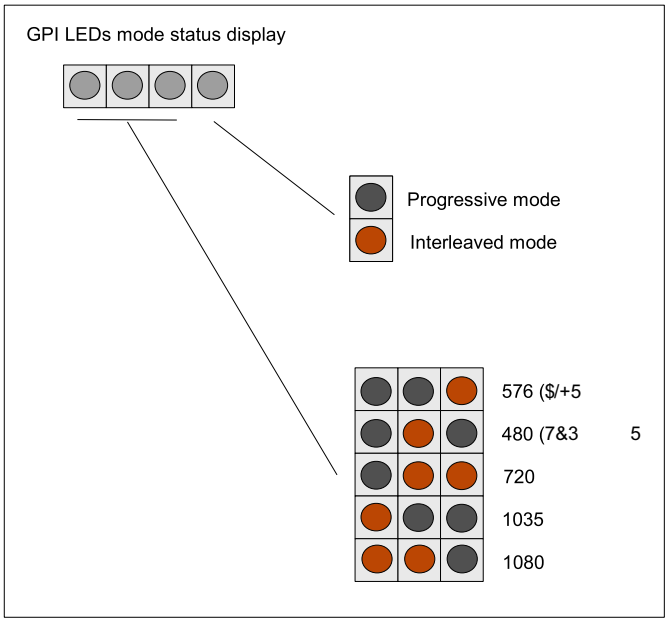


Table 1–4 Register Setting Descriptions

<table>
<tr><th>Ch A & Ch B</th><th>Description</th></tr>
<tr><td>0Eh</td><td>
GPI LED Settings
Min: N/A – Max: N/A
<table>
<tr><th>Bits</th><th>Function</th></tr>
<tr><td>0:3</td><td>
<table>
<tr><th colspan="2">GPI 4</th></tr>
<tr><th>LED</th><th>Description</th></tr>
<tr><td>0000</td><td>GPI Rx Ch A on LEDs 1 to 4
GPI Rx Ch B on LEDs 5 to 8</td></tr>
<tr><td>0001</td><td>GPI Rx Ch A OR GPI-In 1 to 4 on LEDs 1 to 4
GPI Rx Ch B OR GPI-In 1 to 4 on LEDs 5 to 8</td></tr>
<tr><td>0010</td><td>GPI Rx Ch A on LEDs 1 to 4
GPI Rx Ch B OR GPI-In 1 to 4 on LEDs 5 to 8</td></tr>
<tr><td>0011</td><td>GPI Rx Ch A on LEDs 1 to 4
GPI Rx Ch B OR GPI-In 1 to 4 on LEDs 5 to 8</td></tr>
<tr><td>0100</td><td>GPI Tx Ch A on LEDs 1 to 4
GPI Tx Ch B on LEDs 5 to 8</td></tr>
<tr><td>Else</td><td>Show status on LEDs 1 to 4. See tables below.</td></tr>
</table>
<table>
<tr><th>LED</th><th>LED 4 Description</th></tr>
<tr><td>0</td><td>Interleaved Mode</td></tr>
<tr><td>1</td><td>Progressive Mode</td></tr>
</table>
<table>
<tr><th rowspan="2">Description</th><th colspan="3">LED</th></tr>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td>576 (PAL)</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>480 (NTSC)</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>720</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1035</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Not Used</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1080</td><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>4:5</td><td>Not Used</td></tr>
<tr><td>6</td><td>GPI Output Levels: 1=Normal active high
0=Inverted active low</td></tr>
<tr><td>7</td><td>Not Used</td></tr>
</table>
</td></tr>
</table>

Figure 1–7 Registers 0Fh and 2Fh

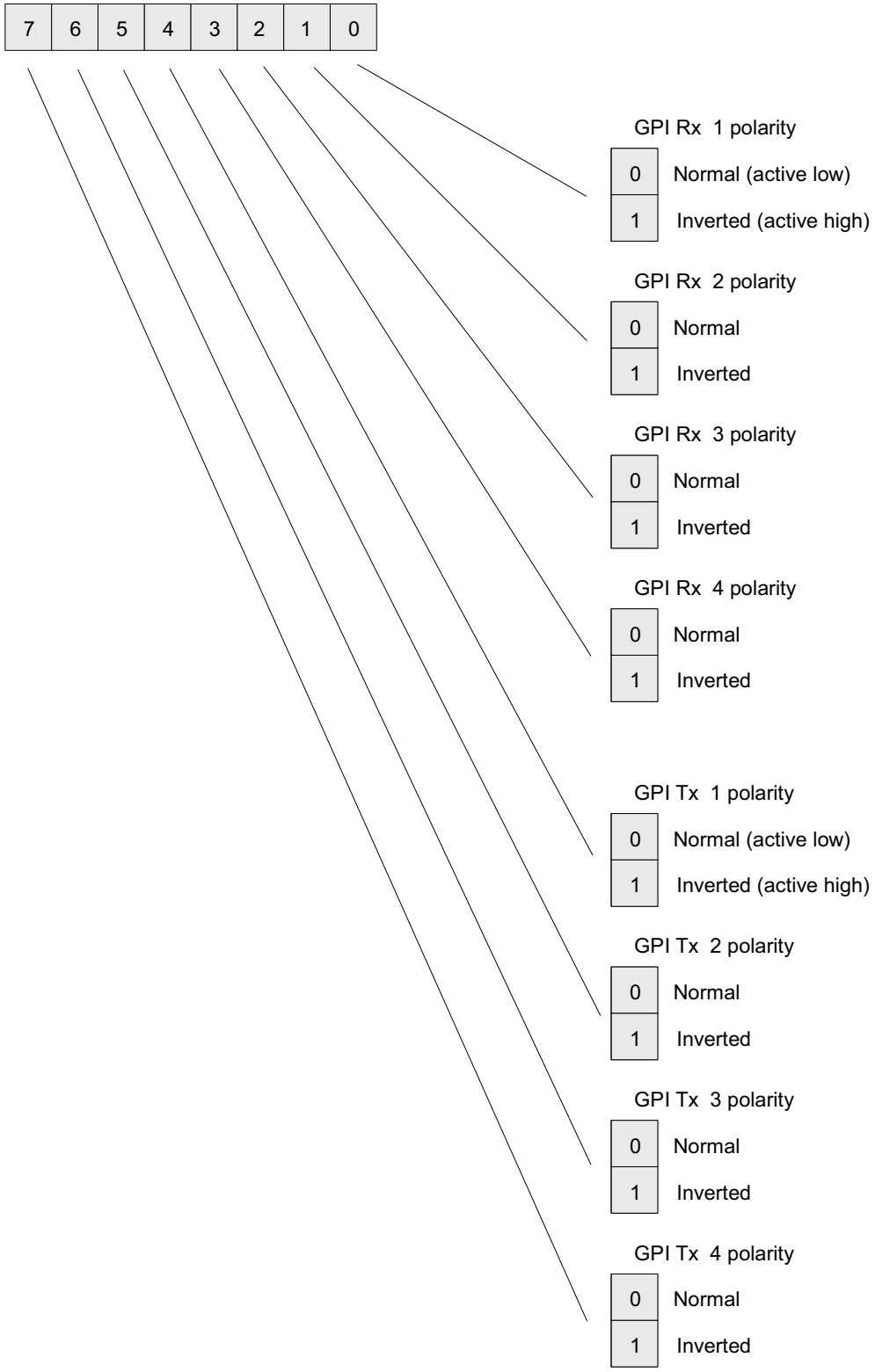


Table 1–5 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>0Fh</td><td>2Fh</td><td>
GPI Tx/Rx Polarity
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>0</td><td>GPI Rx 1</td><td rowspan="8">0 = Normal (Active Low)
1 = Inverted (Active High)</td></tr>
<tr><td>1</td><td>GPI Rx 2</td></tr>
<tr><td>2</td><td>GPI Rx 3</td></tr>
<tr><td>3</td><td>GPI Rx 4</td></tr>
<tr><td>4</td><td>GPI Tx 1</td></tr>
<tr><td>5</td><td>GPI Tx 2</td></tr>
<tr><td>6</td><td>GPI Tx 3</td></tr>
<tr><td>7</td><td>GPI Tx 4</td></tr>
</table>
</td></tr>
</table>

Figure 1–8 Registers 10h and 30h

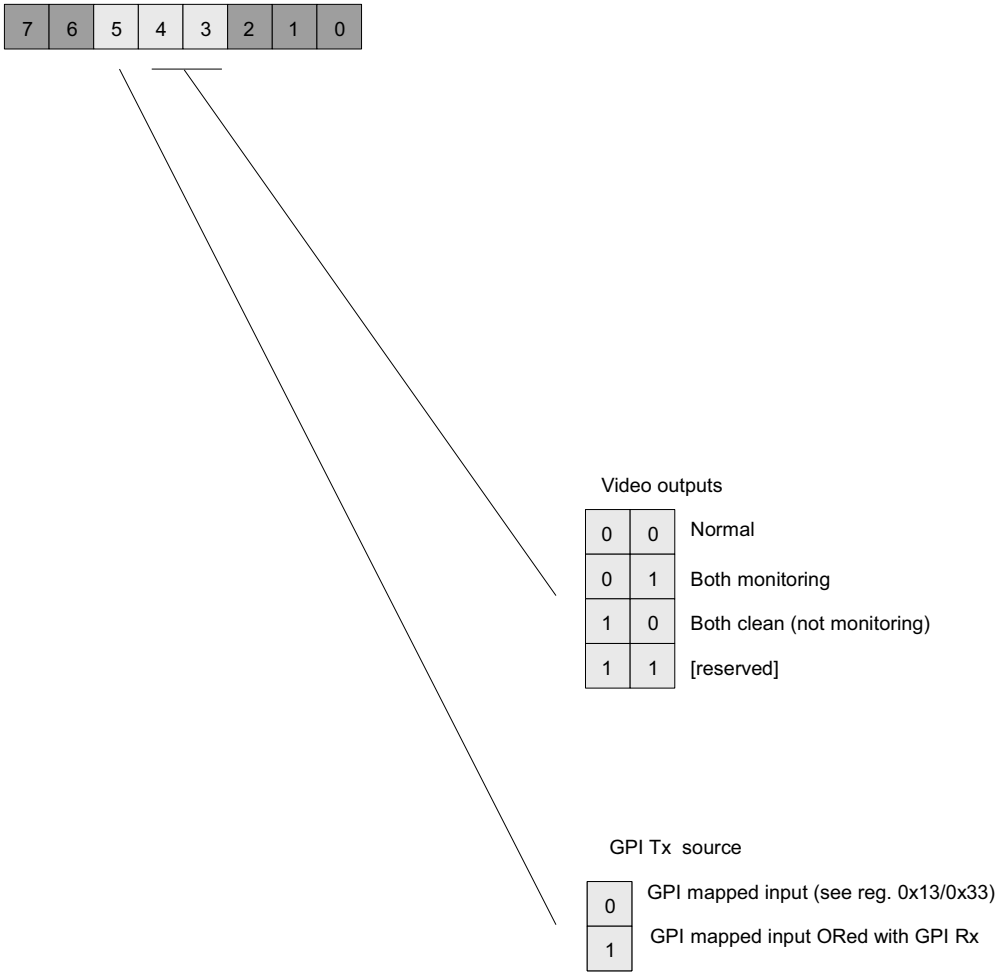


Table 1–6 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>10h</td><td>30h</td><td>
Special Features—2
Min: N/A – Max: N/A

This register controls miscellaneous functions on the card including the video outputs.

<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>3:4[a]</td><td>Video Output Mode:
00 = Normal
01 = Both outputs set to monitoring
10 = Both outputs are clean
11 = Not Used</td></tr>
<tr><td>5</td><td>GPI Tx Source:
0 = GPI mapped input (See Registers 13h and 33h.)
1 = GPI mapped input ORed with GPI Rx</td></tr>
</table>
a Normal (default) = Monitoring O/Ps are 3 and 4; Clean O/Ps are 1 and 2
Monitoring = Burnt-in GPI cues status information on all O/Ps
Clean = No burnt-in GPI cues status information on any O/Ps
</td></tr>
</table>

Figure 1–9 Registers 12h and 32h

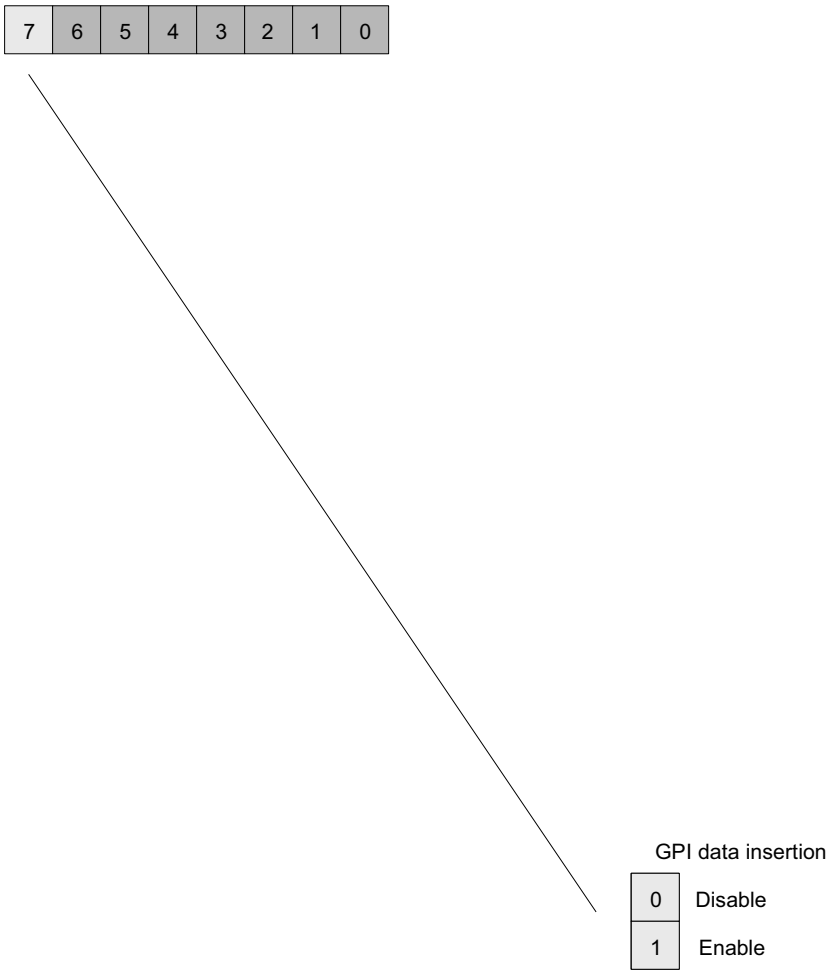


Table 1–7 Register Setting Descriptions

Ch A Reg #	Ch B Reg #	Description
12h	32h	**GPI Insertion Control and Insert Mode Timeout** *Min: N/A – Max: N/A* Bit(s): 7 — Function: GPI Data Insertion: 0 = Off 1 = On

Figure 1–10 Registers 13h and 33h

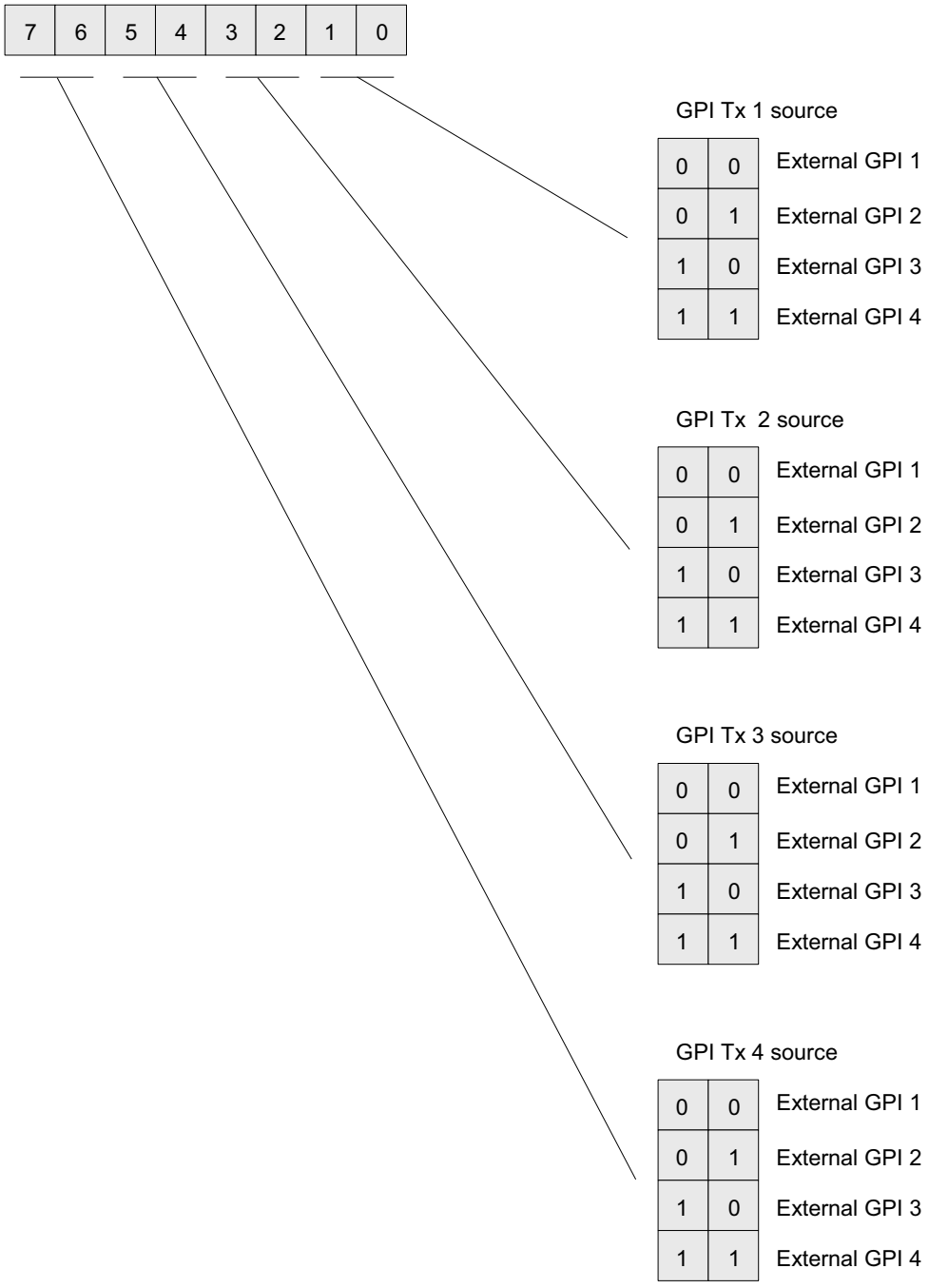


Table 1–8 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>13h</td><td>33h</td><td>GPI Mapping for Tx
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>GPI Tx Source</th><th>Function</th></tr>
<tr><td>0:1</td><td>1</td><td rowspan="4">External GPIs:
00 = GPI 1
01 = GPI 2
10 = GPI 3
11 = GPI 4</td></tr>
<tr><td>2:3</td><td>2</td></tr>
<tr><td>4:5</td><td>3</td></tr>
<tr><td>6:7</td><td>4</td></tr>
</table></td></tr>
</table>

Figure 1–11 Register 19h and 39h

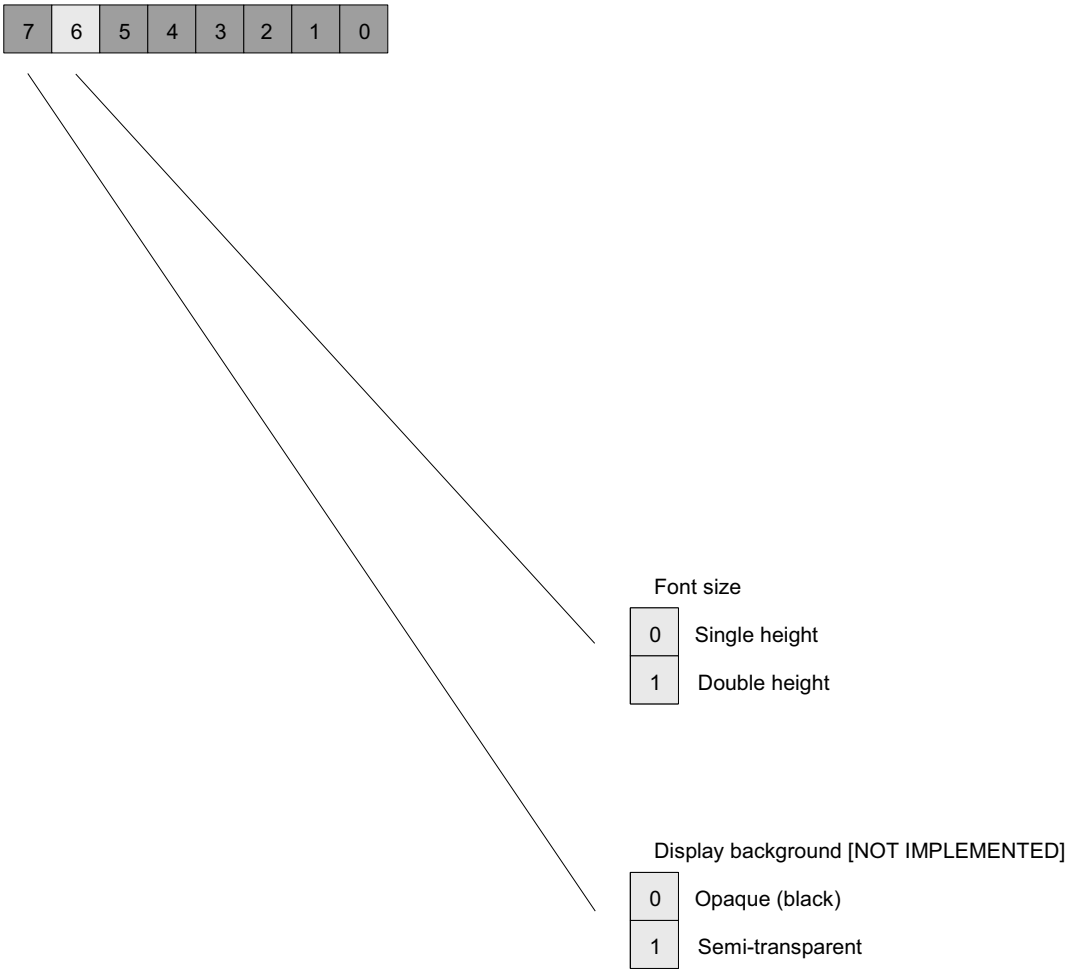


Table 1–9 Register Setting Descriptions

<table>
<tr><th>Ch A Reg #</th><th>Ch B Reg #</th><th>Description</th></tr>
<tr><td>19h</td><td>39h</td><td>Display Attributes
Min: N/A – Max: N/A
<table><tr><th>Bit(s)</th><th>Function</th></tr><tr><td>6</td><td>Font Size
0 = Single Height
1 = Double Height</td></tr></table></td></tr>
</table>

Figure 1–12 Register FEh

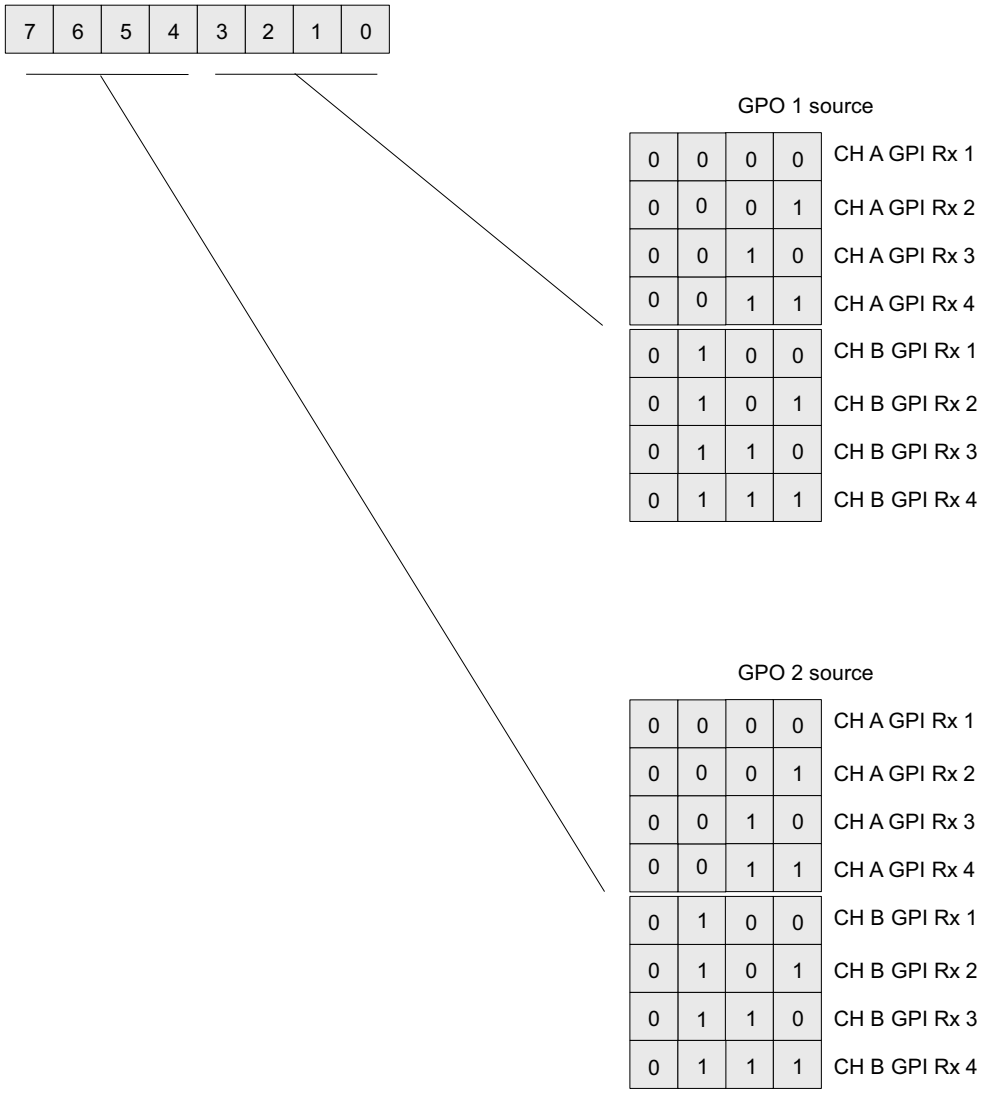


Table 1–10 Register Setting Descriptions

<table>
<tr><th>Both Channels</th><th>Description</th></tr>
<tr><td>FEh</td><td>GPO 1 and 2 Source
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>0:3</td><td>GPO 1 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
<tr><td>4:7</td><td>GPO2 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
</table></td></tr>
</table>

Figure 1–13 Register FFh

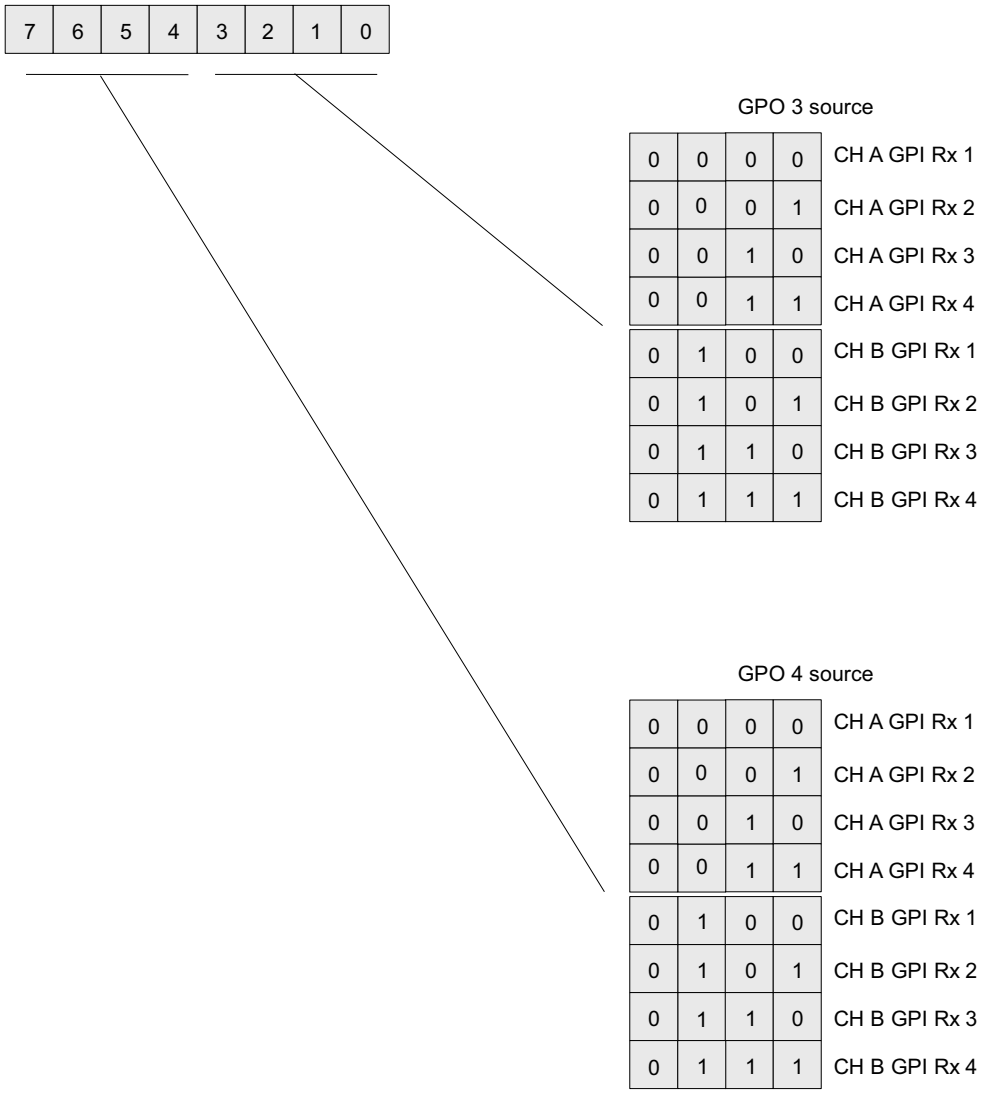


Table 1–11 Register Setting Descriptions

<table>
<tr><th>Both Channels</th><th>Description</th></tr>
<tr><td>FFh</td><td>GPO 3 and 4 Source
Min: N/A – Max: N/A
<table>
<tr><th>Bit(s)</th><th>Function</th></tr>
<tr><td>0:3</td><td>GPO 3 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
<tr><td>4:7</td><td>GPO 4 Source
0000 = Ch A GPI Rx 1
0001 = Ch A GPI Rx 2
0010 = Ch A GPI Rx 3
0011 = Ch A GPI Rx 4
0100 = Ch B GPI Rx 1
0101 = Ch B GPI Rx 2
0110 = Ch B GPI Rx 3
0111 = Ch B GPI Rx 4</td></tr>
</table></td></tr>
</table>

CHAPTER 2
Using the General Purpose Inputs/Outputs

Introduction

Overview

This chapter describes the functionality of the GPI/O connectors on the adaptors.

Topics

Functionality

The GPI interface allows the user to encode contact closure triggers into a HD or SD video stream frame accurately. The encoded data uses a proprietary algorithm designed to withstand severe degradation and prevent false triggering or releasing of GPIs. Error checking information is embedded within the GPI data stream which accomplishes this task and is far more advanced than simple CRC.

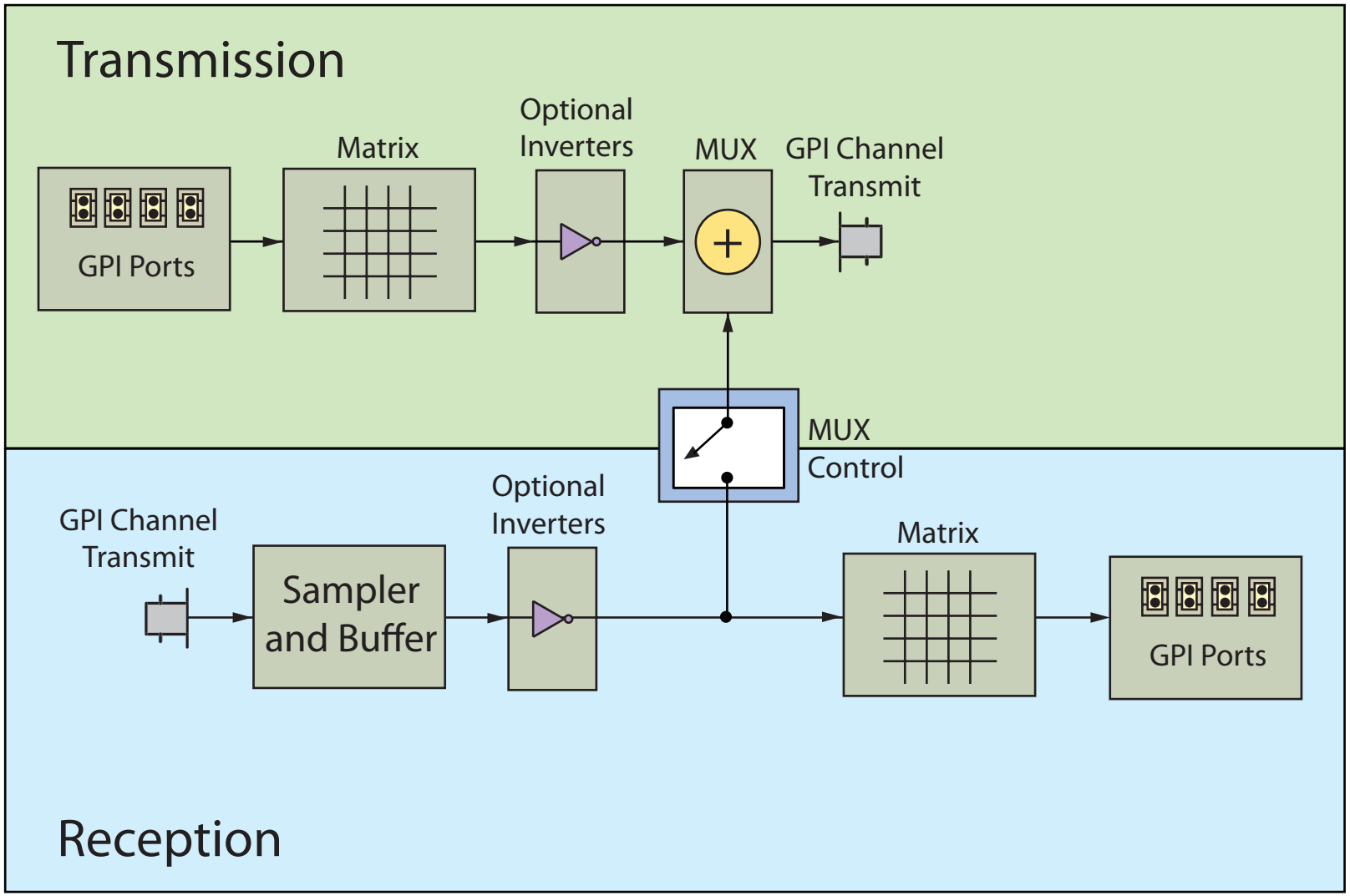
Typical triggers that users can encode from automation include (but are not limited to:

- ARC switching
- Commerical cue triggers (more accurate than the antiquated cue tone system)
- Machine control
- Regional commercial insertion cards

Typically the GPI data is encoded on Line 13 for both the HD-SDI signals and the SD-SDI signals. However, the HDCC is flexible enough to allow you to assign the lines on which you want the GPI data. See Modifying the Register Settings on page 6 for details.

Figure 2–1 on page 25 illustrates the GPI/O signal flow through the HDCC. For our purposes, a GPI is an input signal to the HDCC card supplied by the user through the physical GPI/O port can be encoded onto the outgoing SDI video stream to notify downstream equipment of some condition, event, or command. A GPO is a signal the HDCC card receives on the incoming SDI video stream that is output to the physical GPI/O port to signify some condition, event, or command generated by upstream equipment.

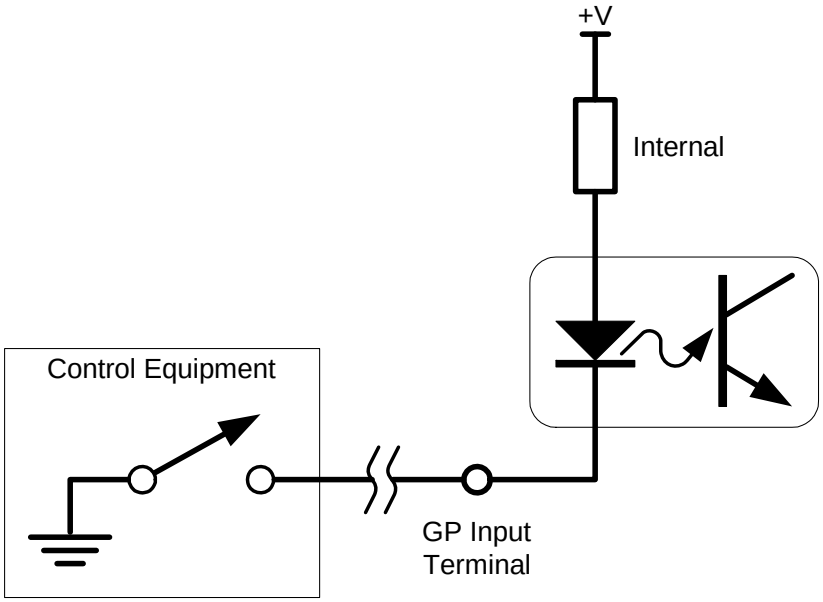
Figure 2–1 GPI/O Functional Diagram



GPIs

The GP inputs are designed to be asserted by switching the closures to ground. Asserting a GP input will result in that input state being encoded on the appropriate line of the video signal and/or activate the required function.

Figure 2–2 Input Diagram



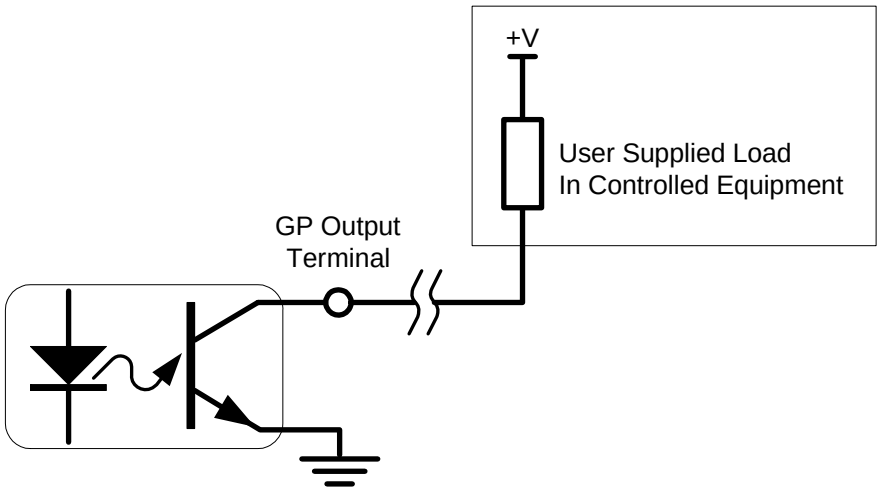
GPOs

If the incoming SDI data stream contains GP data on the appropriate line of the video signal, the corresponding GP output on the card will be activated. The GP output is asserted when its voltage is high.

Important: The GP outputs are optically isolated and "open collector" so the user must provide the appropriate pull-up resistor for each GP output. See Figure 2–3 below.

The HDCC provides four GPOs. (See Connector Pin Assignments on page 34 in Chapter 4 for connectivity.)

Figure 2–3 Output Diagram



GPI/O Polarities

You can control the polarities of the encoded GPIs, both at the receiving stage (Rx) and at the encoding stage (Tx).

GPI Encoded Polarity (Rx)

Channel	Register	Bit(s)	Values
A	0Fh	0 through 3	See Table 2–1 below.
B	2Fh	0 through 3	

The polarity settings are listed in Table 2–1 below.

Table 2–1 GPI Assertion Polarity

Bits	GPI	Active Low (default)	Active High
0	GPI-1	0	1
1	GPI-2	0	1
2	GPI-3	0	1
3	GPI-4	0	1

GPI Encoded Polarity (Tx)

Channel	Register	Bit(s)	Values
A	0Fh	4 through 7	See Table 2–2 below.
B	2Fh	4 through 7	

You can set the polarity of the GPI as encoded on the data stream as shown in Table 2–2 below.

Table 2–2 Register 0Fh and 2Fh: Bits 4 through 7

Bits	GPI	Active Low (default)	Active High
4	GPI-1	0	1
5	GPI-2	0	1
6	GPI-3	0	1
7	GPI-4	0	1

Enabling/Disabling GPI Transmission

Channel	Register	Bit(s)	Values
A	12h	7	0=Disable 1=Enable
B	32h	7	

The HDCC can be configured to enable or disable transmission of GPI data by setting bit 7 of register 12h for Channel A, or 32h for Channel B.

CHAPTER 3
Features and Specifications

Introduction

Overview

This chapter explains the features of the HDCC closed caption card and details all of the specifications.

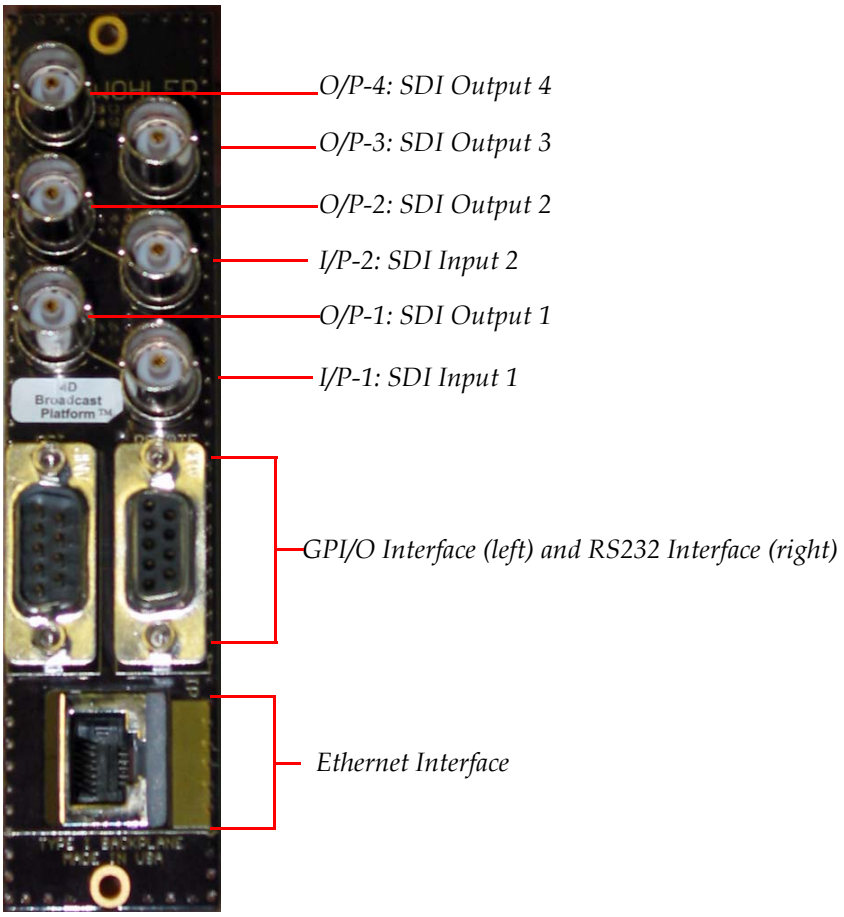
Topics

Features

Hardware

The image and call outs in Figure 3–1 provide a reference for the detailed interface descriptions provided below.

Figure 3–1 Codan Adapter and Interface Layout



BNC Interfaces

- **I/P-1 and I/P-2:** These interfaces (Channel A and Channel B, respectively) accept SDI channel inputs that conform to the SMPTE 259M standard for SD and SMPTE 292M standard for HD.

- **O/P-1 and O/P-2:** These SDI outputs provide GPI cues data encoded video signal. They are relay bypassed on power failure, card removal, or card failure.

- **O/P-3 and O/P 4:** These SDI outputs (Channel A and Channel B, respectively) provide GPI cues data as well as on-screen GPI cues status information. This status OSD is fed from the final output stage of the card.

Ethernet and Serial Interfaces

The ethernet interface (100BT) and the serial (RS-232) interfaces are used to modify the register table.

GPI Interfaces

Four optically isolated GPIs and four optically isolated GPOs are available to four optically isolated GPIs are available to encode up to four GPI cues per output video channel in the VBI or HD-VANC; four optically isolated GPOs are reflecting the status of GPI cues encoded in the input video channels.

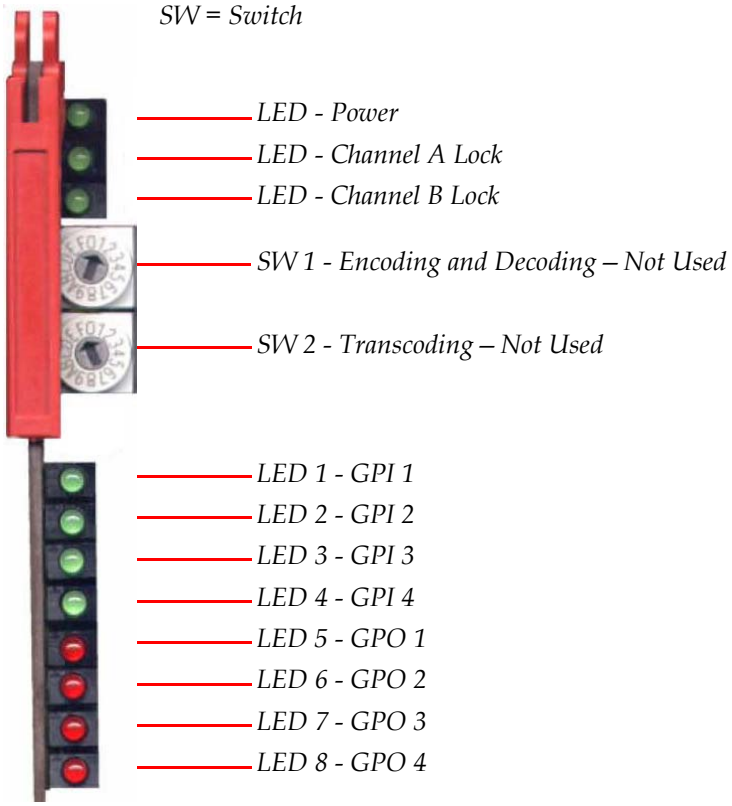
Supported Formats

The HDCC supports the following video formats:

- 480i60
- 576i50
- 720p (all field rates)
- 1035i (all field rates)
- 1080i (all field rates)

Status Indicators

Figure 3–2 HDCC Front Panel



Note: The general purpose input and/or output (GPI/O) functions and pin outs are described in Connector Pin Assignments on page 65.

Table 3–1 below describes the LED status indicators on the front of the HDCC card..

Table 3–1 Front Panel Status Indicators

LED #	Label	Color	Function
Power		Green	Lights to indicate that the card is receiving power.
SDI I/P		Green	Confirms that a valid serial digital input is present. This LED will light only when the signal is present and locked. If the signal input fails or is not stable, the LED will flash at a 1 Hz rate.

Table 3–1 Front Panel Status Indicators

LED #	Label	Color	Function
SDI O/P		Green	Confirms that a valid serial digital input is present. This LED will light only when the signal is present and locked. If the signal input fails or is not stable, the LED will flash at a 1 Hz rate.
LED 1	GPI-1	Green	Refer to Register 0Eh—See Register 0Eh ONLY —Register 2Eh Not Used on page 23 and Table 2–6 on page 29 for details..
LED 2	GPI-2		
LED 3	GPI-3		
LED 4	GPI-4		
LED 5	GPO-1	Red	
LED 6	GPO-2		
LED 7	GPO-3		
LED 8	GPO-4		

Specifications

Table 3–2 Physical Specifications

Specification	Value
Dimensions (H x W x D)	4″ x 8.7″x .5″ (101.60 mm x 220.98 mm x 127.00 mm)
Shipping Weight	1 lbs (.45 kg)
Space Requirements	3 RU
Supplied Accessories	Rear panel adaptor for user-specified frame
Power Requirements	Receives power from frame
Power Consumption	Approximately 10 W

Table 3–3 Technical Specifications

Specification	Value
Inputs	2 SD/HD-SDI autosensing on BNC 4 GPI (DB-9) (on 10-pin header on the Evertz rear panel adaptor)
Outputs	2 HD/SD-SDI Closed Captioned (BNC) 2 HD/SD-SDI Open Captioned (BNC) 4 GPO (DB-9) (on 10-pin header on the Evertz rear panel adaptor)

Table 3–3 Technical Specifications

Specification	Value
Inputs/Outputs	Ethernet (RJ-45) (not available on the IRT rear panel adaptor) 1 RS-232 (DB-9) (on Codan and IRT rear panel adaptors) 1 RS-232 (10-pin header on the Evertz rear panel adaptor)
Frame compatibility	• Codan • Evertz • IRT
Available functions	GPI Encoding and Decoding

Connector Pin Assignments

Table 3–4 GPI DB-9 Pin-Out Assignments (Codan and IRT Adaptors)

Pin	Label	Interface
1	Common GND	GND
2	GPO-4	Open Collector (Emitter to Ground)
3	GPO-3	
4	GPO-2	
5	GPO-1	
6	GPI-4	Active Low
7	GPI-3	
8	GPI-2	
9	GPI-1	

Figure 3–3 GPI DB-9 Male Pin-Out

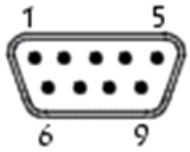


Table 3–5 RS-232 DB-9 Pin-Out Assignments (Codan and IRT Adaptors)

Pin	Label	Function
1	N.C.	Not Connected
2	TXD	RS-232 Tx Data
3	RXD	RS-232 Rx Data
4	Not Connected	
5	Common GND	GND
6	The IRT adaptor has the second serial port available on pins 6 and 7. See table 4-10 below	
7		
8		

Figure 3–4 RS-232 DB-9 Pin-Out

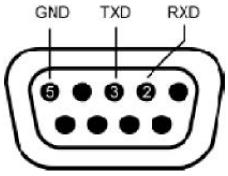


Table 3–6 14-Pin Header Assignments - RS-232 and GPI (Evertz Adaptor)

Pin	Label	Interface
1	GPO-1	Open Collector
2	GPI-1	Active Low
3	GPO-2	Open Collector
4	GPI-2	Active Low
5	GPO-3	Open Collector
6	GPI-3	Active Low
7	GPO-4	Open Collector
8	GPI-4	Active Low
9	RS-232 Rx	RS-232 Rx Data
10	RS-232 Tx	RS-232 Tx Data

Table 3–6 14-Pin Header Assignments - RS-232 and GPI (Evertz Adaptor) (Continued)

Pin	Label	Interface
11	Common GND	Reference Ground
12		
13		
14		

Figure 3–5 14-Pin Header Assignments

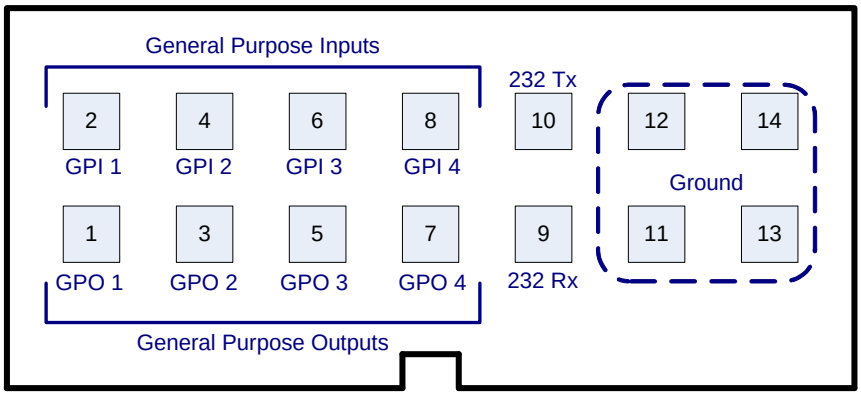


Table 3–7 DB9F Cable Connector Wiring (Codan and IRT Adaptors)

Pin	HDCC (DB9-M) to PC (DB9-F)
1	Do Not Connect.
2	Pin 2
3	Pin 3
4	Do Not Connect.
5	Pin 5
6	Do Not Connect.
7	
8	
9	

Note: Table 3–8 and Table 3–9 below provide the pin-out for the cable connecting the HDCC to the PC. A straight serial cable (not a null modem cable) will also work.

IMPORTANT: Pins 1, 4, 6, 7, 8, and 9 MUST NOT be connected.

Table 3–8 HDCC (IRT) to PC Interface RS-232 #1 Wiring

HDCC (IRT) DB-9M		PC DB-9F	
Pin	Description	Pin	Description
2	Tx D	2	Rx D
3	Rx D	3	Tx D
5	GND	5	GND
1, 4, 8, and 9: NC		1, 4, 6, 7, 8, and 9: NC	

Table 3–9 HDCC (IRT) to PC Interface RS-232 #2

HDCC (IRT) DB-9M		PC DB-9F	
Pin	Description	Pin	Description
7	Tx D	2	Rx D
6	Rx D	3	Tx D
5	GND	5	GND
1, 4, 8, and 9: NC		1, 4, 6, 7, 8, and 9: NC	