

## XVP-3901 – Upgrade Package 9.5.7

### Upgrade Package Release History

Release Version	Comprising:		Release Date	Version Details	User Manual for this release (Miranda document #)
	Firmware Version	Software Version			
9.5.7	9.5.7	9.5.7	2017.08.11	<a href="#">(go)</a>	M886-9900-330
9.5.7	9.5.7	9.5.7	2015.07.30	<a href="#">(go)</a>	M886-9900-330
9.5.7	9.5.7	9.5.7	2015.03.31	<a href="#">(go)</a>	M886-9900-330
9.5.7	9.5.7	9.5.7	2014.06.30	<a href="#">(go)</a>	M886-9900-330
9.5.7	9.5.7	NA	2012.09.20	<a href="#">(go)</a>	M886-9900-330

**NOTES:** The iControl compatibilities shown below are officially supported by Miranda. Earlier versions may also work, with bugs or limited features.  
The Reference number (Ref#) given for each feature or bug in these Release Notes refers to internal Miranda documentation.

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## VERSION: FW:957, CPU:172, FPGA1:2380, FPGA2:1080

Release date: 2017-08-03

iControl compatibility: 4.13 (build 039) and up

iControl Solo compatibility: 4.30 (build 020) and up

RCP-200 compatibility: 1.5.0 (build 771) and up

Hardware incompatibility: This firmware applies to all existing hardware assembly.

### BUGFIXES

Bug#	Description
<a href="#">XVP3901-1788</a>	<b>Frame Sync Issue for 23.98pSF asynchronous</b> When input is asynchronous and format is 1080psF 23.98/24, every 30 minutes, a 3 pixel shift occurs for one frame.

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## **VERSION: 9.5.7 (REL-L) : CPU:172, FPGA1:2339, FPGA2:1080**

Release date: 2015-07-30

iControl compatibility: 4.13 (build 039) and up

iControl Solo compatibility: 4.30 (build 020) and up

RCP-200 compatibility: 1.5.0 (build 771) and up

Hardware incompatibility: This firmware applies to all existing hardware assembly.

### **BUGS FIXED IN THIS RELEASE**

Ref #	Description
<a href="#">XVP3901-1676</a>	<b>PRESETs don't work on new hardware with new dataflash</b>  Parameters are not properly stored in non-volatile memory on new hardware (PCB 600) because the new flash memory requires adapted firmware.  WORKAROUND: use older hardware platform.

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## VERSION: **FW:957 (RC2-10) : CPU:136, FPGA1:2339, FPGA2:1080**

Release date: 2015-03-31

iControl compatibility: 4.13 (build 039) and up

iControl Solo compatibility: 4.30 (build 020) and up

RCP-200 compatibility: 1.5.0 (build 771) and up

Hardware incompatibility: This firmware applies **ONLY** to PCB version 500 and lower.

### BUGFIXES

Bug#	Description
<a href="#">XVP3901-1647</a>	LINK A/B INVERSION AFTER OUTPUT TIMING UPDATE ON 1080P59.94/1080P50 LEVEL B DUAL LINK
<a href="#">XVP3901-1659</a>	<b>PRESERVE INCOMING VPID</b> If all the following conditions are met, the VPID bytes are transferred from the input to the output without any processing: <ol style="list-style-type: none"><li>1. Video format is 3Gbits/s in either Level-A or Level-B Dual-Link</li><li>2. Input and output video formats are identical</li></ol>

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## **VERSION: FW:957 (RC2-9) : CPU:68, FPGA1:2225, FPGA2:1080**

Release date: 2014-06-30

iControl compatibility: 4.13 (build 039) and up

iControl Solo compatibility: 4.30 (build 020) and up

RCP-200 compatibility: 1.5.0 (build 771) and up

Hardware incompatibility: This firmware applies **ONLY** to PCB version 500 and lower.

### **BUGFIXES**

Bug#	Description
<a href="#">XVP3901-1626</a>	1080p59Hz/1080p50Hz Level B Dual link switch line is incorrect

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## VERSION: **FW:957 (RC2-8)** : CPU:67, FPGA1:2225, FPGA2:1080

Release date: 2012-09-20

iControl compatibility: 4.13 (build 039) and up

iControl Solo compatibility: 4.30 (build 020) and up

RCP-200 compatibility: 1.5.0 (build 771) and up

Hardware incompatibility: This firmware applies **ONLY** to PCB version 500 and lower.

### BUGFIXES

Bug#	Description
<a href="#">XVP3901-1563</a>	<b>Horizontal HD timing for 1080i59 do not reach 29.649usec</b>  We can't set more than 23.121usec for 1080i59 Horizontal Timing
<a href="#">XVP3901-1567</a>	<b>Can't save Horizontal timing over 29.649 on user presets for 1080p23sF outputs</b>

## VERSION: FW:957 (RC2-7) : CPU:59, FPGA1:2187, FPGA2:1080

Release date: 2012-01-08

iControl compatibility: 4.13 (build 039) and up

iControl Solo compatibility: 4.30 (build 020) and up

RCP-200 compatibility: 1.5.0 (build 771) and up

Hardware incompatibility: This firmware applies **ONLY** to PCB version 500 and lower.

### BUGFIXES

Bug#	Description
<a href="#">37781</a>	Switch line 1080p23sF
<a href="#">33568</a>	3Gig VPID correction
<a href="#">37937</a>	<b>Video Actif offset on 1080p59.94 Level B</b> Fixed with 1080p59.94 Level B DL input and external reference

### ENHANCEMENTS & NEW FEATURES

Bug#	Description
24783	<b>Add 1080p23.98sF output for 1080p23/p23sF sources</b>  A change has been made to allow the conversion of 1080p23.98/p23sF to 1080p23.98sF. The new 1080p23psF output mode needs to be enabled on the card otherwise the card will continue to produce the selected output format. If enabled, the output format is forced to 1080p23.98sF when the video input is either 1080p23.98 or 1080p23.98sF.
32461	<b>Support SMPTE 318 with URS</b>  To correctly synchronize a 1080p23SF input format with the reference, it is strongly recommended to use an NTSC black burst reference which has a SMPTE 318M information and connect it to the REF-1801. This information will tell the card the timing relation between 59Hz and 23 Hz to ensure all cards have exactly the same output timing. Without it, all 23pSF output will be synchronous, but they may have a different output timing adjustment. The cards must be configured to use the internal URS reference signal coming from the REF-1801 card.

	This is mandatory for the Sony SI project as the external reference will not be properly supported.
33584	<p><b>HANC/VANC passthrough for 1080p23sF operation</b></p> <p>HANC/VANC passes transparently during 1080p23sF to 1080p23sF operation.</p> <p>It is highly recommended to disable VOF in order to avoid any high frequency artifacts.</p> <p>Due to this enhancement, the overall HD out processing delay without reference has been reduced from 82ms to 41ms. With a URS-59 reference, the overall HD output processing delay has been reduced from 59-100 msec to approximately 34-76 msec (in frame sync mode).</p>
32556	<p><b>Support for 3G B Level B -DS (dual stream) input to output</b></p> <p>If a 3G-Level B-DS with 2x1080i59/50 signal is inserted, the HD output is forced to the same format as the input signal. The SD output will not be functional and the test pattern is forced on that output.</p>

## KNOWN BUGS & LIMITATIONS

Bug#	Description
	<p><b>Some limitations for 1080p23sF output format:</b></p> <ul style="list-style-type: none"> <li>- When generating a 1080p23sF HD output, AFD frame accuracy cannot be guaranteed during an input image switch. This is true for both HD and SD outputs only during Auto AFD mode.</li> <li>- In this mode, the SD output undergoes a 3:2 pulldown sequence in order to convert from 1080p23sF to 480i59Hz. This 3:2 sequence is free run. For this reason, there can be a +/- 8 msec lip-sync (relation audio/video) error. Regardless, the SD output video will always be aligned with the reference.</li> <li>- Output alignment and overall operation may not be guaranteed when using a NTSC, 1080i, or 720p tri-level reference. Only a black burst with SMPTE 318M on the REF-1801 distributed using the USR to the cards is supported.</li> <li>- Audio Modules are not supported in this mode.</li> <li>- Audio/Video Fingerprint is not functional in this mode.</li> </ul>



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	<b>1080p23sF to 1080p23sF/SD mode</b> <b>1080p25sF to 1080p25sF/SD mode</b> <b>1080p29sF to 1080p29sF/SD mode</b>
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The Video-Over-Film function should be manually disabled in order to avoid any deinterlacing artifacts within high frequency regions. This is not a limitation, it is a configuration recommendation for the customer.

	<p><b>Video format reporting for pSF formats</b></p> <p>The following formats will not be reported as pSF formats:</p> <ul style="list-style-type: none"> <li>- 1080p25sF will be reported as 1080i50.</li> <li>- 1080p29sF will be reported as 1080i59.</li> </ul>
	<p><b>Film sources 1080p23, 1080p23sF, 1080p25, and 1080p29</b></p> <p>With these input formats, a number of limitations will be present (and have always been present on the XVP-3901):</p> <ul style="list-style-type: none"> <li>- Deglitcher mode is disabled during these sources. If you make a video source hot switch with another source, the video output may freeze momentarily (2-3 frames).</li> <li>- Video sources with Ancillary TimeCode (ATC) of type LTC will be detected, but it will not be passed through the card in those formats. The only exception is 1080p23sF to 1080p23sF. During this mode, ATC of type LTC data may be bypassed to the output using the VBI Insert parameter.</li> <li>- ATC of type VITC will be processed correctly for those formats. The limitation is only for ATC of type LTC.</li> <li>- No key-fill operation is permitted during these sources.</li> </ul>

	<p><b>3G Level B -DS (dual stream) input to output</b></p> <ul style="list-style-type: none"> <li>- Only 2 x 1080i59/50 video signals may be installed during 3G Level B -DS operation.</li> <li>- All incoming ancillary information on Link B is stripped and will not be passed at the output.</li> <li>- The input image shall pass untouched. All video scaling and detail enhancement are disabled.</li> <li>- No key-fill operation is permitted.</li> <li>- A valid 3G Level B -DS source shall produce a 3G Level B -DS output only. During this time, the SD output shall display the internal test pattern as it is not possible to output a dual stream in SD.</li> <li>- The HD output thumbnail will be invalid. Link A and Link B streams will be merged and may produce a distorted image.</li> <li>- Auto or forced AFD not supported.</li> <li>- AFD, CC, ATC shall pass through with no modification.</li> <li>- Freeze function is limited to Black only. The freeze to black will be used every time the video input is in error.</li> </ul>
33876	<p><b>HANC/VANC packets with 3G Level B –DL (dual link) may appear on Link B</b></p> <ul style="list-style-type: none"> <li>- In 3G Level B Dual Link, the HANC/VANC packets (AFD, ATC, Dolby Metadata ...) at the output of the card may sometimes appear either on Link A or on link B when the card conditions change (after power-up hot switch, reference changes, etc...). This does not affect the operations with other Miranda cards which will detect the presence of those packets on both links.</li> <li>- Any metadata not specifically handled by the XVP-3901 during 3G-B-DL outputs, may be randomly placed on Link A or Link B.</li> </ul>
	<p><b>No ATC of type LTC support from HD to 3G Level B –DL (dual link) operation.</b></p> <p>This limitation has always existed. Only ATC of type VITC will be processed.</p>