PESA Engineering Bulletin

Firmware release notes for:

Cheetah Gen1 Embedder revision 10.11.11

Cheetah Gen2 Embedder revision 10.5.5

October 2, 2013

# Overview

This revision of the Cheetah Embedder firmware corrects a problem with the clock phase data contained in the audio packets within each HD video stream. The clock phase data is used by receiving equipment video as one method to recreate the audio sample clock.

# Background

There are two predominate methods used to recreate an audio sample clock from SMPTE HD-SDI and 3G-SDI video signals. The majority of broadcast video equipment includes one or more phase locked loops (PLLs) that are used to synthesize the audio clock directly from the video clock or from a reference signal. The audio packets within SMPTE HD-SDI and 3G-SDI video streams also contain clock phase data that may be used to recreate the audio clock from the video clock without requiring a PLL. This approach is less expensive and easier to implement than the PLL approach but results in more jitter in the recovered audio clock.

In general terms, SMPTE HD-SDI and 3G-SDI video streams may be thought of as a continuous progression or stream of video lines where the end of one line is immediately followed by the beginning of the next line. Each line contains an area for active video data and another area for non-video or ancillary data. These areas are separated by Start of Active Video (SAV) and End of Active Video (EAV) markers. Since the video signal is a continuous stream of consecutive lines, the point at which one line ends and another begins depends upon your frame of reference. While discussing audio packets it is easiest to consider the EAV marker as the point where one line ends and another line begins (see “Figure 1 - Video Line Format”).



Figure - Video Line Format

Audio information is typically placed in the ancillary data space of the line following that in which the sample occurred. For example, “Figure 1 - Video Line Format” shows audio samples (A, B, C, and D) occurring at regular intervals (that is, at the Audio Clock rate). Samples A and B occur during line N and will be placed into the ancillary data space of line N+1. Sample C occurs during line N+1 and will be placed into the ancillary data space of line N+2. The audio embedder must also maintain a counter to measure the number of video clock cycles that have elapsed between each audio sample and the previous EAV. The value of this counter represents the phase of the audio clock with respect to the beginning of the video line in which the audio sample occurred. This phase information is included along with the audio sample data in each audio packet and a video receiver may use this information to recreate a fairly accurate audio clock that may be used to play back the audio samples.

The SMPTE specifications dictate that no audio shall be placed into the line following the video switching line. Any audio samples captured during the switching line must be delayed one additional line before being placed into ancillary space. Referring back to the example (see “Figure 1 - Video Line Format”), assume that line N is the video switching line. Although samples A and B occurred during line N they cannot be inserted into ancillary space until line N+2 since no audio is allowed on the line following the switch point. In the mean time sample C has occurred during line N+1 so there are three samples to be inserted into line N+2. To differentiate between those samples that occurred two lines in the past and those that occurred one line in the past, the SMPTE specifications include a flag bit that will be set for samples that occurred two lines in the past.

# Description of Problem

Customers occasionally reported problems when connecting PESA embedders to certain third-party equipment. Most of the time the information about this problem was sketchy and incomplete, but one customer was able to provide detailed information that allowed us to recreate the problem in-house. It was found that the clock phase information in the audio packets was incorrect. In particular, the flag that identifies samples that occurred two lines in the past was not being generated correctly. Any equipment that synthesizes the audio clock using PLLs locked to the video clock would work correctly, but equipment that recreates the audio clock from the phase data in the audio packets will encounter problems due to this bug.

# Solution

The logic used to create the audio phase flag has been updated to work properly and new firmware has been released to correct the problem. Customers using the 128 or 256 channel Gen1 Embedders, or the 128 or 256 channel Gen2 Embedders are potentially affected by this issue and should be notified that new firmware is available.