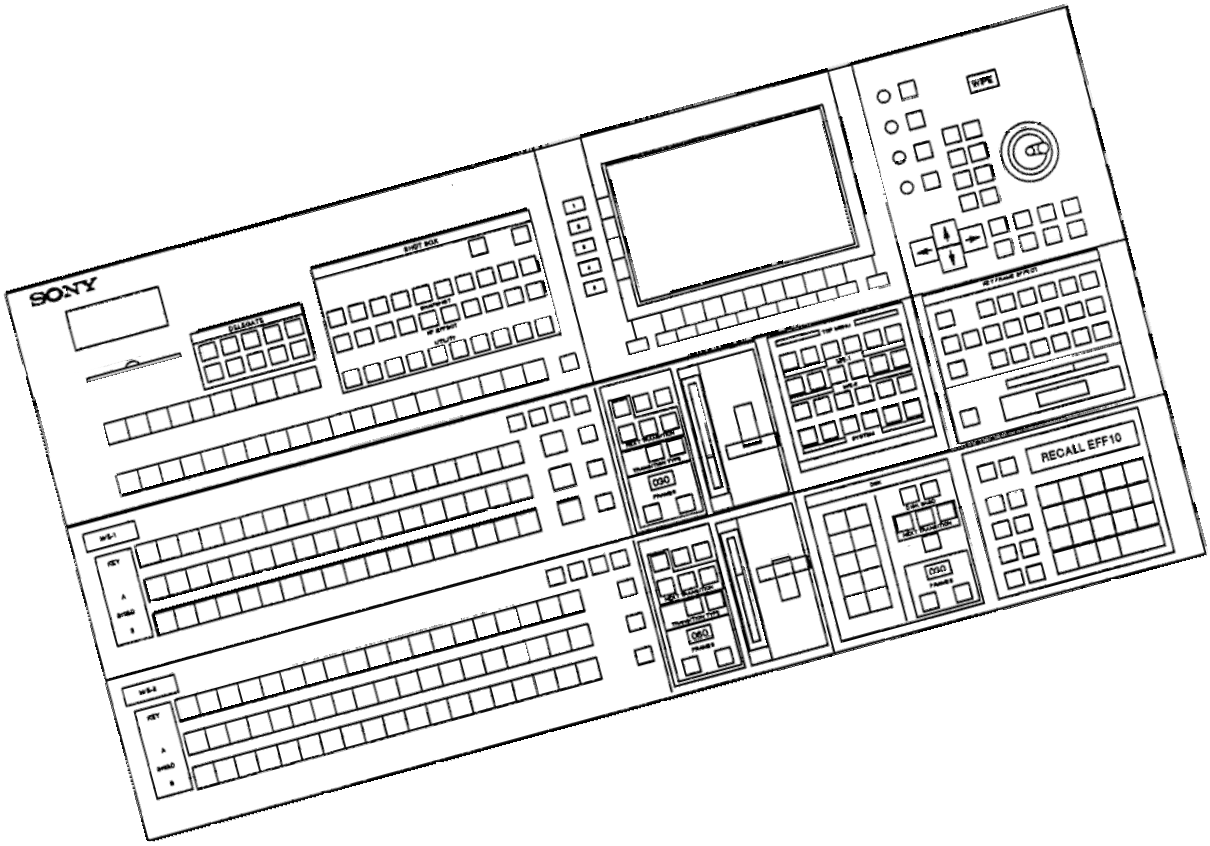
Technical Training

DVS-6000C Maintenance

PDF Compilation June 1997



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DVS-6000C Course Notes - PDF Contents

Credits

This is the PDF / Pocket edition of the DVS-6000C Course Notes, and was compiled by Phil Spiegelhalter, of ***The Sony Training Centre, Basingstoke*** as a portable Archive Record, in June 97.
Original text and drawings by Phil Spiegelhalter. Other illustrations by Kim Anderson, and Atsugi colleagues.
In this first electronic edition, no link pages have been created, and many illustrations are monochromatic.

Note: Engineering Bulletins (available on TIPPS) applying to this product have been produced recently, and are not included within this document. The software currently in use is now V3.xx

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5	*Rear View of Mainframe - connections*
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127-130	Appendices — Separate Document: *Engineering Bulletin for V3.04 release*

Chassis

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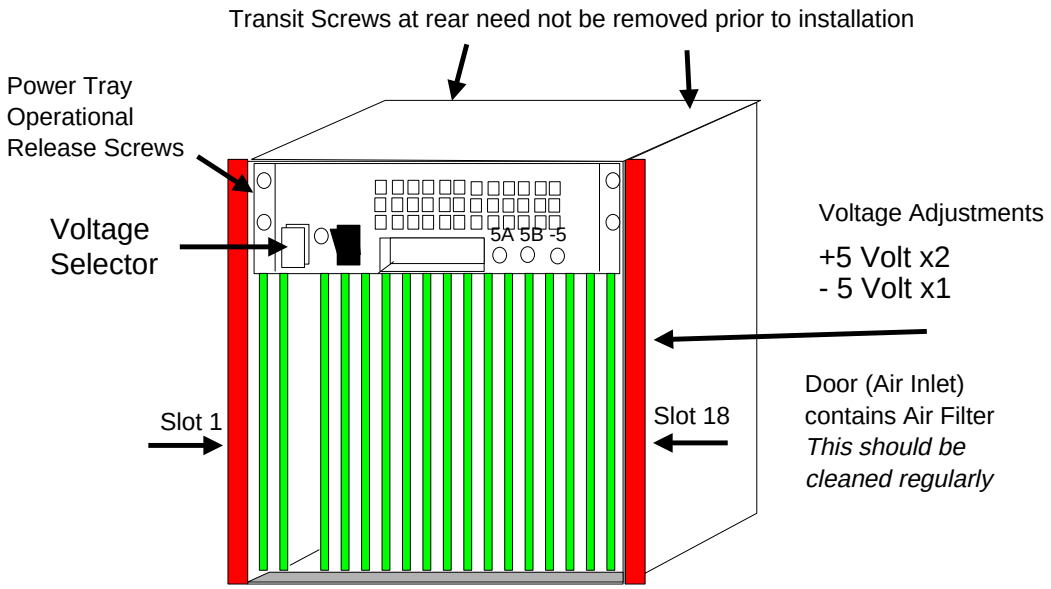
Power Tray and Voltage test slots

CAUTION: Check Voltage Range Selection prior to installation!



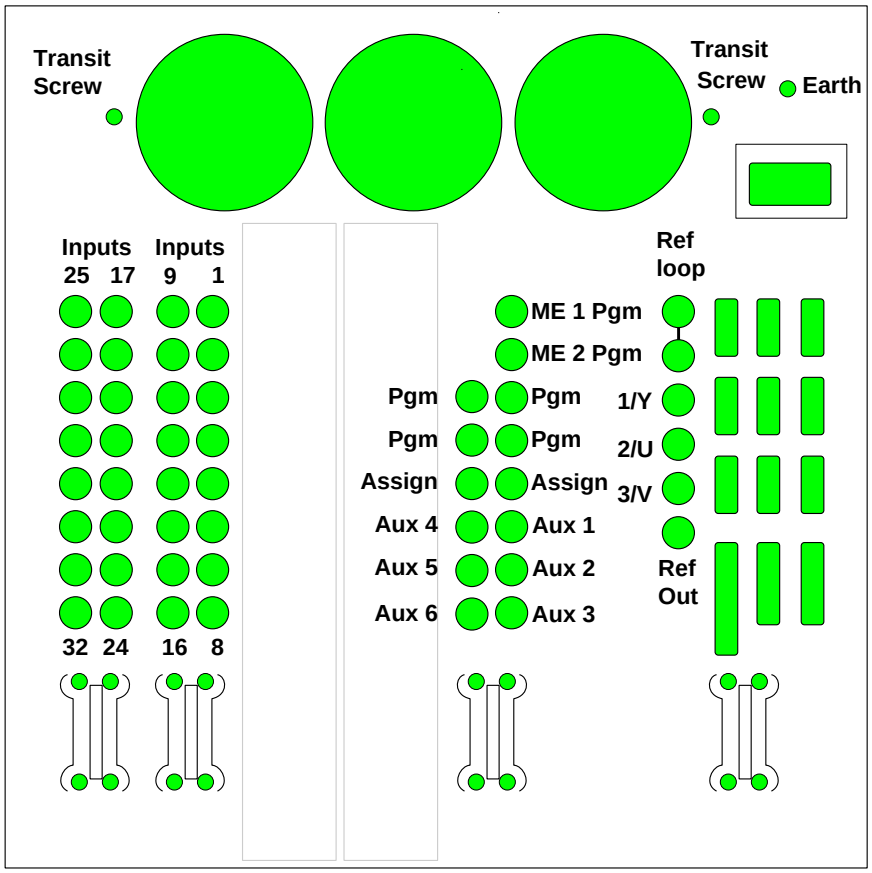
Location of Boards

1/	CPU-147: CPU Board
2/	SG-211: Sync Gen.+Test+LE118/SD30/DA72
3/	EMPTY SLOT
4/	WKG-10: Basic Wipes + WP37 Enhanced
5/	KPC-5: Key Processor Board
6/	MIX-8(A): Mixer Board (Preview = Option)
7/	KPC-5: Key Processor Board
8/	MIX-8(A): Mixer Board (Preview = Option)
9/	MIX-9(A): DSK / Background Mix Board
10/	OUT-3: Output Carrier + SD31modules
11/	CRK-4: Chromakey Processor - Option '8031
12/	CRK-4: Chromakey Processor - Option '8031
13/	MAT-4: Matte Gen/ Re-entry + MT90 blend
14/	MY-51: Frame Memory - Option / MY-67
15/	XPT-2/3/4: Digital or ADC-107 Analogue Input
16/	XPT-2/3/4: Digital or ADC-107 Analogue Input
17/	XPT-2/3/4: Digital or ADC-107 Analogue Input
18/	XPT-2/3/4: Digital or ADC-107 Analogue Input

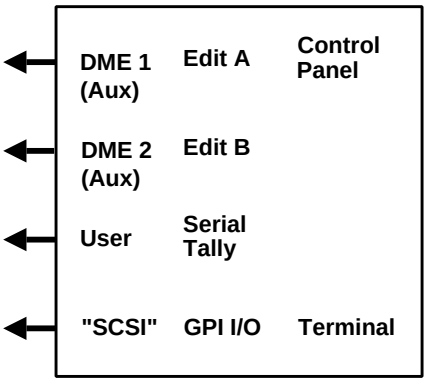
BKDS - 8031 Chromakey *(2 identical boards)* Slot 11 = ME 1, Slot 12 = ME 2
Since any signal may be used as a source (internal or external) no additional external dedicated chromakey inputs are required.

BKDS - 8041 Frame Memory (2 channels, each with last X) Sources = Aux 5 and 6
BKDS-6041 MY-67 - new Frame Memory supporting External Storage of Pictures / Data
BKDS-8022 digital input XPT-3, **BKDS-8023** Component analogue input
or BKDS-8024 digital input XPT-4, with video level adjustments

Rear Connectors



IEC Mains Socket is attached to chassis, and not power tray



1/2/3 or YUV outputs are Analogue Edit Preview

Serial Tally labelled "Matrix" on schematics

"SCSCI" interface intended for MY-67 via IF-499 on SG-211

Board Position in Mainframe

	DVS-6000C	*Options	Comparison: DVS-8000C
1	CPU-147 CPU		CPU-57
2	SG-211 Sync Generator +LE-118	*/*SD-30 Digital Edit Pvw BKDS-6060*	SG-189
		*/*DA-72 Analogue E.Pvw BKDS-6062*	
3	————————		WKG-5
4	WKG-10 Basic Wipes	*+*WP-37 Enhanced Wipes BKDS-6070*	WKG-4
5	KPC-5 Key Processor ME1	*/+*BD-22 Border Generator BKDS-6071*	KPC-1
6	MIX-8A Mixer ME1	*/+Key Preview BKDS-6074*	MIX-4(A)
7	KPC-5 Key Processor ME2	*/+*BD-22 Border Generator BKDS-6071*	KPC-1
8	MIX-8A Mixer ME2	*/+Key Preview BKDS-6074*	MIX-4(A)
9	DSK-9A Downstream Keyer		MIX-6(A)
10	OUT-3 Digital Out mother	*+10x *SD-31 Dig.Out BKDS-6063*	OUT-2
11	**CRK-4 Chromakey Processor*	*½ of BKDS-8031*	*CRK-4*
12	**CRK-4 Chromakey Processor*	*½ of BKDS-8031*	*CRK-4*
13	MAT-4 Matte Gen.	*+2x *MT-90 Bkgnd Col Mix BKDS-6072*	MAT-2
14	**MY-51 Frame Memory BKDS-8041*		*MY-51*
15	**XPT-3 (8x) Digital Inputs 1-8*	***or** AD-107 2xYUV + 2K BKDS-8022/3*	XPT-2
16	**XPT-3 (8x) Digital Inputs 9-16*	***or** AD-107 2xYUV + 2K BKDS-8022/3*	XPT-2
17	**XPT-3 (8x) Digital Inputs 17-24*	***or** AD-107 2xYUV + 2K BKDS-8022/3*	XPT-2
18	**XPT-3 (8x) Digital Inputs 25-32*	***or** AD-107 2xYUV + 2K BKDS-8022/3*	XPT-2

* Options Summary

* BKDS-6010 important “option” -the control panel
* BZS -6020 important “option” -the software (ON DISC)(3½“ HD)
$* BKDS-8022 Digital Input board (8 inputs) XPT-3 ...the new standard for 8000 as well
$* BKDS-8031 Clean Chromakey (as 8000) -CRK-4 x2
$* BKDS-8041 Frame Memory Board MY-51 (2 x 2 [last x on each channel]) /MY-67
* BKDS-6050 Keyframe Control Panel
* BKDS-6060 Digital Edit Preview *-mounts on SG-211 or alternatively*
* BKDS-6062 Analogue YUV Edit Preview Output *-mounts on SG-211*
* BKDS-6070 Enhanced wipe Generator -WP-37
* BKDS-6071 Key Border Generator (1 per Key processor required) -BD-22
* BKDS-6072 Colour Background Mix option (2 required) -MT-90 mounts on MAT-4
* BKDS-6090 Spare Power Tray Unit ——NOTE——this is NOT autorange switching!!
$* Extender card EX-209

Volume Two of the Maintenance Manual

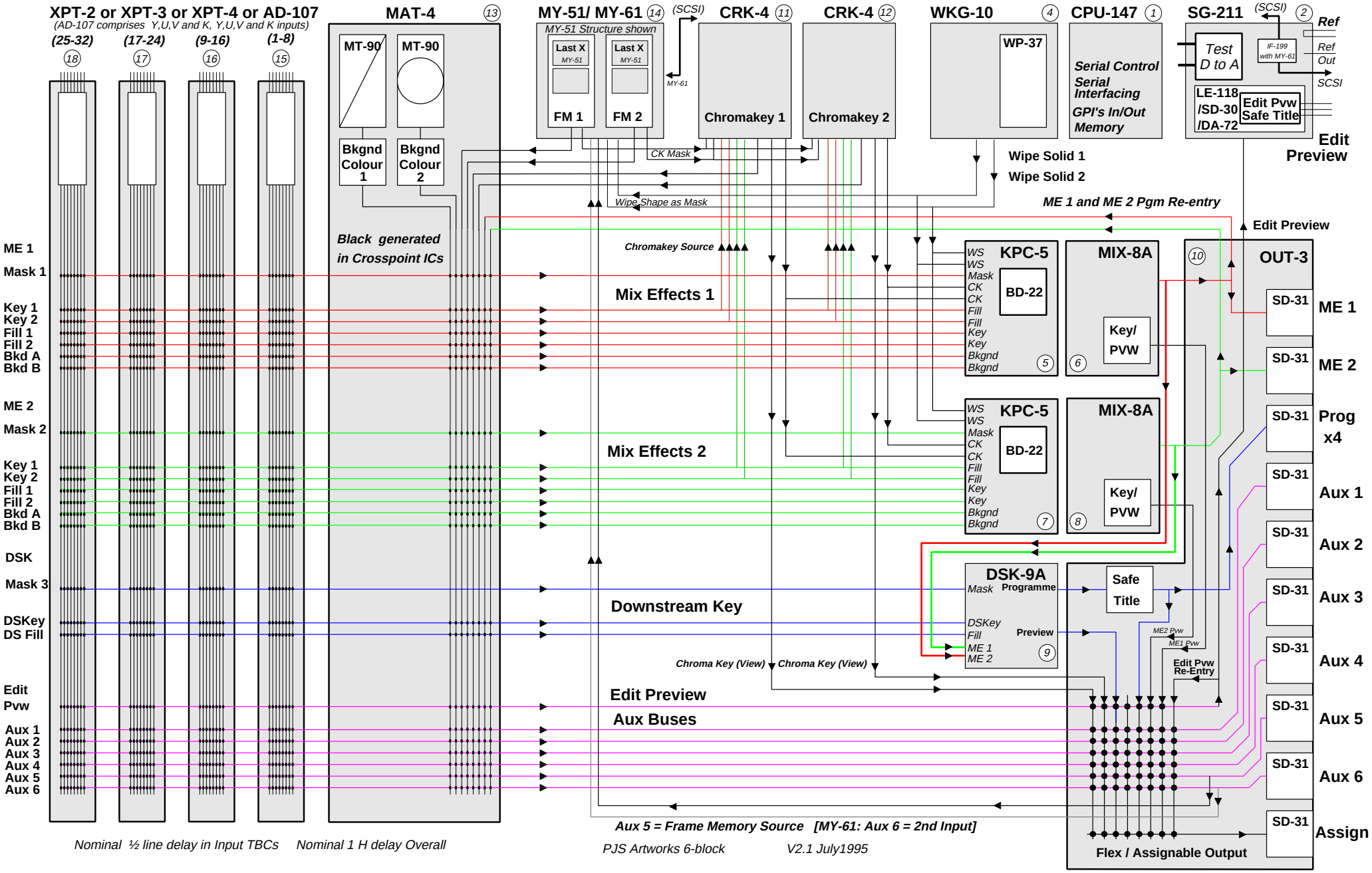
$ = common to DVS-8000C - Other boards may share the basic philosophy.

Dummy boards occupy positions of WP-37/BD-22/MT-90 if no option

LE-118 board is replaced by SD-30 or DA-72

Technical Training

DVS-6000C Vision Switcher (Mixer)



Background

Information

Background Information

PDF Edition

Summary of Features / differences for those with both a DVS-8000C and a DVS-6000C

The architecture is of 2 fully-featured Mix-effects banks 1 + 2 in parallel, combining by mixing or keying at the Downstream keyer, where 10 additional programmable source selection buttons allow for further flexibility. An integral Shotbox is provided

To allow the DVS to be configured to meet a wide variety of customers needs, many of the features have been made optional. Different units at the same location may therefore be configured optimally for their intended use, with onlt the required options and consequent cost saving.

The philosophy of plug-in piggy-back boards allows for easy upgrading and fault correction in the event of a fault by reducing the "basic module" size - making confirmation easier and repair cheaper.

Although no manual fader is provided for DSK / background transition control area, the autotransition button may have different transition times simultaneously (ie independant)

The disk drive is incorporated into the control panel, and provides a convenient means of updating the software, in conjunction with the use of reprogrammable Flash Memory.
Reference -Vertical Drive and Disk drive communication is now included in same 9-pin RS-422 cable connecting the control panel to the mainframe; therefore no separate feed of reference feed or second Rs-422 cable is used, but all 9 wires must be used.

Additional Auxiliary buses 5 and 6 are available, since no P/P programme or Preview is required. The video source for the optional Frame Memory is now from Aux 5, making it independant of the Edit Preview bus.

The Key border option may be added to a single ME at a time.
Mosaic and Diamond dust wipe patterns are now optional.
Blending background colours uses an optional basic wipe generator.

The use of a larger display panel has allowed an easier user interface.

Since a third ME wipe generator is not required, the connectors previously used for this have been reused enabling the optional chromakeys to be flexibly used on either or both MEs.

Note: The label on the control panel for NAM mixing does not apply to the component model.

Before turning on.....
The new power tray for the 6000 IS NOT AUTORANGE switching!!- check voltage first!

E+OE

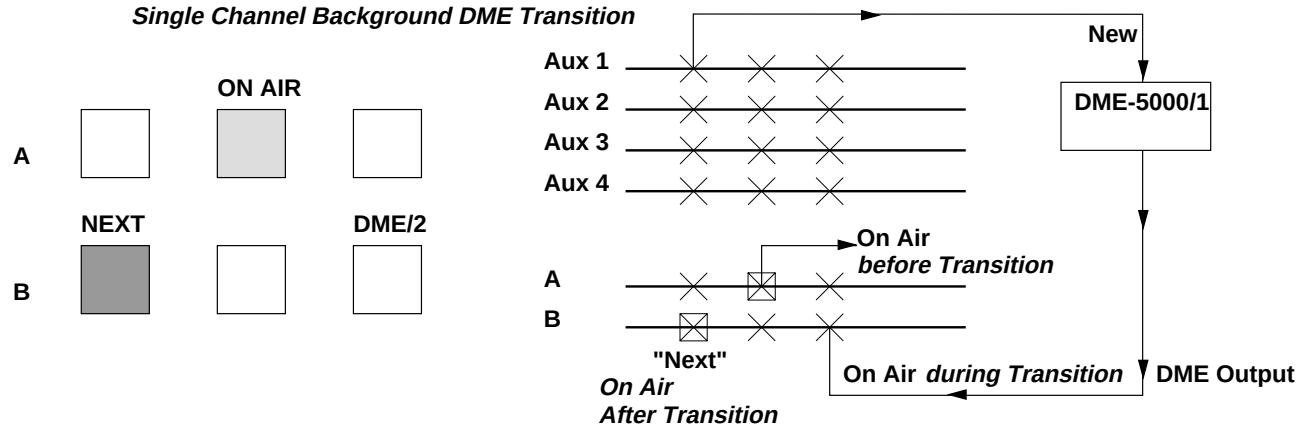
For more complete information refer to the Product Information Manual

DME- Switcher Link:

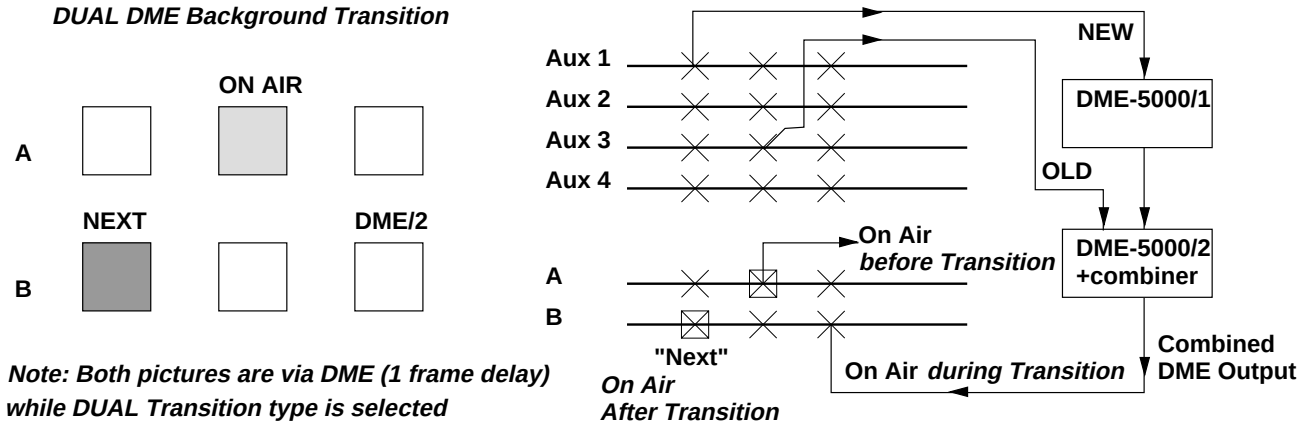
Most DME operations are to perform a picture transition, as a variation from a standard wipe.

The integrated design of the DVS/DME combination enables the operator to use DME transitional effects as simply as any other wipe transition, by using the same group of pattern and source selectors.

The DVS-8000C M/E 1 or M/E 2 fader arm/Auto transition may control the DME transition effect, in conjunction with the internal Aux buses for source switching.



Transitions may be Background or Key. Normal toggle action applies for background (whole picture) transitions, whereas Key transitions will reverse off on the next (key) transition.



Note: Both pictures are via DME (1 frame delay) while DUAL Transition type is selected

The transitions may be selected from a range of slide/squeeze/ rotate/split effects,

Page Turn and Roll may be used if the non-linear option is included.

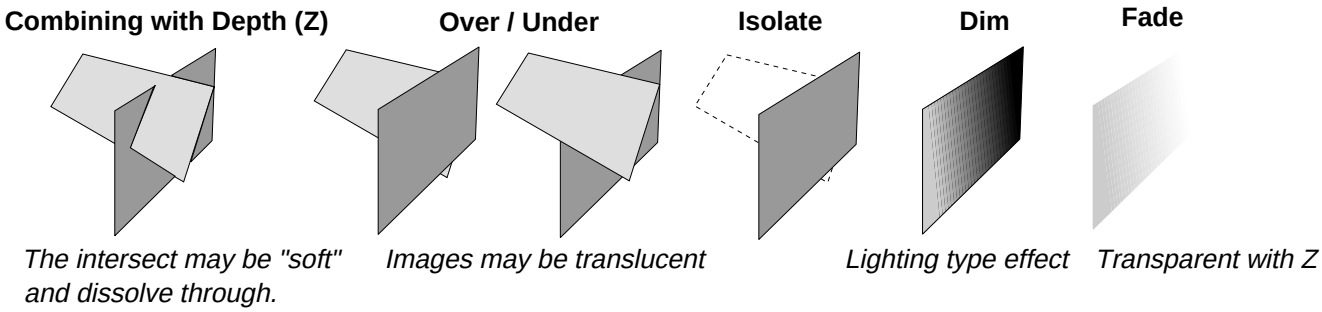
For these effects, borders and angle may be controlled from the switcher wipe area, and *radius* of page turns or *background colour* from the DME menu.

In addition, the user may define their own effects (eg for picture in picture over the shoulder shots) but care should be taken if recursive effects are used with key transitions due to the reversed direction when removing the key - the <User DME> menu shows the run options.

(DME-link operation is now also available with a DVS-6000 using V2.00 software)

Combiner (Option):

Allows multi-channel effects to be built up, with 3D intersections between 4 channels. Dim (video fade) and Fade (key fade) are available.



Variable transparancy and softness may be applied on the combination.

Global control on designated channels allows common or second level motion to be applied. (Note that Global is also effective as a second level motion on single channels systems)

For Tally purposes, the Switcher On-Air Tally menu includes the order of combining channels, but for internal timing / phasing purposes, the DME setup menu includes the order of combining recognised channels.

Note that the On-Air Tally menu also identifies, to the switcher, where the DME inputs can be found for DME Wipe / Link operation, and for control of Aux bus selection.

Input Options:

The 625 DME-5000 may configured for serial digital component video input (and key) or for both Analogue and Digital inputs. External control of a routing matrix (eg Aux bus on DVS-8000C) provides for A-B input switching during a rotate.

Switching Analogue <> Digital is not possible within an effect.

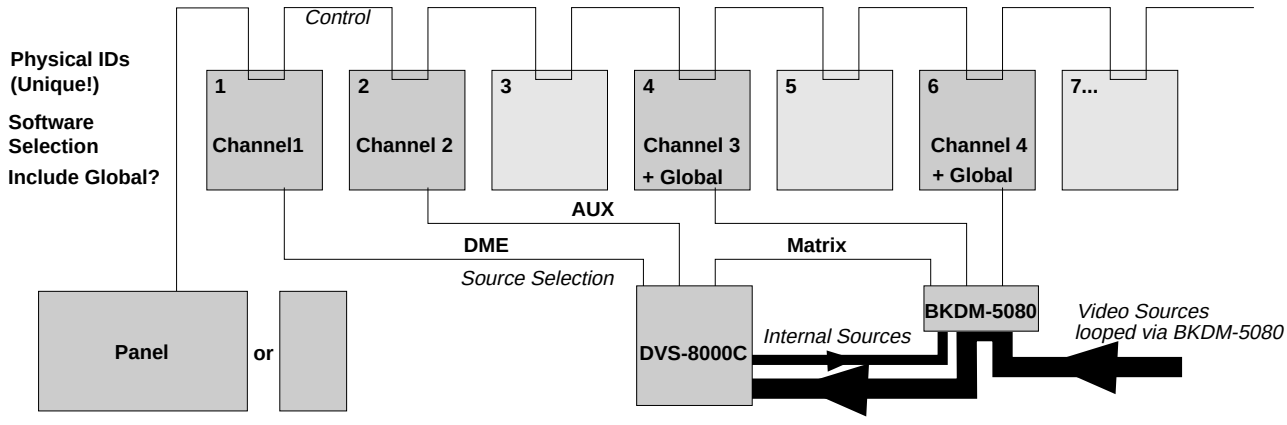
Control:

The BKDS-8010/11 or BKDM-5070 may be used to control upto 4 channels simultaneously.

Each channel must be set with a unique physical address on the CPU card

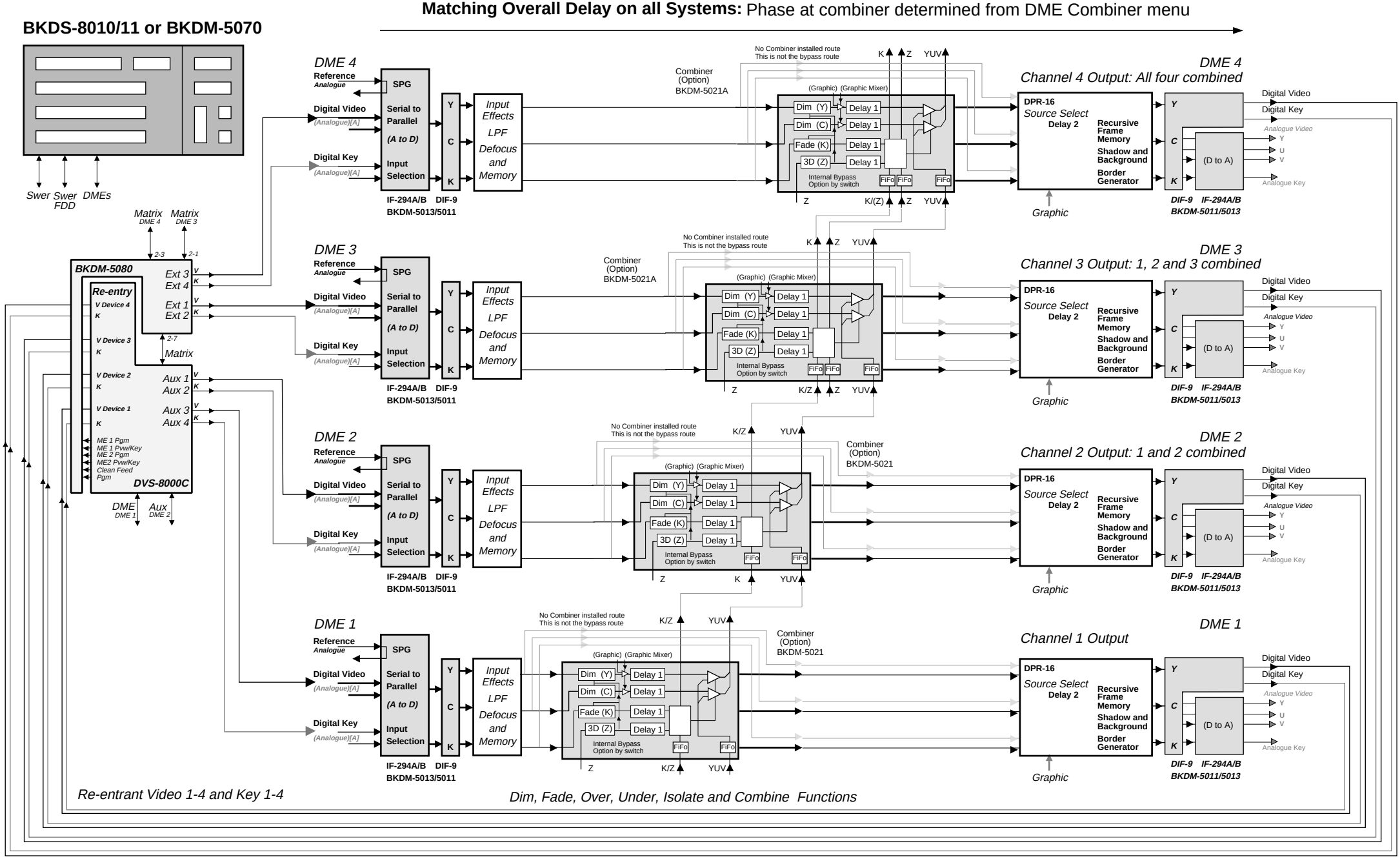
A single loop through control links the panel to all DME channels

Individual cables from each DME go to the Switcher mainframe for DME/Aux bus control.



Technical Training

DME-5000 Cascading Combiners (Old and New) and BKDM-5080 Control

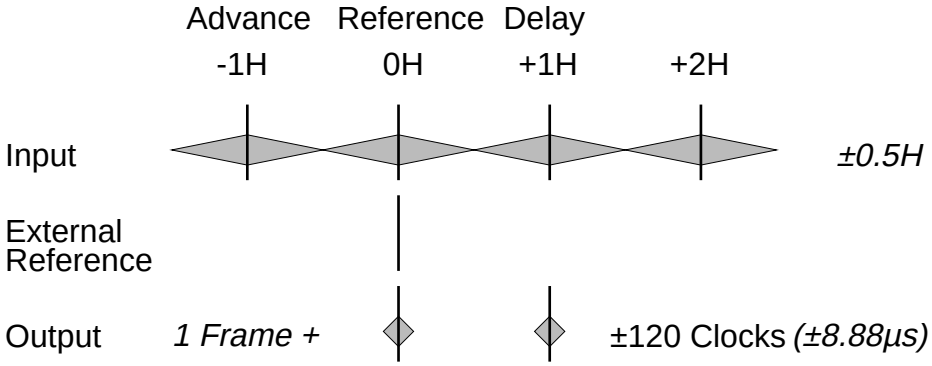


System Timing

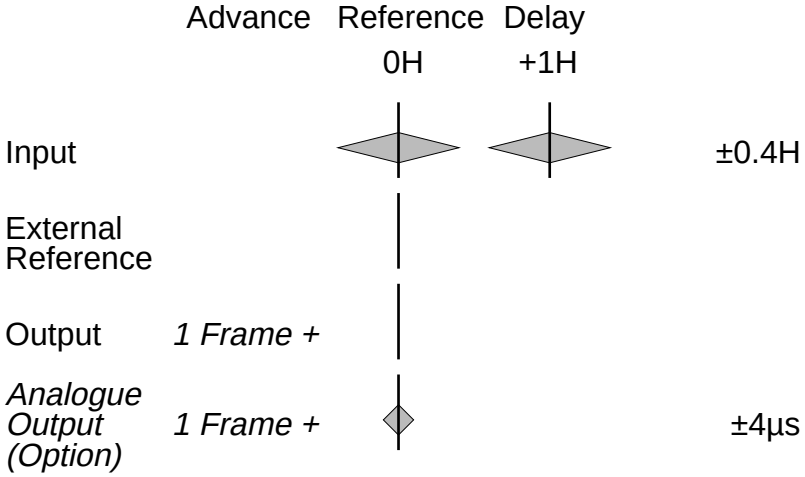
Nominal delays are:

1H for DVS-8000C Vision Mixer and BKDM-5080 routing matrix
1 Frame for DME-9000, 1 (or 2) Frames for DME-5000
DME delays may be reduced by 1H to match delayed inputs from DVS etc.
DVS-V1616 = 44ns DVS-V3232 =42 to 50ns DVS-V6464 = 48 to 80ns (D1)

DME-9000



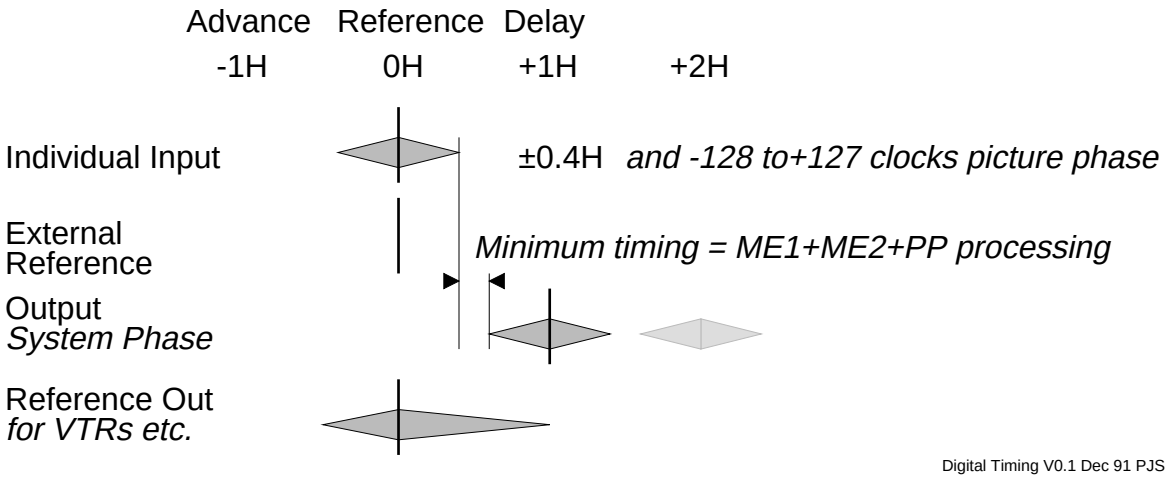
DME-5000



Combiner Operation

The phase at the combiner of each unit is controlled by the combining order menu.

DVS-8000C

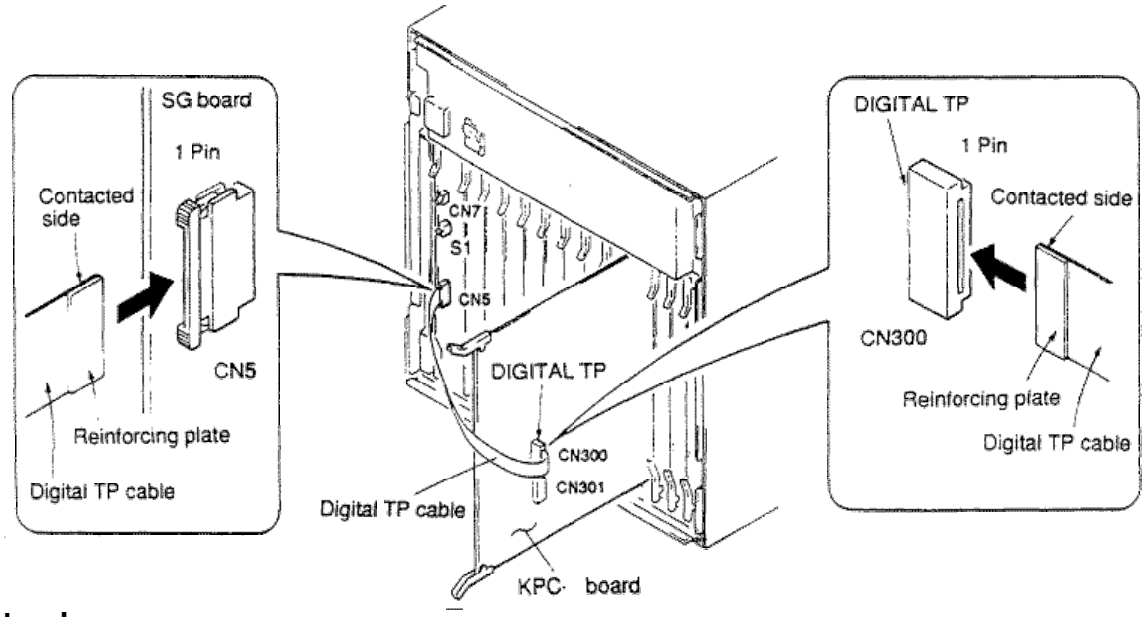


Digital Test Leads

An increasing number of products incorporate Digital Test Points, and provide a supporting D to A Converter, allowing a purely digital signal to be interpreted on an oscilloscope, thereby allowing confirmation, or otherwise, of correct operation.

Slight variations exist between the implementations, in that some provide a manual adjustment of D to A clock phase, while others include a suitable clock frequency and phase within the Digital Test Lead.

Note that many of the numbers being converted may have had positive and negative values, and not all of the original bits may have been converted, resulting in "split" ramp waveforms or apparent repetition; therefore comparison should always be made to known normal operation.



Part Numbers:

Digital Test Lead (Flat foil cable with 13 conductors) J-6186-270-A

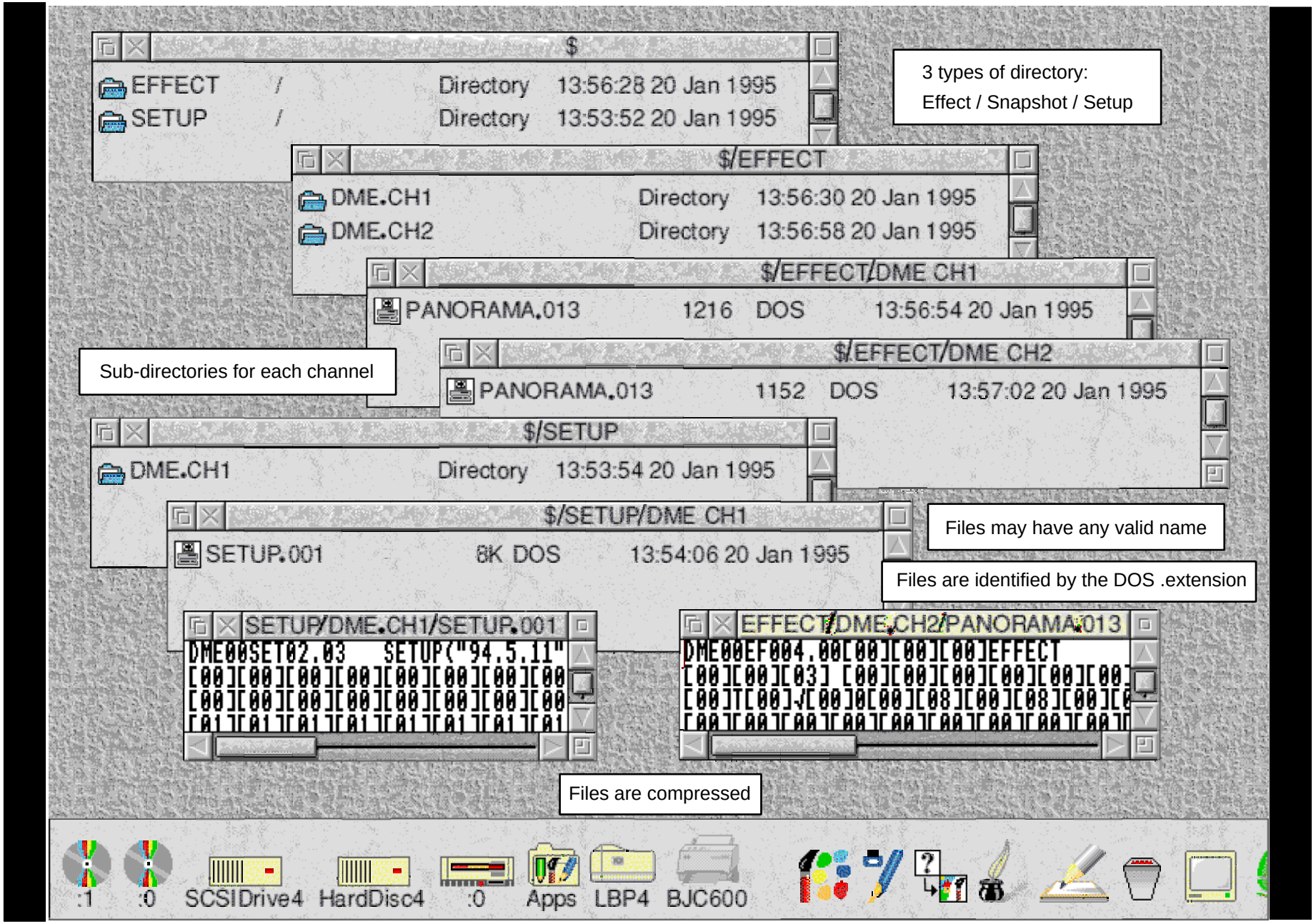
UM - BNC lead (D2 RF test lead / DVS-8000C test lead) J-626-436-0-A

2part lead set:

"Betacam" connector / SDI Monitor / DVS-6000C /DVS-2000C test lead 1-690-351-11

Matching converter to BNC socket (to be attached to BNC lead) 1-569-711-11

Directory Structure DVS/DME Version 4 Software



Serial Digital Interface

Serial Digital Interface

PDF Edition

Serial Digital Interface (SDI)

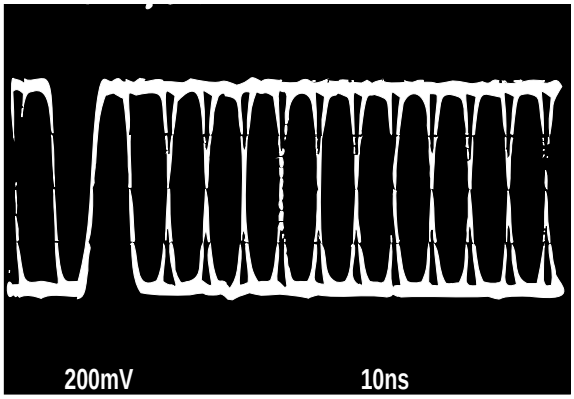
The DVS-6000C is one of a series of totally digital vision mixers from Sony, all of which utilise a common Serial Digital Interface. In conjunction with Digital Betacam, DNS still store, DME series digital effects, DVS serial digital routing matrices etc this allows the signal to remain completely digital from camera to transmission.

The Technical Training Department has produced two explanatory tapes on SDI.
The first explains the principles of the system, and the second is concerned with the new requirements for test and measurement.

These tapes are normally used during this course, and are also available for purchase.

For Routers and Vision Mixers, the use of a single, compact, standard connector allow for compact designs and installation, with a minimum of timing or other problems introduced by differing path lengths with large parallel connectors.
However, once inside the Vision Mixer, the signals will be processed in parallel by passing a 10 bit wide multiplexed UYVY signal at 27MHz, or parallel processing of Y and chroma at 13.5MHz. Both the DVS-6000C and DVS-8000C offer 24 internal buses, and this occupies more than 240 pins! Wipe key signals are also passed in parallel at greater resolution.
Therefore a second serial system will also be used - to control each board and IC..

Serial Digital Interface Summary
Signal Levels and Specifications:



Impedance *75Ω*
Amplitude *800mV ± 10%*
Offset *0 ± 0.5V*
Connector *BNC 75Ω*
Channel Code *Scrambled NRZ*

D1 Format 4:2:2 Signal Transmission

Bit Rate *270 Mbaud* (27MHz x 10 bit words) *Y:U.V at 13.5 : 6.75 : 6.75 MHz*

TRS SAV *(Start of Active Video)* *"FF, 00, 00, XY"* (4 words included in blanking)
EAV *(End of Active Video)* where XY identifies SAV/EAV/field etc

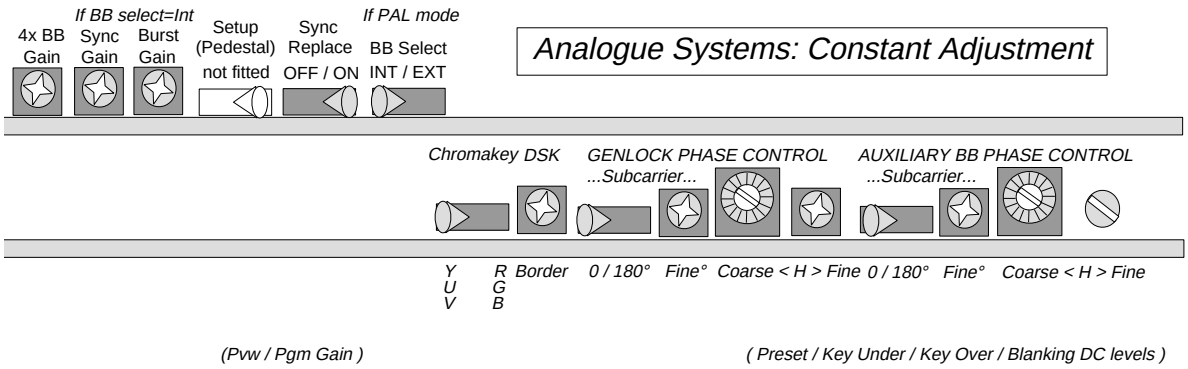
Digital Blanking Period = *276 Words (1440 - 1715)*
Digital Active Line = *1440 Words (0 - 1439)* Total = *1716 Words*

Note that "Digital Blanking" is narrower than "Analogue Blanking"; the digital picture is wider.
PSF1/3 or Belden 8281 cables are commonly used, for runs of upto 200m approx.

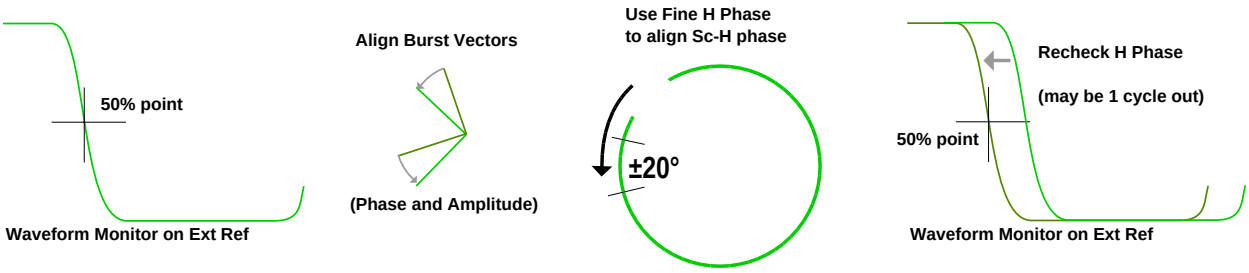
Connecting Units together

The Sony Serial Digital Interface, now an accepted as part of ITU(CCIR) Standard 656 was developed to overcome the limitations of existing systems whose problems could include timing, distance, degradation, and cost.

Analogue

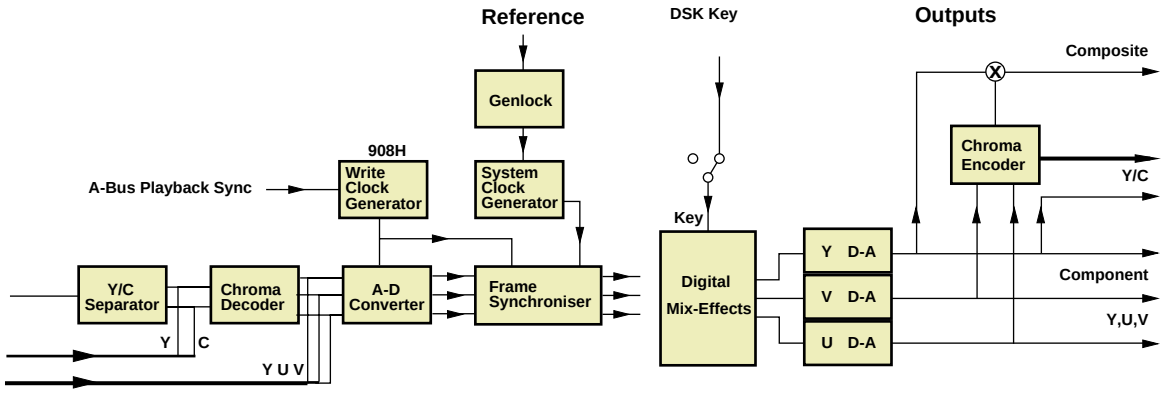


The limitations of composite video distribution were well known, and individual devices were forming islands of digital processing to avoid signal degradation during processing.



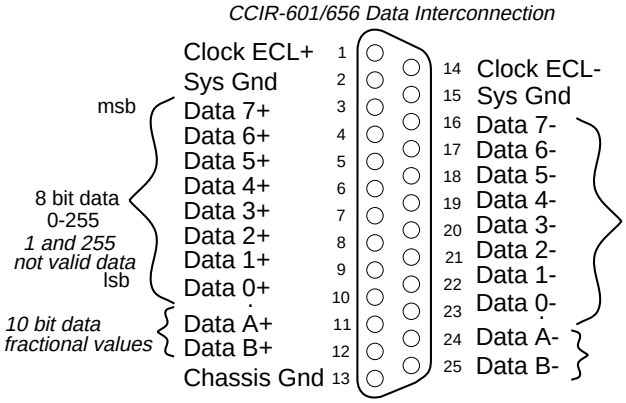
Hybrid

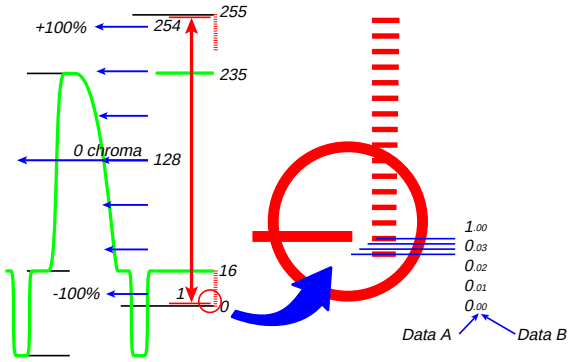
The precise timing required for each signal into a mixing point, and problems with Subcarrier to Horizontal phase could be overcome with "input TBCs" or precision control systems, but there still remained the increasingly frequent decoding and recoding of the signal into component form to facilitate effects processing.



Component Analogue "islands" for Post-Production became popular, but the costs of linking together to complete the transmission chain were high, and imbalances in the tripled cabling and distribution could produce noticeable colour casts or registration errors.

Parallel Digital





27MHz 4:2:2 video: C_b Y C_r : Y : C_b Y C_r : Y

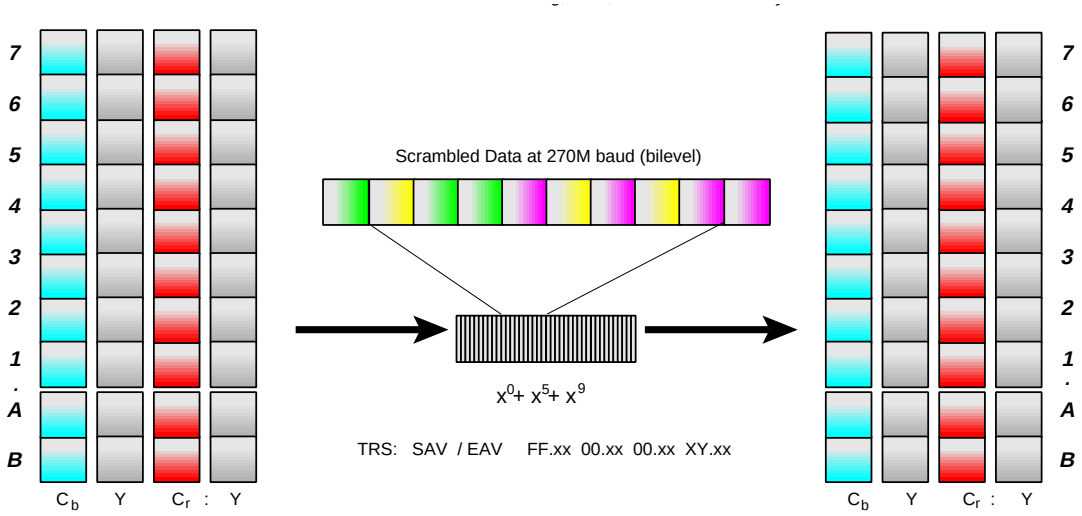
27MHz Key: 0 : K : 0 : K : 0 : K : 0 : K

27MHz Key/Z Z_a : K : Z_b : K : Z_a : K : Z_b : K

220 levels for luminance (Black to White)
235 levels for chrominance (0-100%)
0 chrominance = 128
720 Active Y samples per line
No half-line blanking (Orthogonal structure: no sloping scan lines)

The ITU (CCIR)-601/656 (EBU 3267-E) interface standard defining the digital data format, as used between D-1 recorders and many effect boxes, was also used for parallel cabling within a small area. Problems with slewing of the parallel data and the bulk of the cables limits distances to a few metres, whilst the 25 pin D-type connector prevented compact unit design for devices with a significant number of inputs.

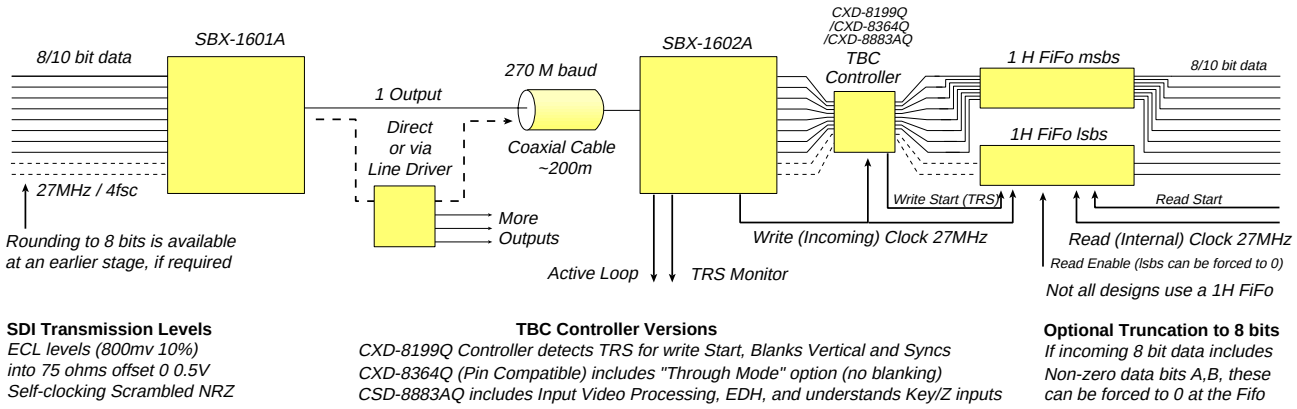
Serial Digital



If the existing parallel data could be serialised, and transmitted down existing Coaxial cables, then this would produce a compact, economical system which would allow entire production centres to remain digital throughout.
If at the same time, space could be found within it, to embed digital audio data, then large economies on cabling could be made, and installation design simplified.
This, in essence, was what the Sony Serial Digital System was designed to do.

The extended 10 bit format of 601/656 (8 bits plus 2 "optional Data bits" offering ½ and ¼ level steps A and B) was allowed for, with the existing restriction of not allowing the reserved words formed by all (the most significant 8) 1's and all 0's to be a valid part of the data, but used to provide a unique timing reference signal (TRS) or digital equivalent of a synchronising pulse.

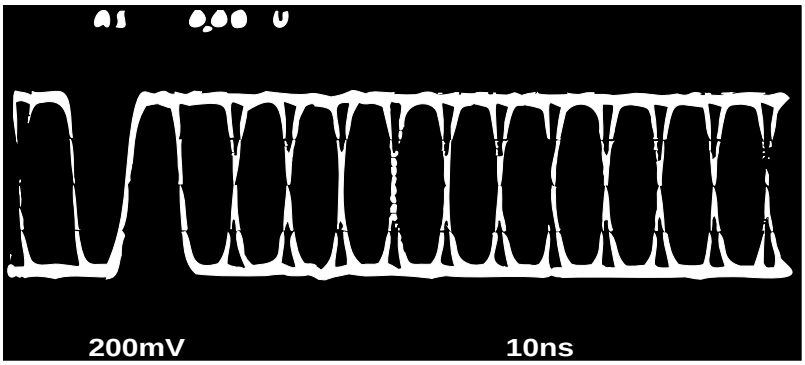
The Overall Structure of a typical Serial Digital Link



By choosing a simple clock frequency of 10*x* the basic data rate {4*x* f_{sc} for NTSC and PAL data} or { 27MHz for interleaved 13.5MHz / 6.75MHz / 6.75MHz component data in 525/ 625}, the SDI components could work with the entire range of signals expected in standard definition.

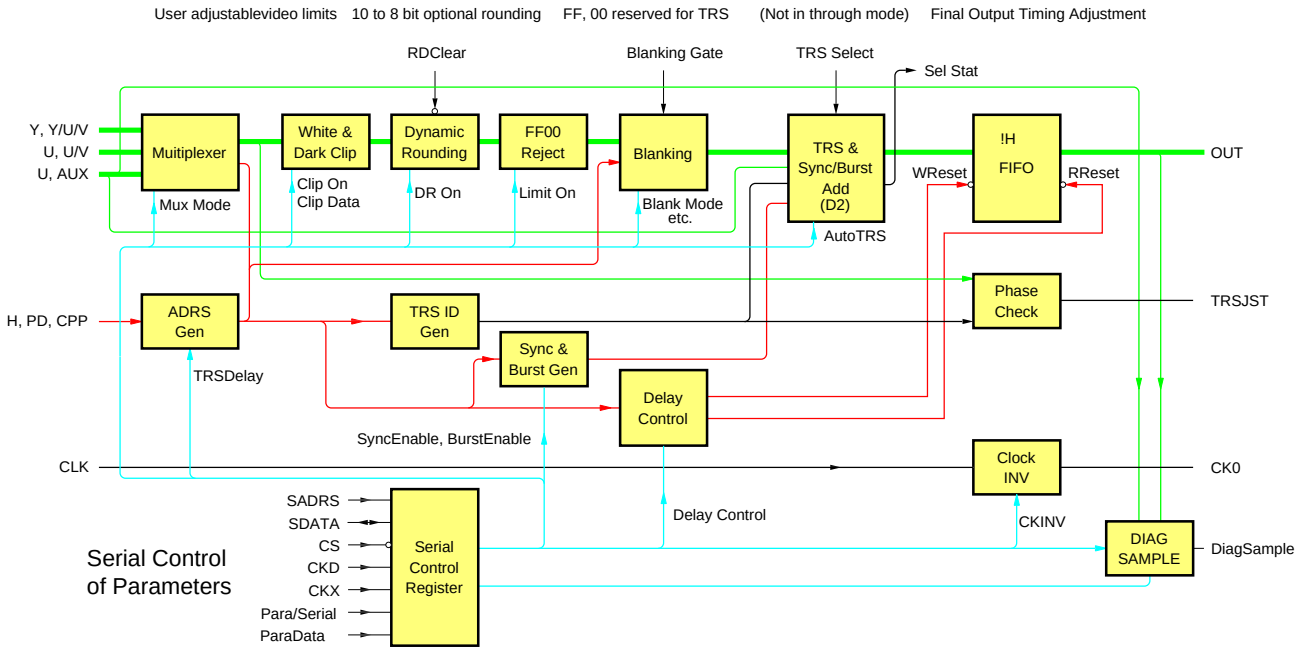
A synchronous datastream using *Non-Return-to-Zero* encoding keeps the basic frequency as low as possible. However, due to the repetitive nature of video data, the data is first passed through a fixed Exclusive-OR scrambling system looking at the 1st, 6th and 10th bits of the data ($x^0+x^5+x^9$), to minimise the possibility of a d.c. component developing, or a particular background illumination producing an unchanging sequence of 1's or 0's so that synchronisation was lost.

For component systems, this results in a basic frequency of 270MHz, with sidebands extending towards 4GHz, and an unaided transmission distance equivalent to 100-200-300 metres of standard Coaxial cable (dependant upon the input design of the receiving device).



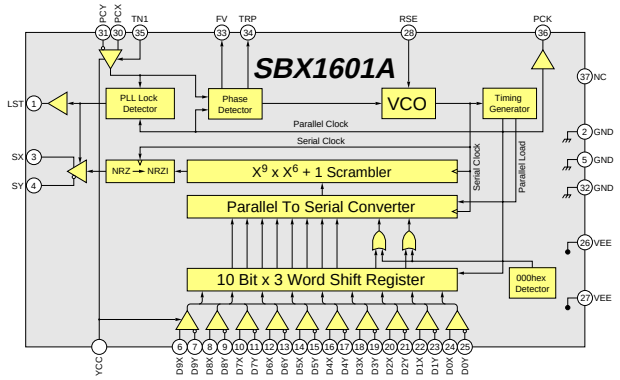
Scrambled 800mV NRZ SDI Waveform viewed on an Oscilloscope.
With a 400MHz bandwidth, little modulation can still be seen
Risetimes will be severely limited. A 4 GHz Oscilloscope is desirable
Although theoretically possible to use "Eye Height" measurements,
it is recommended to observe the "decoded result" using a Wfm-601
(A Wfm-601e could be used to observe and measure the sdi waveform)

Binary level data permitted equalisation to be handled automatically, at the receiving device, rather than being "predictive" at the source.



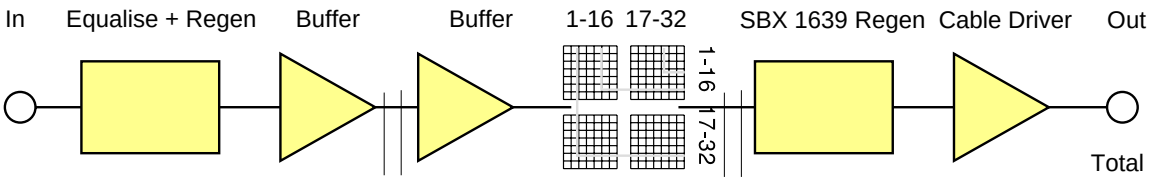
CXD8823Q Digital Video Output Processor (located prior to ECL conversion and SBX-1601)

A single, standard 75 ohm BNC connector is used to provide compatibility with existing cables and the maximum possible density of connectors on equipment, resulting in compact devices, which in turn, lead to more compact installations, and a larger market.



Routing

DVS-V3232



							Total
D1	16	3	4	4 per IC	3	18	48 - 56ns
D2 PAL		3	4	4 per IC	3		
[D2 NTSC]	22	3	4	4 per IC	3	22	58 - 66ns

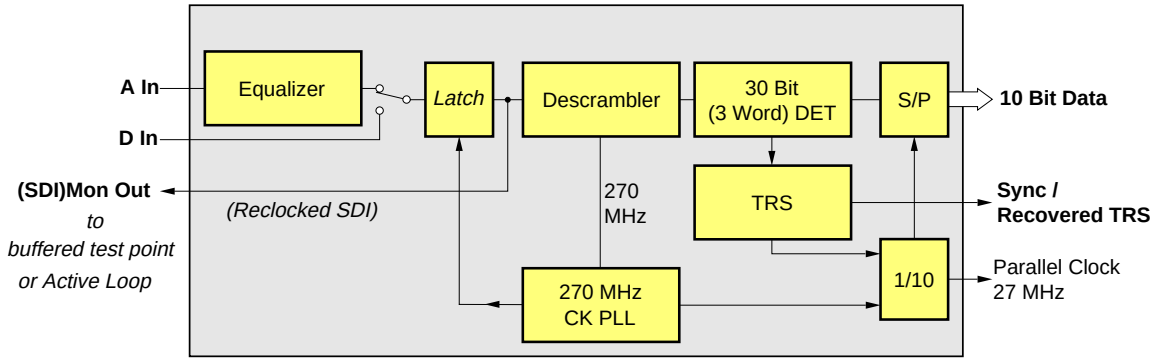
Routing and distribution devices keep the signal in serial form, thus minimising internal wiring, and enabling large numbers of cross-points to be linked together with minimal timing differences caused by differing path lengths.

Products like Vision Switchers (Mixers), VTRs and Effects boxes receive and then translate the incoming data into a parallel form for internal use.

SBX-1602A

The Sony SBX-1602A is used for recovery and Serial to Parallel conversion of the data.

SBX1602A Serial to Parallel Convertor Block Diagram



A Input is for a signal which is likely to require equalisation before recovery, eg after passing down a Coaxial cable
D input: unequalised SDI input - used for on-board selection of locally created signals / separately equalised sources

Serial to Parallel Conversion

The 270 MHz SDI signal is passed as a surface track signal from the rear connector panel. The signal is a.c. coupled by and 75Ω terminated before a surface mount transistor drives the signal into the SBX 1602A.

Internally, the the "analogue" input signal is equalised and reclocked (- the "digital" input bypasses the equaliser, and is for use in short distance "internal" applications).
This is then made available as a monitoring point / active loop - and may be used when checking the existence or validity of an incoming signal without loading the circuit.

The serial data stream is descrambled to return the signal to standard NRZ format, and passed through a 30 bit long buffer. *3FF 000 000* *(10 bit notation)* *or FF.xx 00.xx 00.xx* *(8 bit notation)*

When the incoming pattern forms the sequence 11111111xx00000000xx00000000xx, the TRS position is identified, and the phase to translate the data into parallel form is known.

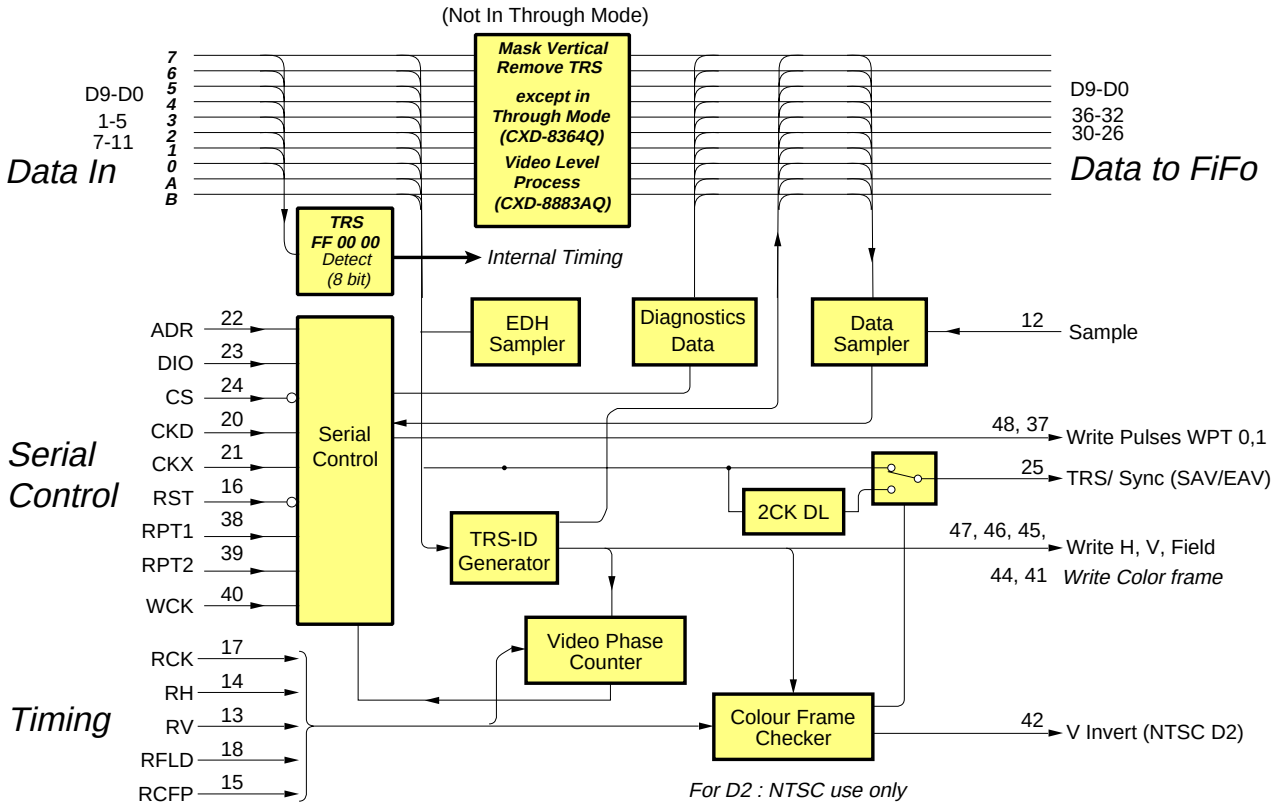
The Timing Reference signal (TRS) identifies the H-start of the incoming line. The following byte contains 1 F V H $P_1P_2P_3P_4$ 0 0 where:
F = field ident, V = vertical blanking ident, H = **S**tart**AV** / **E**nd**AV** (start /end of active video) and P_1 to P_4 are parity on this data *only*.

Timing at the Destination

The digital signal requires extremely precise timing, or errors will be incurred by missing out data samples. This is appears to contradict the basic requirement of an interconnection system which was easy to connect together!

However, *because* of this precise requirement, devices intending to process the incoming signal(s) must "timebase-correct" the incoming data from their original, independently locked clocks, to a single, common clock within the device.

Therefore, once the signal has been received, equalised, and converted to the parallel domain, it is usually sent into a Fi-Fo (often of nominal 1H duration), under the control of a specially designed TBC controller IC, which has detected the incoming TRS signals.



Generic Block Diagram for TBC Controllers

In common with the various adjustments which customers expect to make within TBC processing, and this has been achieved by adopting the processing originally used on the DVS-8000C Chromakeyer board, but within the single TBC IC.

Analogue and Digital Input Boards support:

Input Video Processing:

Video Gain ±200%,
Luminance Gain ±200%
Black Level (Pedestal) -7.3%<>+109.6%,
Chroma Gain ±200%,
Hue Rotate ±180°

(Note that adjustments taking the signal outside the numeric levels available / assigned clip levels will result in hard clipping on a pixel by pixel basis.)

Input Type:
Serial Digital Inputs may be interpreted as:

Video (4:2:2)
Key (4:0:0)
Key-Z (4:2+2) (for DVS-2000C)

Analogue Inputs are digitised as either 4:2:2 from Component Video inputs, or 4:0:0 from key inputs

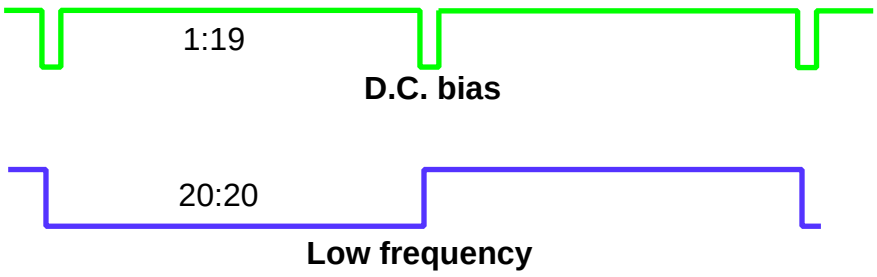
"Colour Bars" and other test signals designed for the analogue domain, do not perform a rigorous test of a link, but only the quality of the A to D and D to A converters in use.

There is also little point in attempting to monitor the SDI signal directly, since any measuring device will load the signal causing errors, and a very large bandwidth would be required.

However, the Sony SBX-1602A does provide an SDI Monitor output, which is either connected to an on-board buffered test point (Eg DVS-8000C/6000C), or provides the "Active loop" signal seen on other equipment (BKDF series, DVWs, DNWs, DVS-2000C).

As a direct result of the coding system used, two particular test patterns have been developed, in order to "stress test" an SDI link.

Pathelogical Test Signals for SDI (shown in SDI domain)



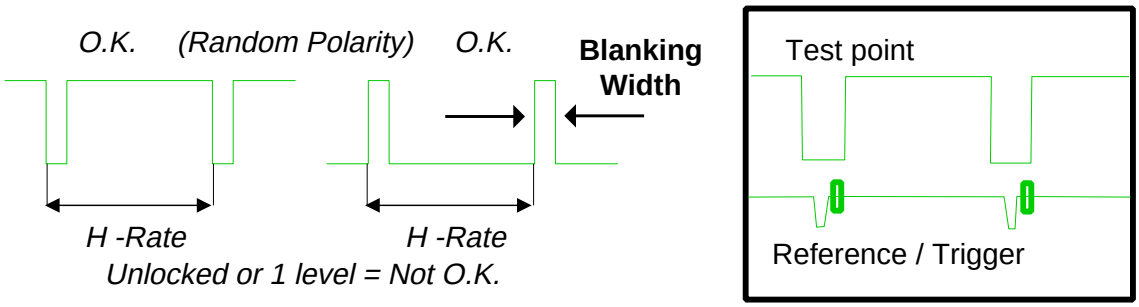
After coding, these signals produce "worst case" dc component and low transition rate causing difficulty in equalisation and clock recovery. A shallow ramp may also be used.

Simple Input recovery Test

A logic probe or standard oscilloscope can be used to monitor the Sync or "detected TRS" output of the SBX-1602A.

It is useful to compare the signal against a known analogue signal (eg Black and Burst reference) for timing purposes.

Monitoring the detected TRS from the SBX-1602A



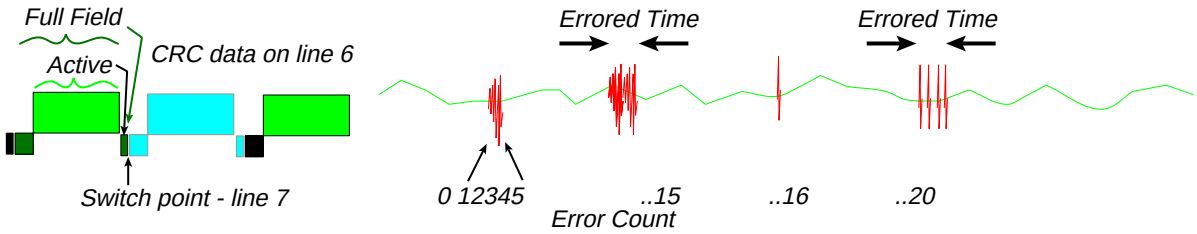
As the use of SDI increases throughout the broadcast programme chain, 16 x9 / 4 x 3 format switchable monitors with integral SDI inputs are are recommended for all new purchases!

Error Detection: **EDH**
The original design of the Sony SDI system was simply a point-to-point transmission system for the audio-video datastream, and offered no error checking on the datastream itself.
The Test equipment manufacturer Tektronix® proposed an enhancement, which would provide error checking on the data segments or the overall signal, and this has since been incorporated into the standard.

The EDH (Error detected Here / Already) system produces a check sums for a field (e.g. the whole field, or only active video area) which is placed into the beginning of the following field, (line 6 for 625 systems), at a point prior to the standard switching line of routers (line 7 for 625 systems).

Devices are therefore capable of knowing that incoming data is error free, or not, and by inserting the appropriate check sums and flags on the output side, can advise any following devices of the integrity of the transmitted data.

"It's alright leaving me", *or not!*



With suitable systems, incoming errors may logged against time or source, and produce an accurate, qualitative, assessment of perceived degradation for contractual or maintenance purposes

SDDI

Having created such a useful, wide bandwidth, routeable point to point distribution system, the possibilities of conveying other forms of data presents itself.

Within the existing SMPTE approved format of SDI, Computer data, compressed video, or other information could be multiplexed into the datastream, and routed directly to its destination, in real time.

Single-occupancy, point-to-point distribution avoids / minimises the bandwidth bottlenecks associated with traditional computer networks, especially when the News programme is about to go On-Air

By moving away from copper wires, the distances over which the data is transmitted could be increases dramatically too.

Applications

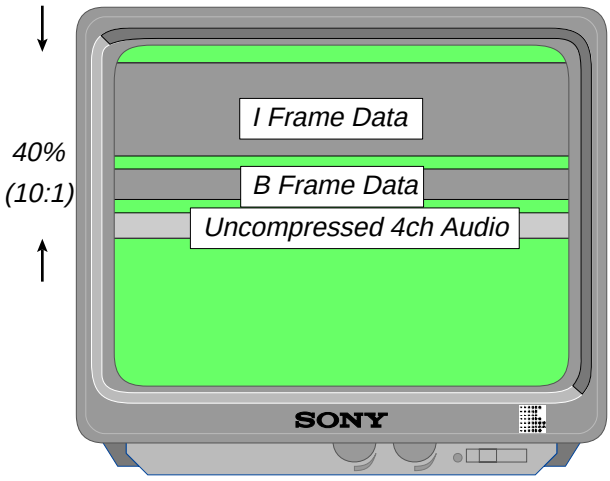
Within the Audio-Video environment, Sony has introduced two applications of SDDI distribution over SDI links:

DV / DVCAM

The widely adopted domestic / professional videotape format which uses Intra-frame coding for its compression, based around 4:1:1 sampling in 525, and 4:2:0 sampling in 625.
Many of Sony's professional range of DVCAM products include SDDI links to facilitate 4x speed transfer.

Betacam SX

The Betacam SX range provides MPEG compression (Inter-frame) using a 2 frame structure to facilitate editing. The video is easily compressed 10:1, enabling SDDI mode transmission at high speed, currently restricted to 4x by the associated tape or disk hardware, or 2x by Satellite transponder bandwidth.
The Audio is transmitted uncompressed as 4 AES/EBU compatible 48kHz 16bit datatreams.



Betacam SX SDDI viewed on SDI Monitor
(1 frame in 4 at 1x Transfer)

In both of these cases, normal SDI monitoring equipment is able to pass the signal through, and permit some interpretation of the integrity of the data.

Serial Control

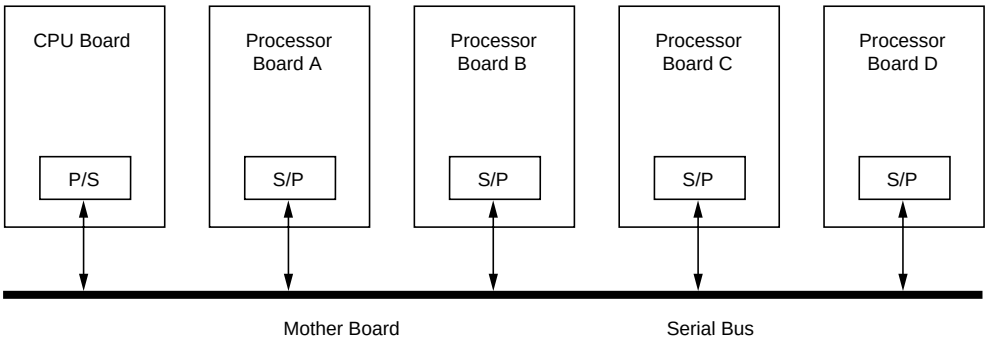
Serial Control

PDF Edition

Serial Control within the DVS-6000C / DVS-8000C

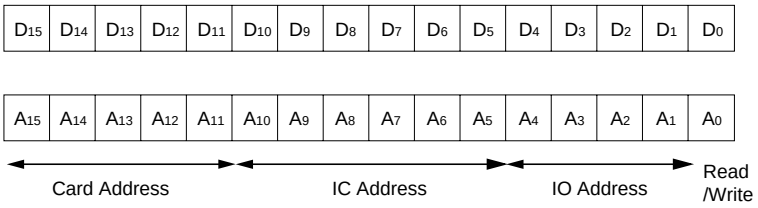
The CPU-147 board performs system control for the DVS-6000C by a 4-wire system using serial address, serial data write, serial data read, and serial data clock lines, which are balanced RS-422 between boards. The format was originally developed for the DVS-8000.

DVS-8000/8000C/6000/6000C SIF Configuration



The address / data clock rate is 13.5MHz (D1) or 2fsc (D2) / 8Mbps

Address and Data Formats

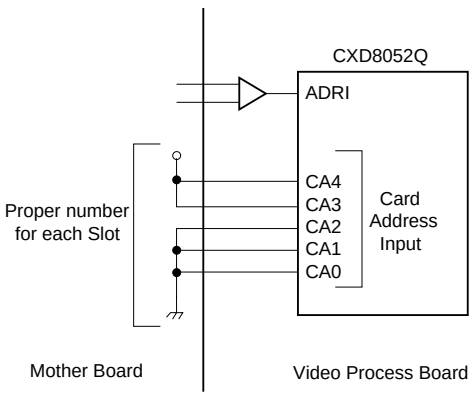


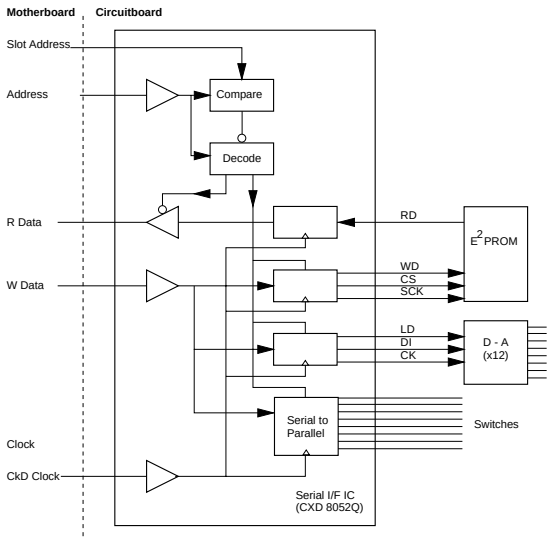
Serial Controller CXD8052Q (80 pin flat)

There are two modes of operation: Master (as found on the CPU board) and Slave (other boards) determined by pin 58 (1=Slave).

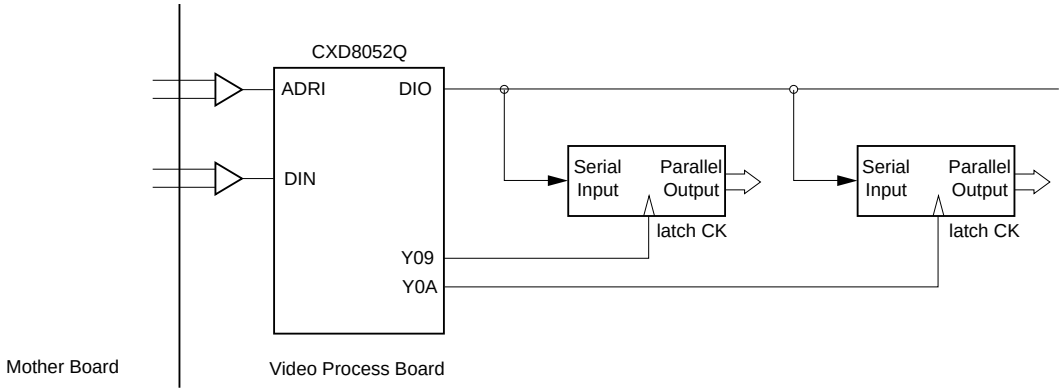
In slave mode board selection is by comparison of the serially transmitted address with a 5 bit parallel slot address. The destination IC address is decoded internally.

Card Address



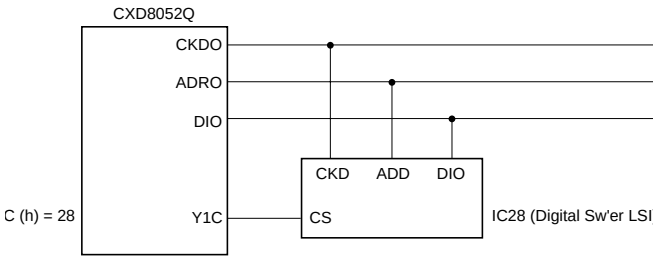


IC Address

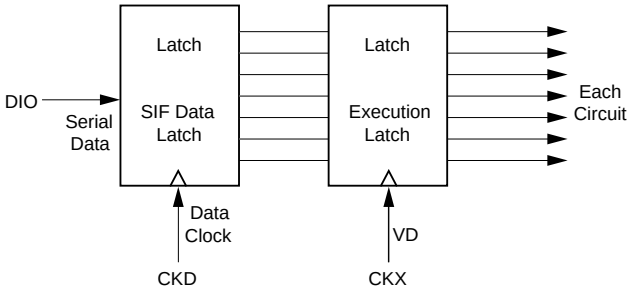


Incoming data is then distributed (in serial form) to the appropriate IC, or collected for forwarding to the CPU as required (eg E^2PROM). Some devices require individual control, chip select, or timing, lines as in the example decoding serial data to parallel form.

IO Address

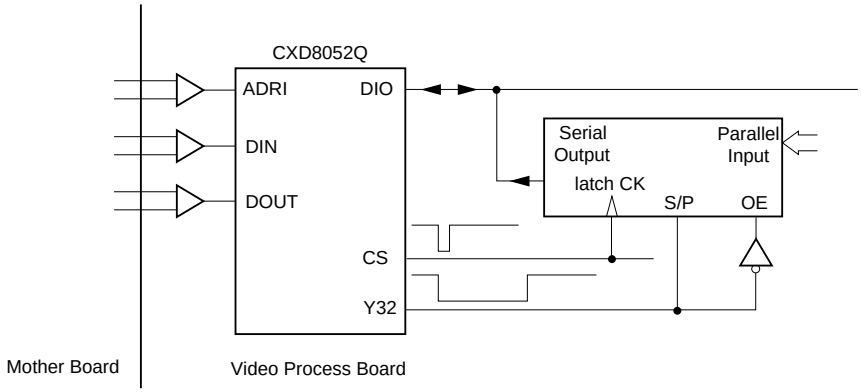


Dual Latch Configuration (Example)



A second latch, triggered by a correctly timed signal (CKX) brings the new settings into use.

Read / Write



The reading ability is currently used for semi-automatic alignment in the factory, and to read the EEPROM values on power up, but able to handle self-diagnosis in the future.

On-board EEPROM

Each board (including piggy-back option boards) carries an EEPROM which is read on power up through one of the CXD8052s on the host board.

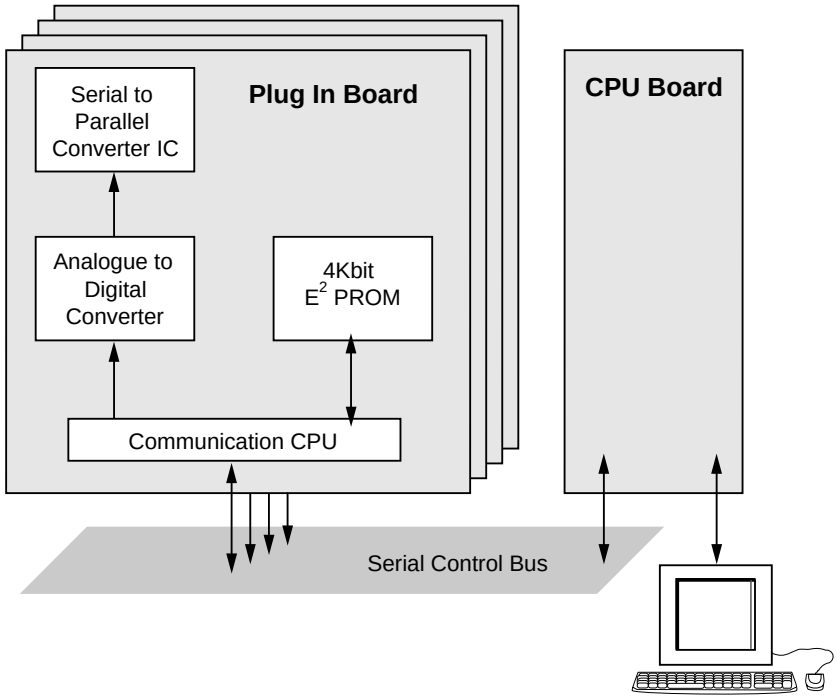
The 512 byte (or 256 x 16) Serial E^2PROM contains:

Control Data:
- *Memory Check Code (Test Pattern)*
- *Card ID (listed on page 1 of notes)*
- *Format D1/525, D1/625, D2NTSC, D2/PAL*
- *Board Control Data (switches and levels for D-A)*

Product Information
- *Company/ Production Year/ Board Name/ Version*
- *Country of Origin/ Designers Name*
- *Option name*
- *Lot (Batch) No./ Serial Number*
- *Type of Product/ Category/ Destination*
- *Product Number/ Assembly Number/ Part Number*

Service Information (Ascii) *Technical memo number*

Board EEPROM Configuration



It is intended that Service Information be entered via the rear RS-232C port in the future. At the factory, this method is used to progamme preset values on each board.

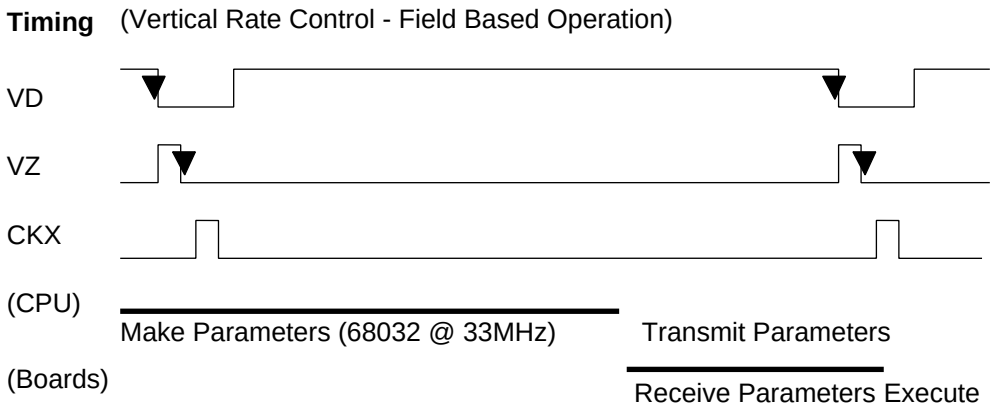
Software update on the DVS-6000C is via floppy disc on the control panel into flash ram, making the distribution of software upgrades both fast and more economical.

Since the same 9-pin cable is used for normal control, this is not guaranteed during software updating or other floppy disc operations - (there may be a delay in responding to buttons etc)

The software on the control panel is kept in sync by supplying a reference on otherwise unused lines in the cable - all 9 pins must be connected!

The 50pin Amphenol SCSCII interface connector is not yet supported

Serial Control Concept



Possible Failure Modes:
If no VZ the CPU software is likely to fail
If no CKX, then the boards will fail to respond (ie action) commands

Serial Control data arriving too late to be actioned in the 'correct time frame' will be processed and actioned in the 'next' field, and not forgotten.

The dual 7-segment display on the front of the CPU card increments as a 'byte count' of received data. This provides a simple visual check on communications from the panel to the mainframe, since each time a function is operated (eg a fader arm is moved), the display will respond.

Interrupt Priorities:

1	NMI (Switch on front of board)
2	VD (in VZ derived form)
3	Counter (software starts transferring data to boards)

Hardware diagnostics:

Serial Interface to intelligent boards with 2 way communication

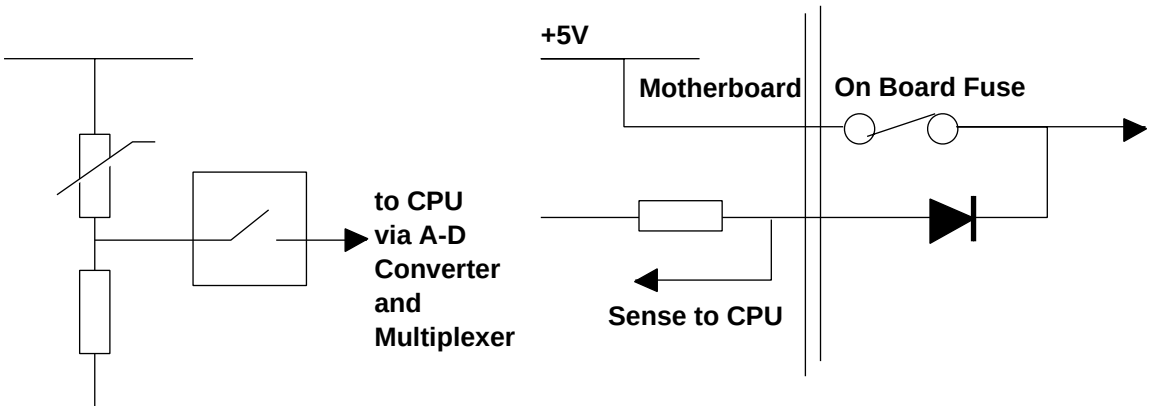
Power Supply Voltage Sense
Power Supply Cooling Fan(s) Stopped (Tach pulses from fans)
Power Supply Temperature (Thermistor in Power Tray)

Board Temperature Sense (Thermistor on each board between connectors)
Board Power Fail with Fuse Open Detector

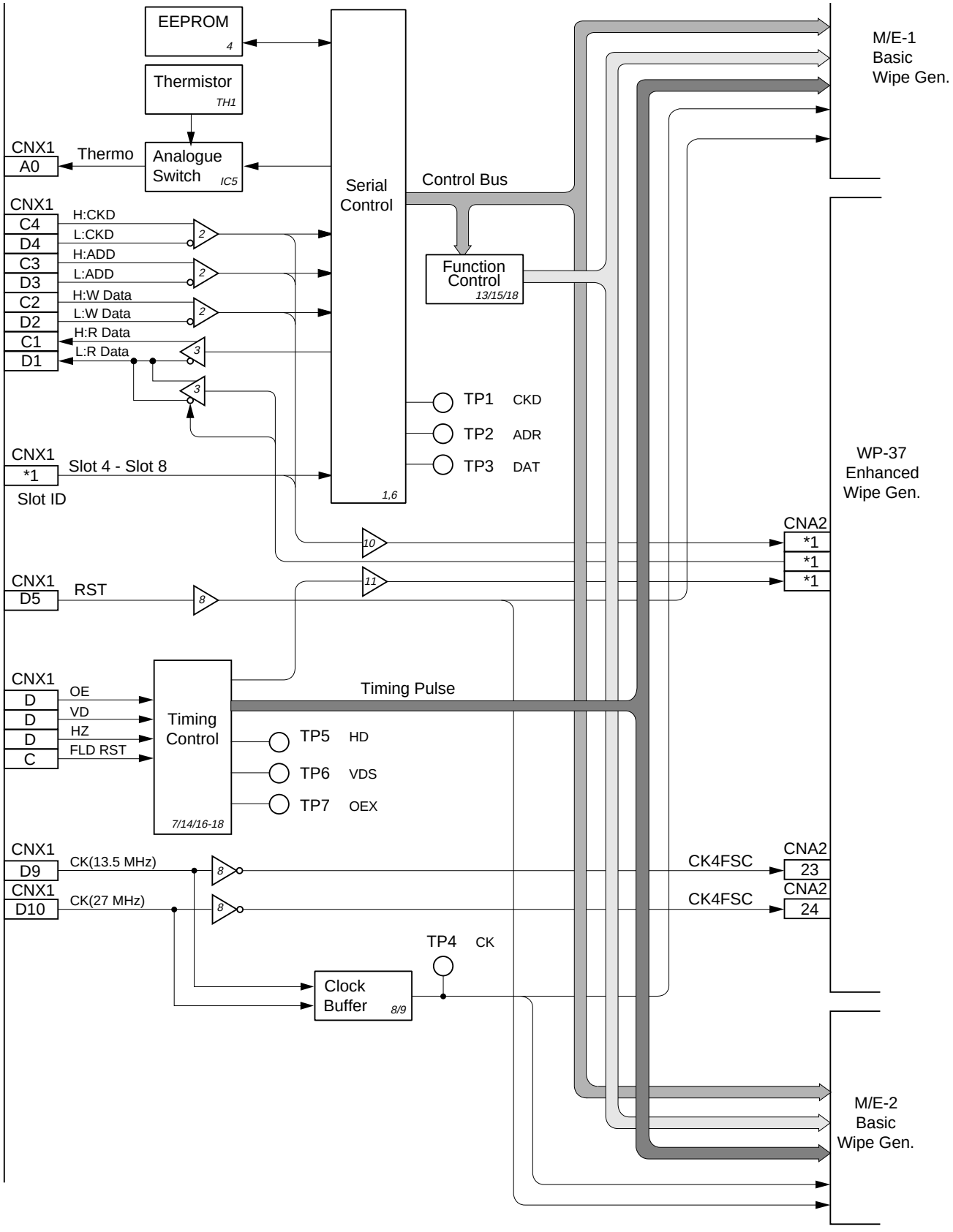
Reminder: The panel requires a synchronising reference within 10H of the mainframe

CPU Board Edge LEDs

- Term
- Panel
- Edit 1
- Edit 2
- DME (1)
- Aux (2)
- FDD
- MTX (3+4)
- User
- Spare



WKG-10 Board Serial Control Interface

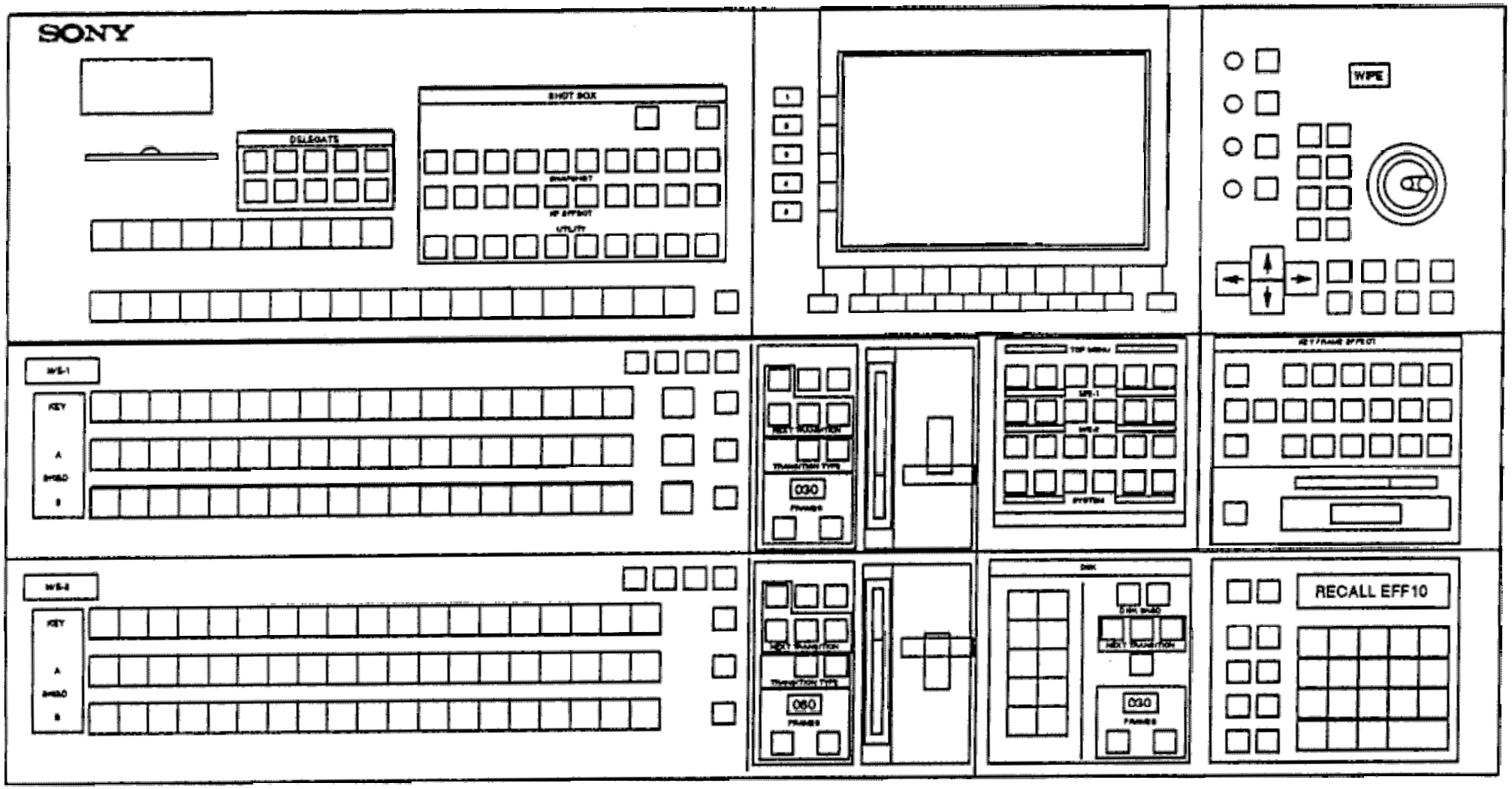


Control Panel

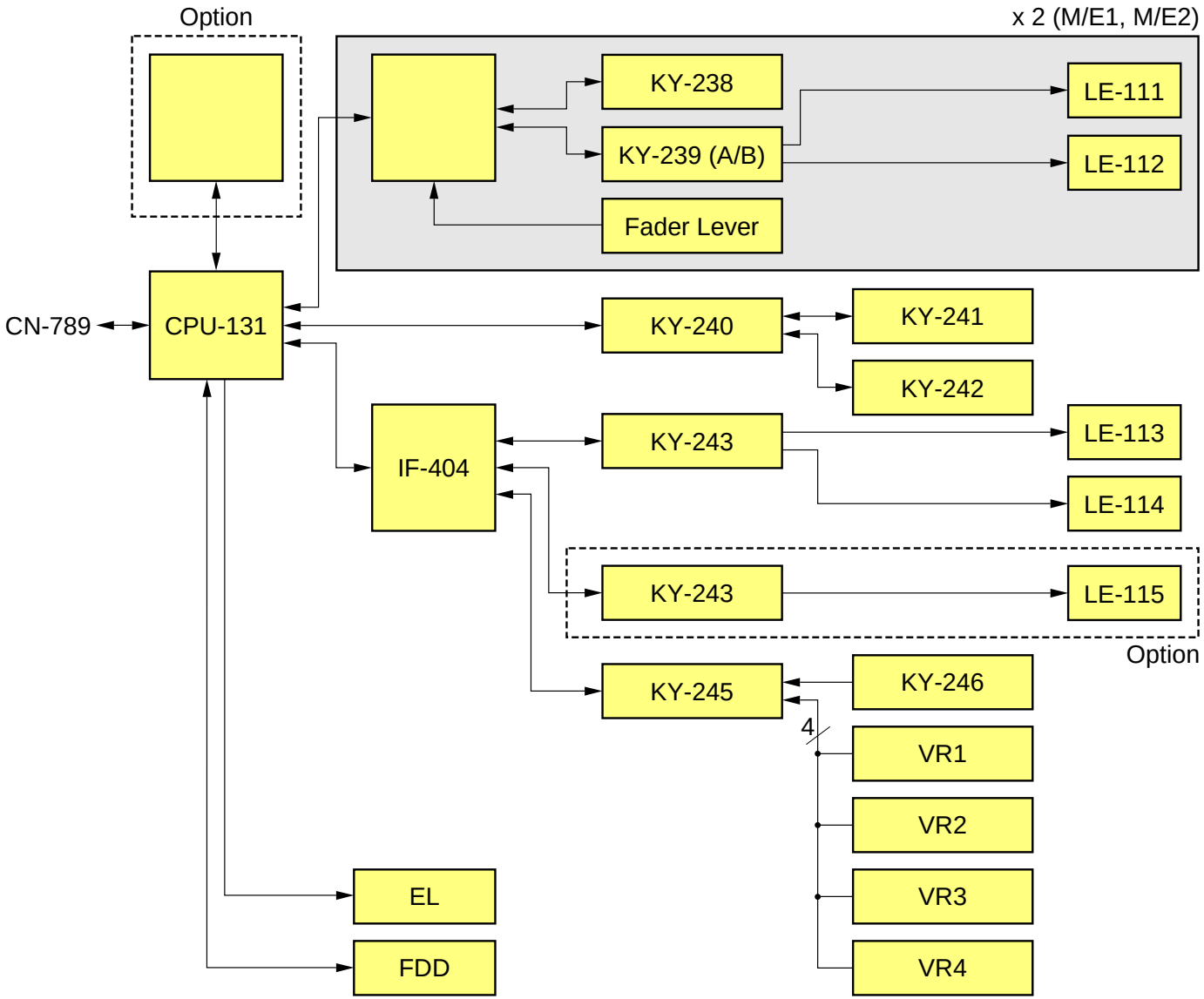
Control Panel

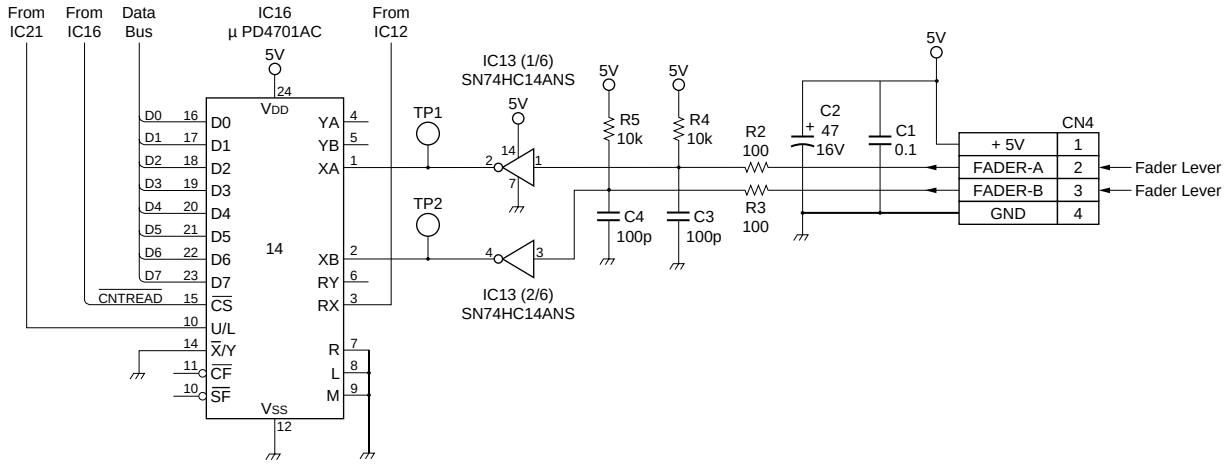
PDF Edition

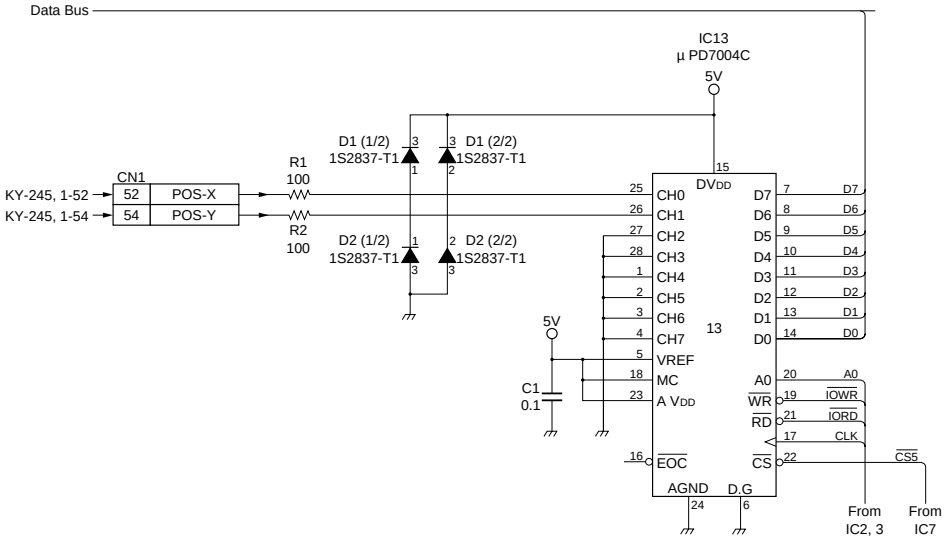
BKDS-6010 Control Panel



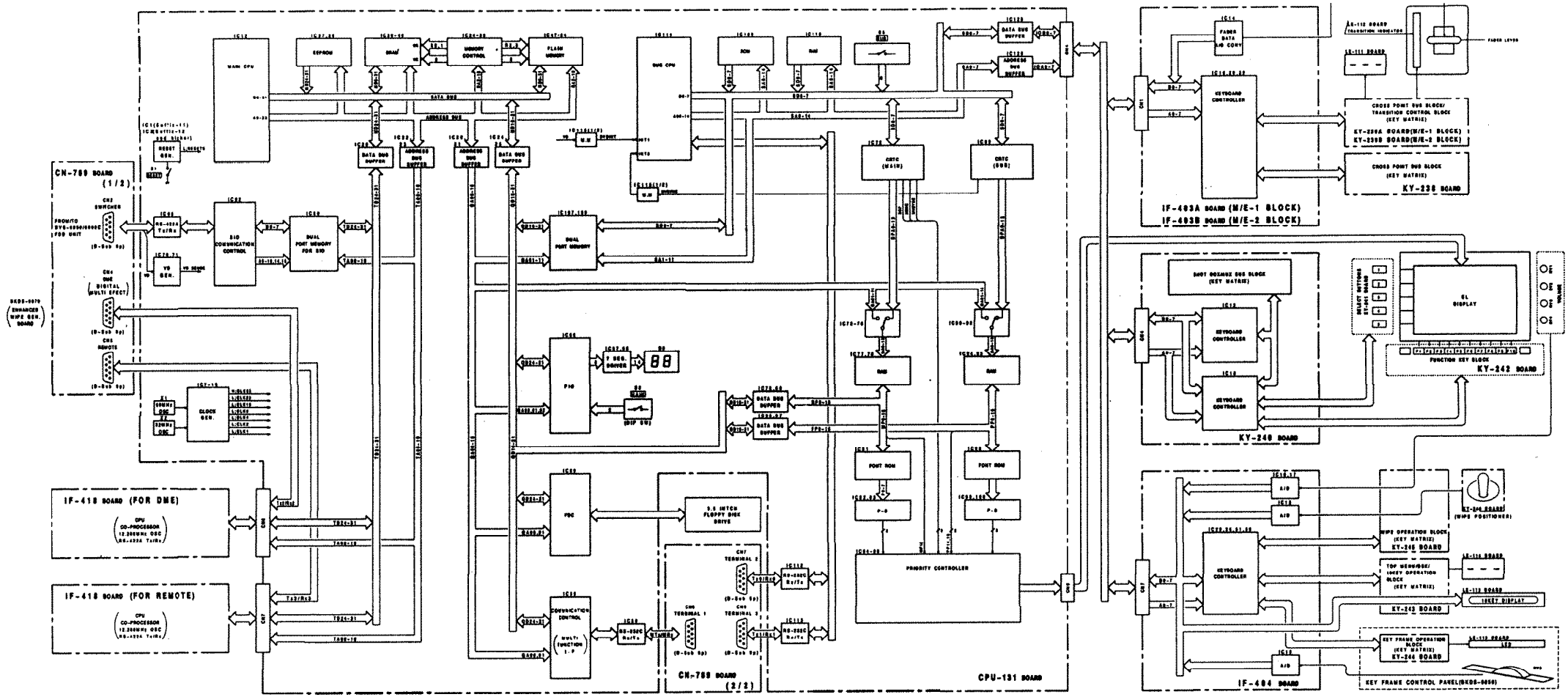
Control Panel




From IC21
From IC16
Data Bus
IC16
µ PD4701AC
From IC12
5V
VDD
24
D0 16
D1 17
D2 18
D3 19
D4 20
D5 21
D6 22
D7 23
CNTREAD 15
10
14
11
10
D0
D1
D2
D3
D4
D5
D6
D7
CS
U/L
X/Y
CF
SF
14
YA 4
YB 5
XA 1
XB 2
RY 6
RX 3
R 7
L 8
M 9
VSS
12
TP1
TP2
IC13 (1/6)
SN74HC14ANS
IC13 (2/6)
SN74HC14ANS
14
7
2
1
4
3
R5
10k
R4
10k
R2
100
R3
100
C2
47
16V
C1
0.1
C4
100p
C3
100p
CN4
+ 5V 1
FADER-A 2
FADER-B 3
GND 4
Fader Lever
Fader Lever


Data Bus
IC13
µ PD7004C
5V
D1 (1/2)
1S2837-T1
D1 (2/2)
1S2837-T1
D2 (1/2)
1S2837-T1
D2 (2/2)
1S2837-T1
R1
100
R2
100
CN1
KY-245, 1-52
KY-245, 1-54
52 POS-X
54 POS-Y
DVDD
15
CH0 25
CH1 26
CH2 27
CH3 28
CH4 1
CH5 2
CH6 3
CH7 4
VREF 5
MC 18
A VDD 23
13
D7 7
D6 8
D5 9
D4 10
D3 11
D2 12
D1 13
D0 14
A0 20
WR 19
RD 21
EOC 16
CS 22
CLK 17
IOWR
IORD
CS5
AGND 24
D.G 6
C1
0.1
From IC2, 3
From IC7

BKDS-6010 Control Panel Block Diagram



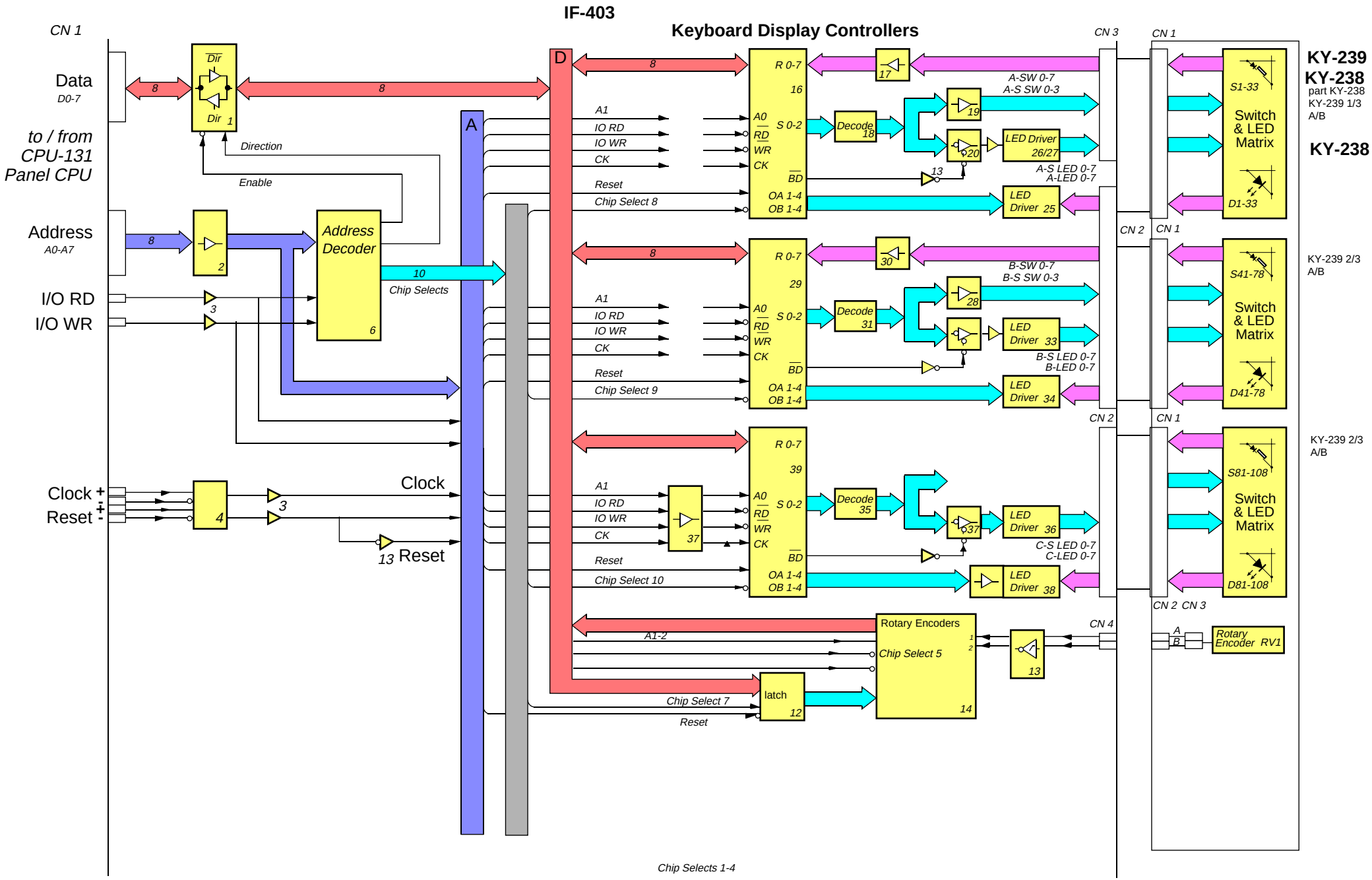
V2.00+ Software Switch Settings:

Version 4 software is required on the BME-5000 for DME-link
Version 1.40 software is required on the DME-3000 for DME-link
A Graphics tablet may be connected to Terminal 2 of the BKDS-6010
The Wacom UD-0608R tablet and UP-201 pen is recommended
(Page 10-7 of the BXS-6020 User Guide gives connection details)

BKDS-6050 Keyframe Option IF-418
(to "Matrix" on DME-5000 / "Switcher Panel" on DME-3000)
Change all 4 jumpers in area A from "Master" to "Slave"
A "Dongle" supplied with the BKDS-6050 must be inserted
at the DME-3000 "Switcher Panel" connector end of the RS-422

Technical Training

BKDS-6010 Control Panel Extract: IF-403 / KY-238 / KY-239



Input Boards

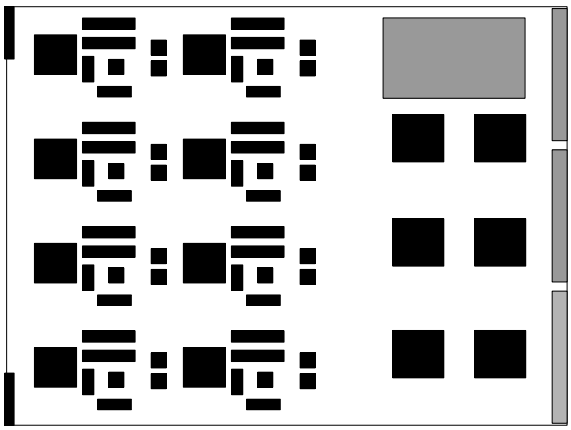
XPT-2, XPT-3, XPT-4 / AD-107

PDF Edition

XPT-4 / AD-107
XPT-2, XPT-3,
Input Boards

XPT-2/3/4 and AD-107

- # **Serial to Parallel Conversion using the SBX 1602 A (or A to D Conversion)**
- # **Automatic input Timing Adjustment using the CXD 8364Q/8883AQ Timebase Controller**
- # **Crosspoint Selection (8 x 8) using pairs of 5-bit wide CXD 8258Q**



The XPT 2 board is the serial digital input board used by the DVS-8000C. (The XPT-1 board is for 525/D2)

BKDS-8022

The XPT-3 (universal) board, is available as the BKDS-8022 option for the DVS-6000 and DVS-6000C.

The XPT-3 board supports "through mode" in conjunction with direct output through Aux and Edit Preview.

The test points showing detected "syncs" have been brought to the front edge of the board, enabling verification without the use of an extender.

The XPT-3 board may be used in the DVS-8000 and DVS-8000C with version 3+ software in place of the earlier boards. Some XPT-2 boards have been modified to provide "Through Mode" operation as with XPT-3 boards. XPT-2 boards have been observed to work in place of XPT-3 in 625, but this is not guaranteed.

BKDS-8024

The XPT-4 board additionally allows Video Processing of each individual input, in the digital domain.

This uses a similar technique to that found previously on the CRK-4 chromakeyer for modifying foreground video, but using higher levels of integration, this occupies only a part of the new TBC controller IC CXD8883AQ.

This IC was first used in the DVS-2000C, where it also supports Z-key and EDH.

Since the package size has increased to 52 pins from 48, it will not be possible to upgrade older XPT-2/3 boards to the new faclities by substituting the IC, as could be done to support "through mode" on XPT-2.

BKDS-8023

The AD-107 board accepts two YUV analogue component signals and 2 analogue keys (Y,U,V / K / Y,U,V / K.)

Sync timing for the YUV input may be selected from the signal itself or from the Vision Switcher's reference.

Sync timing for the key input may be from the key itself, its associated YUV input, or Switcher reference.

The input signal is 75ohm terminated at Rx03 TPx0,1 and then buffered by ICx01 before low pass filtering to prevent aliasing. IC x02 provides an offset based on digitally detected error. Diode bridge Dx01/2 /Tx01

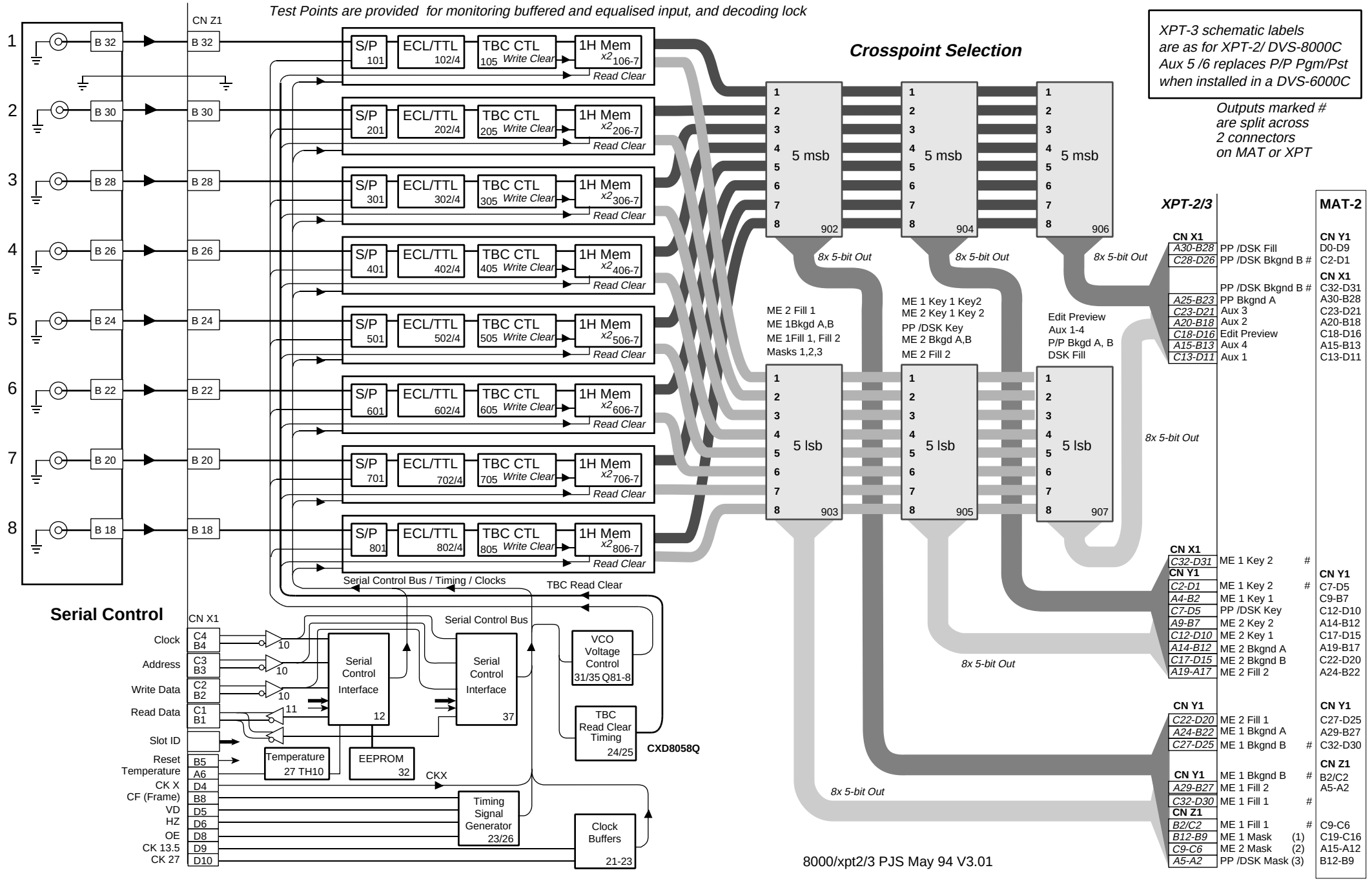
CXD-8274Q CMOS Digital Clock Generator provides the timing signals to the CXA-1577R-9 10-bit TTL 20MSPS A to D converter, and outputs the error offsets. The TBC controller is also the new CXD8883AQ.

All boards share a common Crosspoint Matrix arrangement using 3 pairs of ICs.

Technical Training

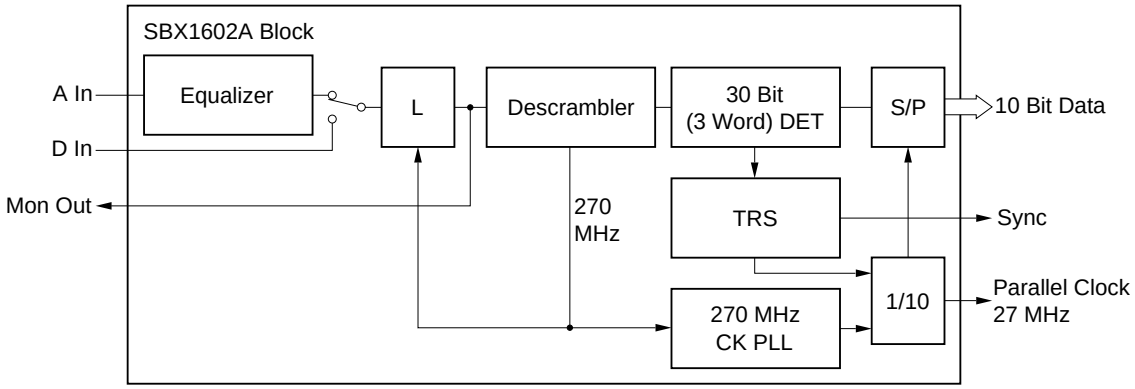
XPT-2/3 Serial to Parallel Conversion Input TBC / Phase Control Primary Input Selection

Test Points are provided for monitoring buffered and equalised input, and decoding lock



8000/xpt2/3 PJS May 94 V3.01

Serial to Parallel Conversion

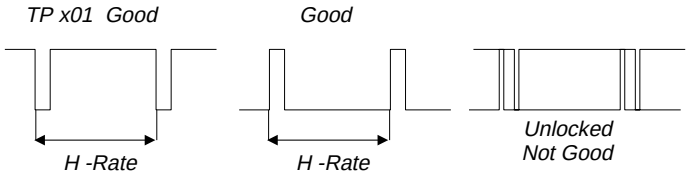


SBX1602A Serial to Parallel Convertor Block Diagram (D1 Mode)

The 270 MHz SDI signal is passed as a surface track signal from the rear connector panel CN-312A (passive) onto the XPT board. The cable limit is upto 200m, according to cable type, but is likely to be much shorter. (If a BKDM-5080 32 x 4 input router is used for DME channels 3 and 4, the signals will be looped via this).

The signal is a.c. coupled by C x11 and 75R terminated by R x14. Q x01 drives the signal into the SBX 1602A. Internally, the signal is equalised and reclocked (using the "analogue" input - the "digital" input bypasses the equalliser, and is for use in short distance "internal" applications) and is then made available as a monitoring point CN x01 - this should be used when checking the existance or validity of an incoming signal - without loading the circuit. In other applications, such as the BKPF-102, this is used as the "Active Through" port.

The SDI format requires a 30 bit buffer in order to recognise the SDI sync word sequence of 3FF 000 000 (10 bit notation) or FF 00 00 (8 bit notaion). This Timing Reference signal (TRS) identifies the H-start of the incoming line, and synchronises the word-relationship of the serial to parallel conversion. Detection of the TRS also causes the Sync Out signal on TP x01, which may be observed on an ordinary oscilloscope - this should show a line-locked signal pulsing low or high but not both. Performance on an extender may be noisier.



The on-board EEPROM holds VCO values for each SBX-1602A. To maintain stability (and lock-in capability after temporary loss of incoming signal) the thermistor located to the rear of the board is sampled regularly (every minute) in order to provide temperature compensation on the XPT-1 and XPT-2 boards. The XPT-3 uses diode compensation.

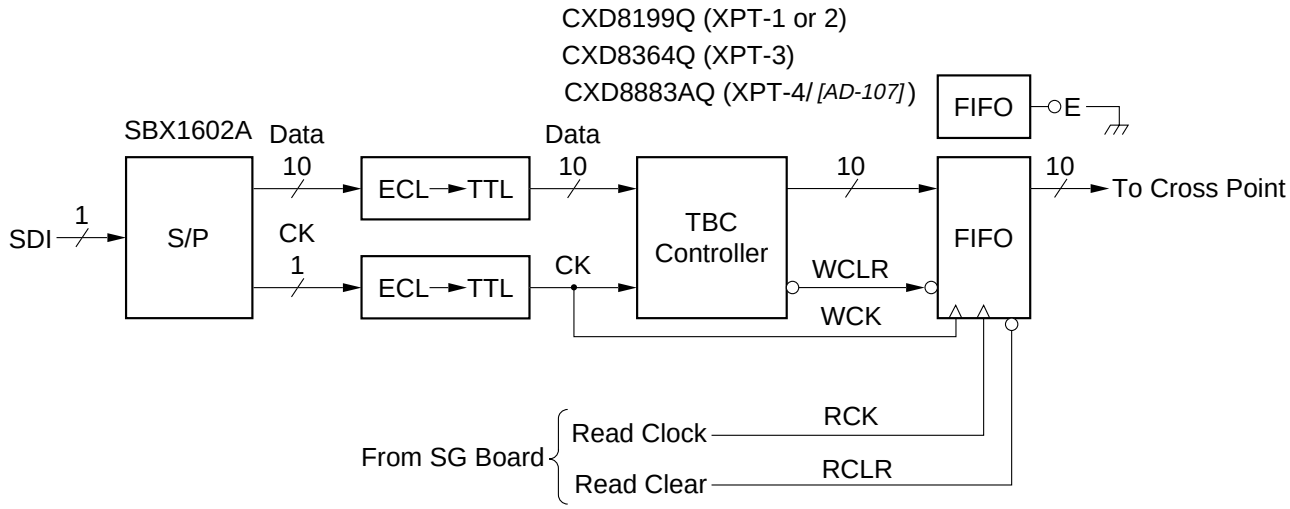
Observed VCO Values for a XPT-3 board:

Location 40...	68	60	76	76	90	6a	7b	70	for D1	
Location 60...	44	3b	50	51	66	4b	56	4c	for D2	(1 step = 0.06MHz)

For a XPT-2 board, only the D1 values are programmed, and similarly on the XPT-1 board for NTSC D2.

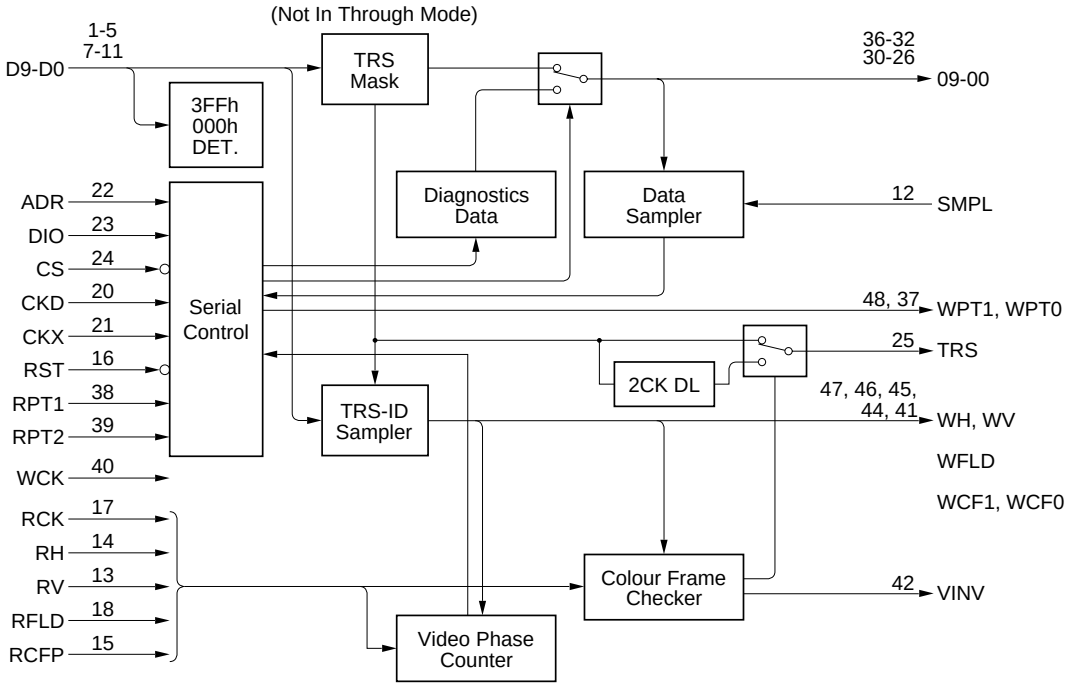
On the production line, adjustment data for boards and modules is written using the rear connector on a DVS-6000(C), but the 8000 requires a special interface card from the parallel link on the front of its Sync Generator card to the PC serial port. This software is not currently available for use outside the factory.

Input TBC



TBC Control FIFO Block Diagram

The CXD 8364Q receives the 10-bit parallel incoming data after ECL to TTL conversion, and identifies the TRS for itself (3FF 000 000). The TRS is then usually masked out, but in "through mode" the signal is passed unaltered.



CXD8364Q Block Diagram

(The CXD 8199Q used on older XPT-2 boards always masked the TRS, prohibiting the use of "through mode") The TRS pulse is sent as "Write Clear" to 2x Hitachi HM63021P-28 Fifo which act in parallel as a 10-bit wide delay line (8+2). (For D2, colour framing detection is required, and a 2 clock *write clear* delay may be added) *Read Clear* for each individual source initiates reading a new line from the FIFO. This is nominally 0.5H behind a correctly timed input. An adjustment of -127 to +128 clock pulses (13.5MHz) may be made to enable horizontal image repositioning in pixel steps, should this be required.

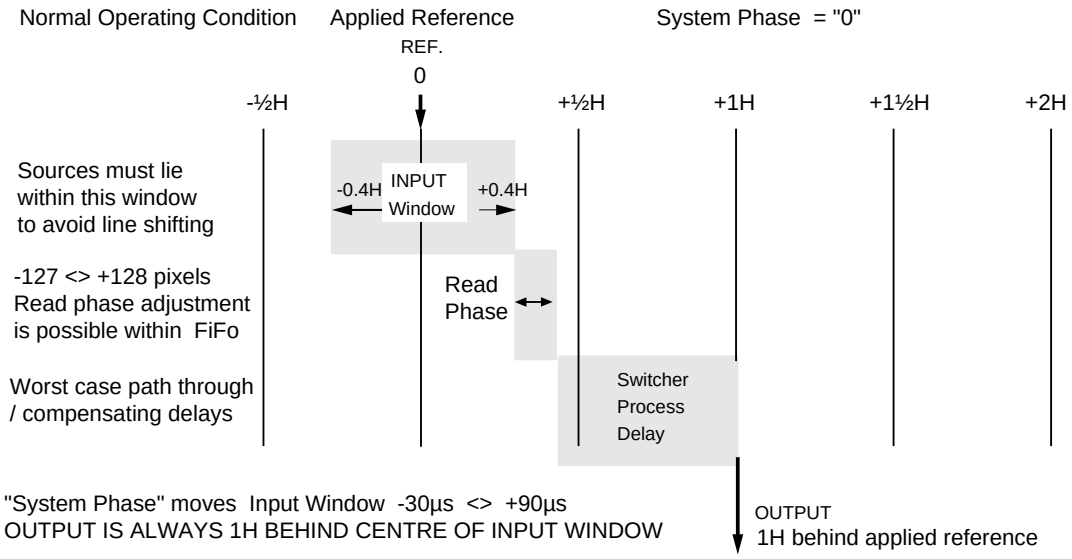
Timing is provided through Programmable Interval Timers (PITs or CTCs) providing H-rate pulse outputs.

The later designs support suppression of the 2 lsbs, which may be desirable where an 8-bit source is used, but the originating equipment has not, itself, set the 2 lsbs to zero.

Overview of System Timing

For the anticipated configuration, the input sources are approximately co-timed with the applied External Reference. The Switcher output will be 1 line later.

DVS System Phase Relation Timing Chart



In this case, sources should all lie within ±0.4H of the reference.

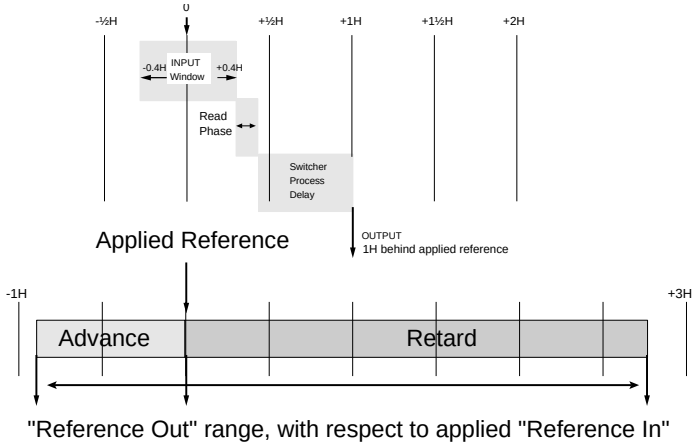
However, the System Timing may be varied, with respect to the *applied reference plus 1 line*, by -30µs to +90µs. In this case, the inputs should all lie within -1.4H to -0.6H of the output System Timing.

(Note that this is displayed as -30µ to =90µs in the Switcher Output Control menu)

Reference Output

If required, there is a Reference Output, which may be used to time sources, and is adjustable from -60µs to +180µs *with respect to the applied external reference*.

The 1H delay of the ouput is after D to A conversion by Edit Preview (or BKPF)- digital outputs are 0.7µs earlier.



"Reference Out" range, with respect to applied "Reference In"

Crosspoint Selection

3 pairs of CXD 8258Q, each an 8 x 8 matrix 5 bits wide, operate in parallel to give an 8 input x 24 output,10 bit routing matrix. These boards are in parallel with the re-entrant MAT card, giving a maximum 32 + 9 sources.

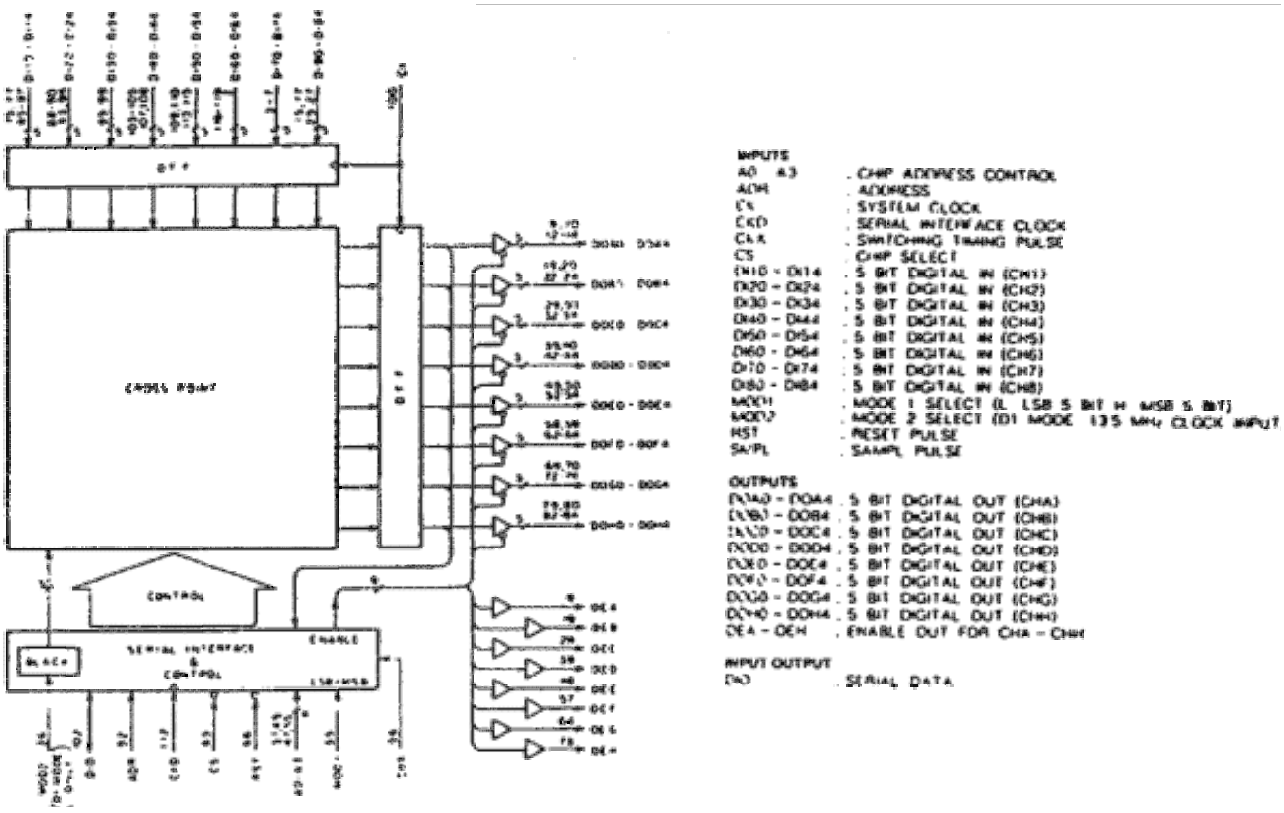
A wired-OR system is used, and output goes high impedance when inactive (tri-state).

Source switching takes place shortly after the rising edge of Vertical Drive VD, using CK X ("Clock eXecute")

The Mode 1 pin has 5v on IC 902/904/906 identifying them as MSB and 0v on IC 903/905/907 as LSB - this is applicable when the internal matte generator is used to output BLACK (+ no chroma), but is currently only used by the similar CXD8300Q on the MAT board.

Where 14-bit signals must be routed, 3 ICs will be used together.

Cross point IC block diagram:



MOTHER BOARD
(1A)

MAT-2

	A	B	C	D
1	+5V	RDATA : L	RDATA : H	-5V
2	+5V	WDATA : L	WDATA : H	-5V
3	+5V	ADD : L	ADD : H	FUSE -
4	+5V	CKD : L	CKD : H	CKX
5	FUSE +	RST	LALT	VD
6	THERMO	SC	HBLK	HZ
7	SLTAD 1	SLTAD 2	SLTAD 3	SLTAD 4
8	SLTAD 0	CF	VBLK	OE
9	GND	GND	GND	CK14 (13.5M)
10	GND	GND	GND	CK8 (27.0M)
11	AUX1 6	AUX1 7	AUX1 8	AUX1 9
12	AUX1 2	AUX1 3	AUX1 4	AUX1 5
13	AUX4 8	AUX4 9	AUX1 0	AUX1 1
14	AUX4 4	AUX4 5	AUX4 6	AUX4 7
15	AUX4 0	AUX4 1	AUX4 2	AUX4 3
16	PVW 6	PVW 7	PVW 8	PVW 9
17	PVW 2	PVW 3	PVW 4	PVW 5
18	AUX2 8	AUX2 9	PVW 0	PVW 1
19	AUX2 4	AUX2 5	AUX2 6	AUX2 7
20	AUX2 0	AUX2 1	AUX2 2	AUX2 3
21	AUX3 6	AUX3 7	AUX3 8	AUX3 9
22	AUX3 2	AUX3 3	AUX3 4	AUX3 5
23	PGM 18	PGM 19	AUX3 0	AUX3 1
24	PGM 14	PGM 15	PGM 16	PGM 17
25	PGM 10	PGM 11	PGM 12	PGM 13
26	PGM 26	PGM 27	PGM 28	PGM 29
27	PGM 22	PGM 23	PGM 24	PGM 25
28	BKGD A D8	BKGD A D9	PGM 20	PGM 21
29	BKGD A D4	BKGD A D5	BKGD A D6	BKGD A D7
30	BKGD A D0	BKGD A D1	BKGD A D2	BKGD A D3
31	GND	GND	BKGD B D8	BKGD B D9
32	GND	GND	BKGD B D6	BKGD B D7

	A	B	C	D
1	BKGD B D2	BKGD B D3	BKGD B D4	BKGD B D5
2	FILL D8	FILL D9	BKGD B D0	BKGD B D1
3	FILL D4	FILL D5	FILL D6	FILL D7
4	FILL D0	FILL D1	FILL D2	FILL D3
5	KYSR 2 16	KYSR 2 17	KYSR 2 18	KYSR 2 19
6	KYSR 2 12	KYSR 2 13	KYSR 2 14	KYSR 2 15
7	KYSR 1 18	KYSR 1 19	KYSR 2 10	KYSR 2 11
8	KYSR 1 14	KYSR 1 15	KYSR 1 16	KYSR 1 17
9	KYSR 1 10	KYSR 1 11	KYSR 1 12	KYSR 1 13
10	KYSR D6	KYSR D7	KYSR D8	KYSR D9
11	KYSR D2	KYSR D3	KYSR D4	KYSR D5
12	KYSR 2 28	KYSR 2 29	KYSR D0	KYSR D1
13	KYSR 2 24	KYSR 2 25	KYSR 2 26	KYSR 2 27
14	KYSR 2 20	KYSR 2 21	KYSR 2 22	KYSR 2 23
15	KYSR 1 26	KYSR 1 27	KYSR 1 28	KYSR 1 29
16	KYSR 1 22	KYSR 1 23	KYSR 1 24	KYSR 1 25
17	BKGD A 28	BKGD A 29	KYSR 1 20	KYSR 1 21
18	BKGD A 24	BKGD A 25	BKGD A 26	BKGD A 27
19	BKGD A 20	BKGD A 21	BKGD A 22	BKGD A 23
20	BKGD D 26	DKGD D 27	BKGD B 28	BKGD B 29
21	BKGD B 22	BKGD B 23	BKGD B 24	BKGD B 25
22	FILL 2 28	FILL 2 29	BKGD B 20	BKGD B 21
23	FILL 2 24	FILL 2 25	FILL 2 26	FILL 2 27
24	FILL 2 20	FILL 2 21	FILL 2 22	FILL 2 23
25	FILL 1 26	FILL 1 27	FILL 1 28	FILL 1 29
26	FILL 1 22	FILL 1 23	FILL 1 24	FILL 1 25
27	BKGD A 18	BKGD A 19	FILL 1 20	FILL 1 21
28	BKGD A 14	BKGD A 15	BKGD A 16	BKGD A 17
29	BKGD A 10	BKGD A 11	BKGD A 12	BKGD A 13
30	BKGD B 16	BKGD B 17	BKGD B 18	BKGD B 19
31	GND	GND	BKGD B 14	BKGD B 15
32	GND	GND	BKGD B 12	BKGD B 13

	A	B	C
1	GND	GND	GND
2	FILL 2 19	BKGD B 10	BKGD B 11
3	FILL 2 16	FILL 2 17	FILL 2 18
4	FILL 2 13	FILL 2 14	FILL 2 15
5	FILL 2 10	FILL 2 11	FILL 2 12
6	FILL 1 17	FILL 1 18	FILL 1 19
7	FILL 1 14	FILL 1 15	FILL 1 16
8	FILL 1 11	FILL 1 12	FILL 1 13
9	MASK 38	MASK 39	FILL 1 10
10	MASK 35	MASK 36	MASK 37
11	MASK 32	MASK 33	MASK 34
12	MASK 29	MASK 30	MASK 31
13	MASK 26	MASK 27	MASK 28
14	MASK 23	MASK 24	MASK 25
15	MASK 20	MASK 21	MASK 22
16	MASK 17	MASK 18	MASK 19
17	MASK 14	MASK 15	MASK 16
18	MASK 11	MASK 12	MASK 13
19	CKFL 18	CKFL 19	MASK 10
20	CKFL 15	CKFL 16	CKFL 17
21	CKFL 12	CKFL 13	CKFL 14
22	CKFL 29	CKFL 10	CKFL 11
23	CKFL 26	CKFL 27	CKFL 28
24	CKFL 23	CKFL 24	CKFL 25
25	CKFL 20	CKFL 21	CKFL 22
26	MY 17	MY 18	MY 19
27	MY 14	MY 15	MY 16
28	MY 11	MY 12	MY 13
29	MY 28	MY 29	MY 10
30	MY 25	MY 26	MY 27
31	MY 22	MY 23	MY 24
32	GND	MY 20	MY 21

13
MATTE

(1E)

XPT-2

	A	B	C	D
1	+5V	RDATA : L	RDATA : H	-5V
2	+5V	WDATA : L	WDATA : H	-5V
3	+5V	ADD : L	ADD : H	FUSE -
4	+5V	CKD : L	CKD : H	CKX
5	FUSE +	RST	LALT	VD
6	THERMO	SC	HBLK	HZ
7	SLTAD 1	SLTAD 2	SLTAD 3	SLTAD 4
8	SLTAD 0	CF	VBLK	OE
9	GND	GND	GND	CK16 (13.5M)
10	GND	GND	GND	CK8 (27.0M)
11	AUX1 6	AUX1 7	AUX1 8	AUX1 9
12	AUX1 2	AUX1 3	AUX1 4	AUX1 5
13	AUX4 8	AUX4 9	AUX1 0	AUX1 1
14	AUX4 4	AUX4 5	AUX4 6	AUX4 7
15	AUX4 0	AUX4 1	AUX4 2	AUX4 3
16	PVW 6	PVW 7	PVW 8	PVW 9
17	PVW 2	PVW 3	PVW 4	PVW 5
18	AUX2 8	AUX2 9	PVW 0	PVW 1
19	AUX2 4	AUX2 5	AUX2 6	AUX2 7
20	AUX2 0	AUX2 1	AUX2 2	AUX2 3
21	AUX3 6	AUX3 7	AUX3 8	AUX3 9
22	AUX3 2	AUX3 3	AUX3 4	AUX3 5
23	BKGD A D8	BKGD A D9	AUX3 0	AUX3 1
24	BKGD A D4	BKGD A D5	BKGD A D6	BKGD A D7
25	BKGD A D0	BKGD A D1	BKGD A D2	BKGD A D3
26	BKGD B D6	BKGD B D7	BKGD B D8	BKGD B D9
27	BKGD B D2	BKGD B D3	BKGD B D4	BKGD B D5
28	FILL D8	FILL D9	BKGD B D0	BKGD B D1
29	FILL D4	FILL D5	FILL D6	FILL D7
30	FILL D0	FILL D1	FILL D2	FILL D3
31	GND	GND	KYSR 2 18	KYSR 2 19
32	GND	GND	KYSR 2 16	KYSR 2 17

	A	B	C	D
1	KYSR 2 12	KYSR 2 13	KYSR 2 14	KYSR 2 15
2	KYSR 1 18	KYSR 1 19	KYSR 2 10	KYSR 2 11
3	KYSR 1 14	KYSR 1 15	KYSR 1 16	KYSR 1 17
4	KYSR 1 10	KYSR 1 11	KYSR 1 12	KYSR 1 13
5	KYSR D6	KYSR D7	KYSR D8	KYSR D9
6	KYSR D2	KYSR D3	KYSR D4	KYSR D5
7	KYSR 2 28	KYSR 2 29	KYSR D0	KYSR D1
8	KYSR 2 24	KYSR 2 25	KYSR 2 26	KYSR 2 27
9	KYSR 2 20	KYSR 2 21	KYSR 2 22	KYSR 2 23
10	KYSR 1 26	KYSR 1 27	KYSR 1 28	KYSR 1 29
11	KYSR 1 22	KYSR 1 23	KYSR 1 24	KYSR 1 25
12	BKGD A 28	BKGD A 29	KYSR 1 20	KYSR 1 21
13	BKGD A 24	BKGD A 25	BKGD A 26	BKGD A 27
14	BKGD A 20	BKGD A 21	BKGD A 22	BKGD A 23
15	BKGD B 26	BKGD B 27	BKGD B 28	BKGD B 29
16	BKGD B 22	BKGD B 23	BKGD B 24	BKGD B 25
17	FILL 2 28	FILL 2 29	BKGD B 20	BKGD B 21
18	FILL 2 24	FILL 2 25	FILL 2 26	FILL 2 27
19	FILL 2 20	FILL 2 21	FILL 2 22	FILL 2 23
20	FILL 1 26	FILL 1 27	FILL 1 28	FILL 1 29
21	FILL 1 22	FILL 1 23	FILL 1 24	FILL 1 25
22	BKGD A 18	BKGD A 19	FILL 1 20	FILL 1 21
23	BKGD A 14	BKGD A 15	BKGD A 16	BKGD A 17
24	BKGD A 10	BKGD A 11	BKGD A 12	BKGD A 13
25	BKGD B 16	BKGD B 17	BKGD B 18	BKGD B 19
26	BKGD B 12	BKGD B 13	BKGD B 14	BKGD B 15
27	FILL 2 18	FILL 2 19	BKGD B 10	BKGD B 11
28	FILL 2 14	FILL 2 15	FILL 2 16	FILL 2 17
29	FILL 2 10	FILL 2 11	FILL 2 12	FILL 2 13
30	FILL 1 16	FILL 1 17	FILL 1 18	FILL 1 19
31	GND	GND	FILL 1 14	FILL 1 15
32	GND	GND	FILL 1 12	FILL 1 13

	A	B	C
1	GND	GND	GND
2	MASK 39	FILL 1 10	FILL 1 11
3	MASK 36	MASK 37	MASK 38
4	MASK 33	MASK 34	MASK 35
5	MASK 30	MASK 31	MASK 32
6	MASK 27	MASK 28	MASK 29
7	MASK 24	MASK 25	MASK 26
8	MASK 21	MASK 22	MASK 23
9	MASK 18	MASK 19	MASK 20
10	MASK 15	MASK 16	MASK 17
11	MASK 12	MASK 13	MASK 14
12	GND	MASK 10	MASK 11
13	GND	GND	GND
14	GND	GND	GND
15	GND	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	GND	INPUT 38	GND
19	GND	GND	GND
20	GND	INPUT 37	GND
21	GND	GND	GND
22	GND	INPUT 36	GND
23	GND	GND	GND
24	GND	INPUT 35	GND
25	GND	GND	GND
26	GND	INPUT 34	GND
27	GND	GND	GND
28	GND	INPUT 33	GND
29	GND	GND	GND
30	GND	INPUT 32	GND
31	GND	GND	GND
32	GND	INPUT 31	GND

17
PRI INPUT 3

Re-entrant Xpts

MAT-4

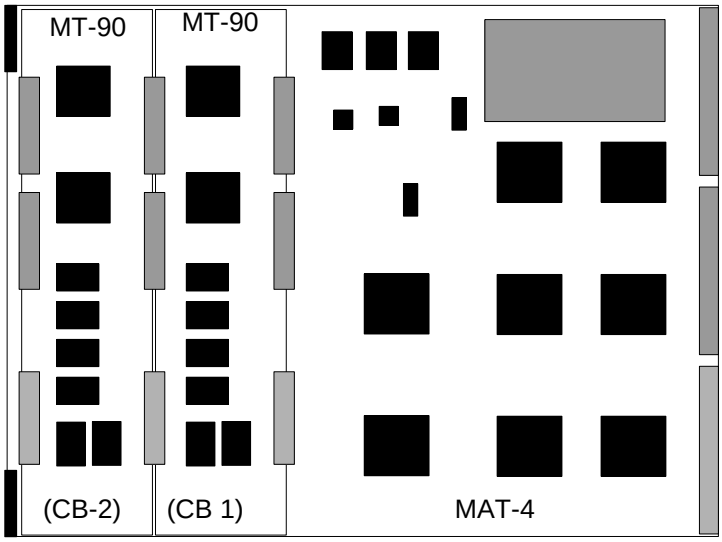
Blended Background Colour Option
MT-90

PDF Edition

MAT-4 Board and MT-90 Options (BKDS-6072)

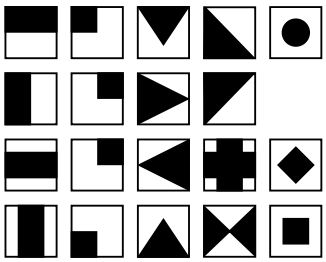
The Mat-4 board provides two basic functions:

Internal generation of two colour background sources and black
Crosspoint selection for on-board colour backgrounds, and black
Crosspoint selection for re-entrant sources:
Chromakey Fill 1,2, Memory 1,2 and ME1 and ME 2 Pgm outputs



MT-90 Options

Each option board can blend *a* colour background using basic wipe solids.



The Basic Wipes with MT-90

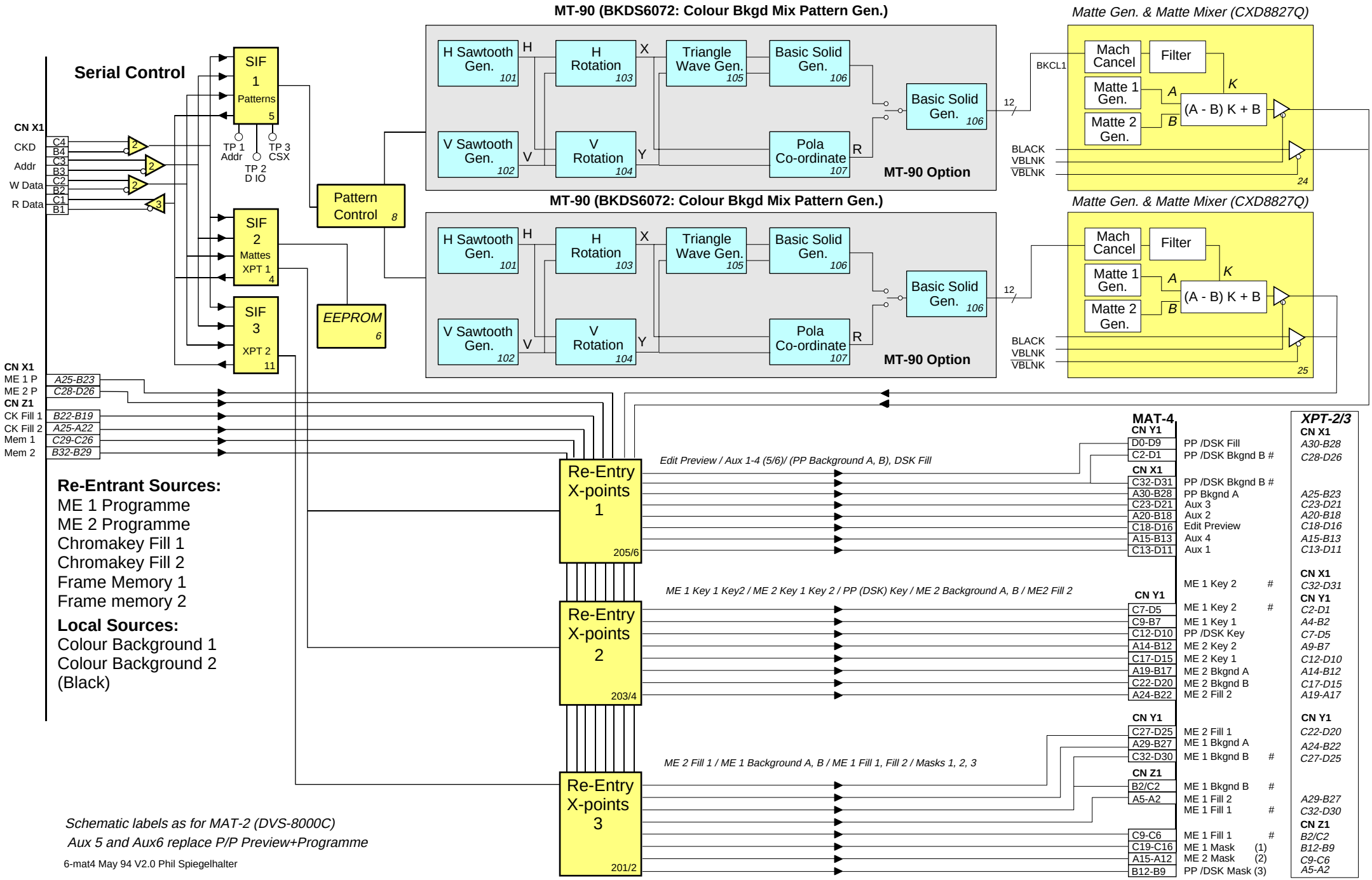
Additional functions include Pattern mix and modification
The method is similar to the basic wipes on WKG-10, without modulation or rotation

Control

IC 4 Serial Interface controls matte generator ICs 24 and 25 crosspoint ICs 203/4 205/6
IC 11 controls crosspoint ICs 201/2 and EEPROM IC6 (MAT-4)
IC 5 controls the optional MT-90 boards
IC 8, controlled from IC 5, generates the control signals for pattern selection etc
IC 7 is concerned with timing pulses

Training and Engineering Information Department

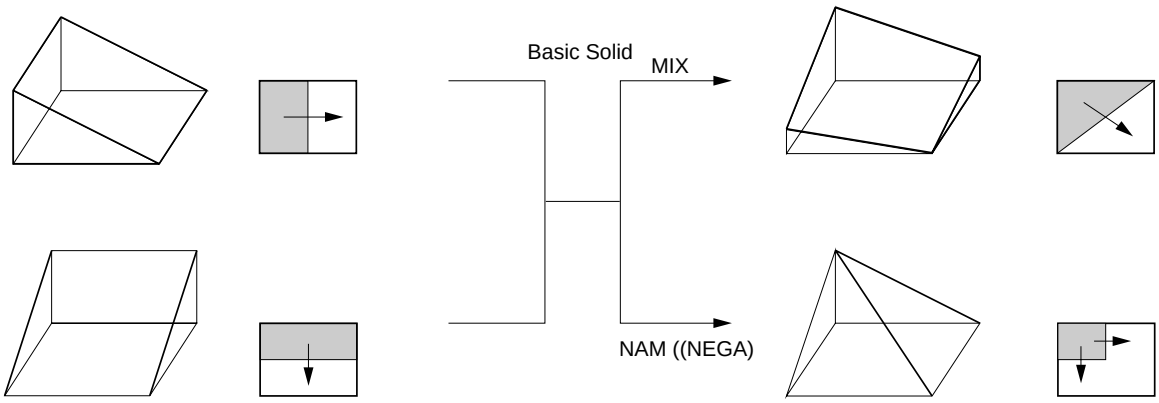
Colour Background and Re-entry MAT-4 and MT-90 / MT-90 Blend Options



Schematic labels as for MAT-2 (DVS-8000C)

Aux 5 and Aux6 replace P/P Preview+Programme

Wipe Solid Generation



Wipe Solids

Digital ramp generators at horizontal (101) and vertical (102) rate generate the basic form.

Modifiers are Multi (multiple restarts of the H or V count) and Angle / Speed (rotation).

H and V rotation (103+104) allows modification of the angle by controlling a mix of the H and V data.

The triangle wave generator allows for symmetrical patterns by "reflecting" the count at a desired point (around zero).

The wipe solid geometric model is created by combining the resulting X and Y signals by simple addition (mixing) or passing the greater signal (NAM)

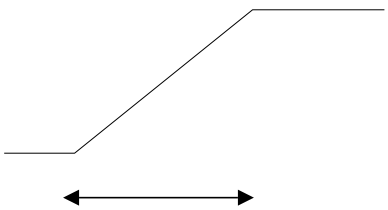
Polar wipes interprete the values as radius and angle

The final wipe shape seen on screen is formed by a plane (value) intersecting the solid.

The Key Generator (108) controls Clip and Gain of the wipe signal and then Mach processing inside the *Super Video Modifier* produces a smoothed transition instead of harsh clipped start/stop.

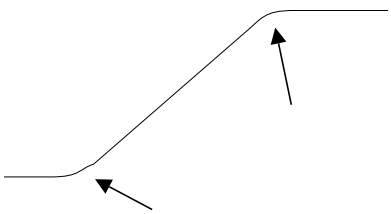
This is to remove the "edge enhancement" effect of the eye, and is achieved rom coding (as MAT-2) or ¼ ½ ¼ (video based) averaging of adjacent key samples.

Wipe Transition



(Area of Softness)

Mach Cancellation



(By Rom on MAT-2)

Internal matte generators produce Y and C channels which are independantly mixed by the wipe blend signal. For D-1 the output data is multiplexed.

In the absence of a MT-90 wipe signal, only Matte 1 is active for each colour background, and is applied uniformly across the whole screen.

Crosspoint Selection

CXD 8300Q Crosspoint ICs selects:-

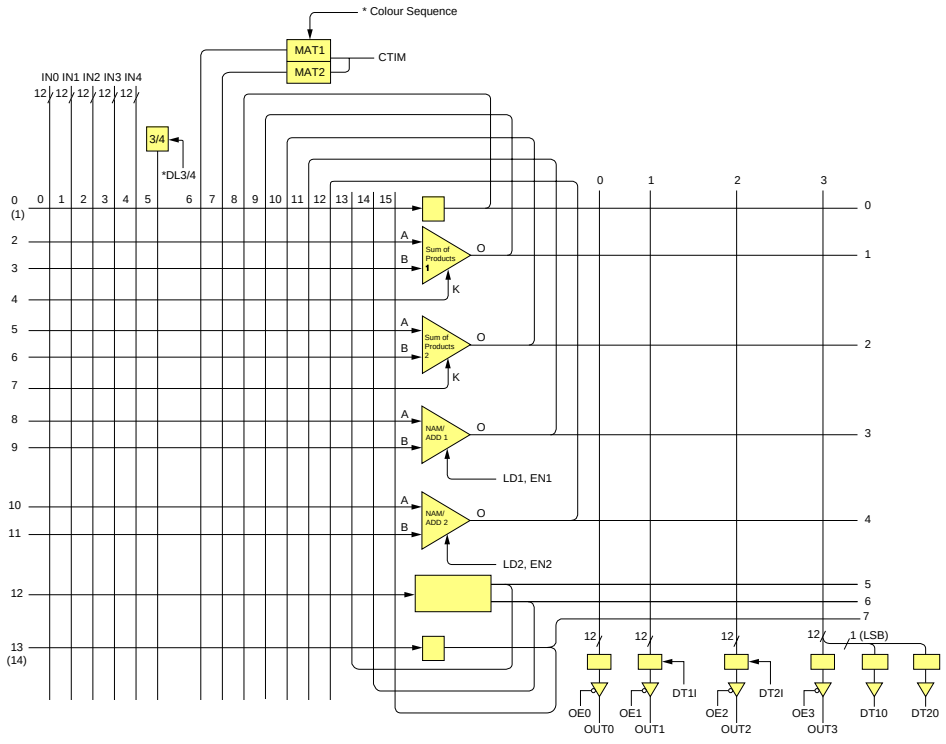
Colour Background 1, Colour background 2 and Black from this board

re-entrant Mix Effects Programme 1, and Mix Effects Programme 2, from their respective MIX-8A boards

re-entrant Chromakey Fill 1 and Chromakey Fill 2
(processed foregrounds from the BKDS-8031 board) CRK-4

re-entrant Frame Memory Channel 1 and Frame Memory Channel 2
(either "MEM IN" or "MEM OUT") as required from the BKDS-8050 FMY-51

CXD8827Q Super Video Modifier used on MAT-4



6-31cx8827 Kim/Phil Spiegelhalter June 94 V0.1

MOTHER BOARD
(1A)

MAT-2

	A	B	C	D
1	+5V	RDATA : L	RDATA : H	-5V
2	+5V	WDATA : L	WDATA : H	-5V
3	+5V	ADD : L	ADD : H	FUSE -
4	+5V	CKD : L	CKD : H	CKX
5	FUSE +	RST	LALT	VD
6	THERMO	SC	HBLK	HZ
7	SLTAD 1	SLTAD 2	SLTAD 3	SLTAD 4
8	SLTAD 0	CF	VBLK	OE
9	GND	GND	GND	CK14 (13.5M)
10	GND	GND	GND	CK8 (27.0M)
11	AUX1 6	AUX1 7	AUX1 8	AUX1 9
12	AUX1 2	AUX1 3	AUX1 4	AUX1 5
13	AUX4 8	AUX4 9	AUX1 0	AUX1 1
14	AUX4 4	AUX4 5	AUX4 6	AUX4 7
15	AUX4 0	AUX4 1	AUX4 2	AUX4 3
16	PVW 6	PVW 7	PVW 8	PVW 9
17	PVW 2	PVW 3	PVW 4	PVW 5
18	AUX2 8	AUX2 9	PVW 0	PVW 1
19	AUX2 4	AUX2 5	AUX2 6	AUX2 7
20	AUX2 0	AUX2 1	AUX2 2	AUX2 3
21	AUX3 6	AUX3 7	AUX3 8	AUX3 9
22	AUX3 2	AUX3 3	AUX3 4	AUX3 5
23	PGM 18	PGM 19	AUX3 0	AUX3 1
24	PGM 14	PGM 15	PGM 16	PGM 17
25	PGM 10	PGM 11	PGM 12	PGM 13
26	PGM 26	PGM 27	PGM 28	PGM 29
27	PGM 22	PGM 23	PGM 24	PGM 25
28	BKGD A D8	BKGD A D9	PGM 20	PGM 21
29	BKGD A D4	BKGD A D5	BKGD A D6	BKGD A D7
30	BKGD A D0	BKGD A D1	BKGD A D2	BKGD A D3
31	GND	GND	BKGD B D8	BKGD B D9
32	GND	GND	BKGD B D6	BKGD B D7

	A	B	C	D
1	BKGD B D2	BKGD B D3	BKGD B D4	BKGD B D5
2	FILL D8	FILL D9	BKGD B D0	BKGD B D1
3	FILL D4	FILL D5	FILL D6	FILL D7
4	FILL D0	FILL D1	FILL D2	FILL D3
5	KYSR 2 16	KYSR 2 17	KYSR 2 18	KYSR 2 19
6	KYSR 2 12	KYSR 2 13	KYSR 2 14	KYSR 2 15
7	KYSR 1 18	KYSR 1 19	KYSR 2 10	KYSR 2 11
8	KYSR 1 14	KYSR 1 15	KYSR 1 16	KYSR 1 17
9	KYSR 1 10	KYSR 1 11	KYSR 1 12	KYSR 1 13
10	KYSR D6	KYSR D7	KYSR D8	KYSR D9
11	KYSR D2	KYSR D3	KYSR D4	KYSR D5
12	KYSR 2 28	KYSR 2 29	KYSR D0	KYSR D1
13	KYSR 2 24	KYSR 2 25	KYSR 2 26	KYSR 2 27
14	KYSR 2 20	KYSR 2 21	KYSR 2 22	KYSR 2 23
15	KYSR 1 26	KYSR 1 27	KYSR 1 28	KYSR 1 29
16	KYSR 1 22	KYSR 1 23	KYSR 1 24	KYSR 1 25
17	BKGD A 28	BKGD A 29	KYSR 1 20	KYSR 1 21
18	BKGD A 24	BKGD A 25	BKGD A 26	BKGD A 27
19	BKGD A 20	BKGD A 21	BKGD A 22	BKGD A 23
20	BKGD D 26	DKGD D 27	BKGD B 28	BKGD B 29
21	BKGD B 22	BKGD B 23	BKGD B 24	BKGD B 25
22	FILL 2 28	FILL 2 29	BKGD B 20	BKGD B 21
23	FILL 2 24	FILL 2 25	FILL 2 26	FILL 2 27
24	FILL 2 20	FILL 2 21	FILL 2 22	FILL 2 23
25	FILL 1 26	FILL 1 27	FILL 1 28	FILL 1 29
26	FILL 1 22	FILL 1 23	FILL 1 24	FILL 1 25
27	BKGD A 18	BKGD A 19	FILL 1 20	FILL 1 21
28	BKGD A 14	BKGD A 15	BKGD A 16	BKGD A 17
29	BKGD A 10	BKGD A 11	BKGD A 12	BKGD A 13
30	BKGD B 16	BKGD B 17	BKGD B 18	BKGD B 19
31	GND	GND	BKGD B 14	BKGD B 15
32	GND	GND	BKGD B 12	BKGD B 13

	A	B	C
1	GND	GND	GND
2	FILL 2 19	BKGD B 10	BKGD B 11
3	FILL 2 16	FILL 2 17	FILL 2 18
4	FILL 2 13	FILL 2 14	FILL 2 15
5	FILL 2 10	FILL 2 11	FILL 2 12
6	FILL 1 17	FILL 1 18	FILL 1 19
7	FILL 1 14	FILL 1 15	FILL 1 16
8	FILL 1 11	FILL 1 12	FILL 1 13
9	MASK 38	MASK 39	FILL 1 10
10	MASK 35	MASK 36	MASK 37
11	MASK 32	MASK 33	MASK 34
12	MASK 29	MASK 30	MASK 31
13	MASK 26	MASK 27	MASK 28
14	MASK 23	MASK 24	MASK 25
15	MASK 20	MASK 21	MASK 22
16	MASK 17	MASK 18	MASK 19
17	MASK 14	MASK 15	MASK 16
18	MASK 11	MASK 12	MASK 13
19	CKFL 18	CKFL 19	MASK 10
20	CKFL 15	CKFL 16	CKFL 17
21	CKFL 12	CKFL 13	CKFL 14
22	CKFL 29	CKFL 10	CKFL 11
23	CKFL 26	CKFL 27	CKFL 28
24	CKFL 23	CKFL 24	CKFL 25
25	CKFL 20	CKFL 21	CKFL 22
26	MY 17	MY 18	MY 19
27	MY 14	MY 15	MY 16
28	MY 11	MY 12	MY 13
29	MY 28	MY 29	MY 10
30	MY 25	MY 26	MY 27
31	MY 22	MY 23	MY 24
32	GND	MY 20	MY 21

13
MATTE

(1E)

XPT-2

	A	B	C	D
1	+5V	RDATA : L	RDATA : H	-5V
2	+5V	WDATA : L	WDATA : H	-5V
3	+5V	ADD : L	ADD : H	FUSE -
4	+5V	CKD : L	CKD : H	CKX
5	FUSE +	RST	LALT	VD
6	THERMO	SC	HBLK	HZ
7	SLTAD 1	SLTAD 2	SLTAD 3	SLTAD 4
8	SLTAD 0	CF	VBLK	OE
9	GND	GND	GND	CK16 (13.5M)
10	GND	GND	GND	CK8 (27.0M)
11	AUX1 6	AUX1 7	AUX1 8	AUX1 9
12	AUX1 2	AUX1 3	AUX1 4	AUX1 5
13	AUX4 8	AUX4 9	AUX1 0	AUX1 1
14	AUX4 4	AUX4 5	AUX4 6	AUX4 7
15	AUX4 0	AUX4 1	AUX4 2	AUX4 3
16	PVW 6	PVW 7	PVW 8	PVW 9
17	PVW 2	PVW 3	PVW 4	PVW 5
18	AUX2 8	AUX2 9	PVW 0	PVW 1
19	AUX2 4	AUX2 5	AUX2 6	AUX2 7
20	AUX2 0	AUX2 1	AUX2 2	AUX2 3
21	AUX3 6	AUX3 7	AUX3 8	AUX3 9
22	AUX3 2	AUX3 3	AUX3 4	AUX3 5
23	BKGD A D8	BKGD A D9	AUX3 0	AUX3 1
24	BKGD A D4	BKGD A D5	BKGD A D6	BKGD A D7
25	BKGD A D0	BKGD A D1	BKGD A D2	BKGD A D3
26	BKGD B D6	BKGD B D7	BKGD B D8	BKGD B D9
27	BKGD B D2	BKGD B D3	BKGD B D4	BKGD B D5
28	FILL D8	FILL D9	BKGD B D0	BKGD B D1
29	FILL D4	FILL D5	FILL D6	FILL D7
30	FILL D0	FILL D1	FILL D2	FILL D3
31	GND	GND	KYSR 2 18	KYSR 2 19
32	GND	GND	KYSR 2 16	KYSR 2 17

	A	B	C	D
1	KYSR 2 12	KYSR 2 13	KYSR 2 14	KYSR 2 15
2	KYSR 1 18	KYSR 1 19	KYSR 2 10	KYSR 2 11
3	KYSR 1 14	KYSR 1 15	KYSR 1 16	KYSR 1 17
4	KYSR 1 10	KYSR 1 11	KYSR 1 12	KYSR 1 13
5	KYSR D6	KYSR D7	KYSR D8	KYSR D9
6	KYSR D2	KYSR D3	KYSR D4	KYSR D5
7	KYSR 2 28	KYSR 2 29	KYSR D0	KYSR D1
8	KYSR 2 24	KYSR 2 25	KYSR 2 26	KYSR 2 27
9	KYSR 2 20	KYSR 2 21	KYSR 2 22	KYSR 2 23
10	KYSR 1 26	KYSR 1 27	KYSR 1 28	KYSR 1 29
11	KYSR 1 22	KYSR 1 23	KYSR 1 24	KYSR 1 25
12	BKGD A 28	BKGD A 29	KYSR 1 20	KYSR 1 21
13	BKGD A 24	BKGD A 25	BKGD A 26	BKGD A 27
14	BKGD A 20	BKGD A 21	BKGD A 22	BKGD A 23
15	BKGD B 26	BKGD B 27	BKGD B 28	BKGD B 29
16	BKGD B 22	BKGD B 23	BKGD B 24	BKGD B 25
17	FILL 2 28	FILL 2 29	BKGD B 20	BKGD B 21
18	FILL 2 24	FILL 2 25	FILL 2 26	FILL 2 27
19	FILL 2 20	FILL 2 21	FILL 2 22	FILL 2 23
20	FILL 1 26	FILL 1 27	FILL 1 28	FILL 1 29
21	FILL 1 22	FILL 1 23	FILL 1 24	FILL 1 25
22	BKGD A 18	BKGD A 19	FILL 1 20	FILL 1 21
23	BKGD A 14	BKGD A 15	BKGD A 16	BKGD A 17
24	BKGD A 10	BKGD A 11	BKGD A 12	BKGD A 13
25	BKGD B 16	BKGD B 17	BKGD B 18	BKGD B 19
26	BKGD B 12	BKGD B 13	BKGD B 14	BKGD B 15
27	FILL 2 18	FILL 2 19	BKGD B 10	BKGD B 11
28	FILL 2 14	FILL 2 15	FILL 2 16	FILL 2 17
29	FILL 2 10	FILL 2 11	FILL 2 12	FILL 2 13
30	FILL 1 16	FILL 1 17	FILL 1 18	FILL 1 19
31	GND	GND	FILL 1 14	FILL 1 15
32	GND	GND	FILL 1 12	FILL 1 13

	A	B	C
1	GND	GND	GND
2	MASK 39	FILL 1 10	FILL 1 11
3	MASK 36	MASK 37	MASK 38
4	MASK 33	MASK 34	MASK 35
5	MASK 30	MASK 31	MASK 32
6	MASK 27	MASK 28	MASK 29
7	MASK 24	MASK 25	MASK 26
8	MASK 21	MASK 22	MASK 23
9	MASK 18	MASK 19	MASK 20
10	MASK 15	MASK 16	MASK 17
11	MASK 12	MASK 13	MASK 14
12	GND	MASK 10	MASK 11
13	GND	GND	GND
14	GND	GND	GND
15	GND	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	GND	INPUT 38	GND
19	GND	GND	GND
20	GND	INPUT 37	GND
21	GND	GND	GND
22	GND	INPUT 36	GND
23	GND	GND	GND
24	GND	INPUT 35	GND
25	GND	GND	GND
26	GND	INPUT 34	GND
27	GND	GND	GND
28	GND	INPUT 33	GND
29	GND	GND	GND
30	GND	INPUT 32	GND
31	GND	GND	GND
32	GND	INPUT 31	GND

17
PRI INPUT 3

Wipe Generator

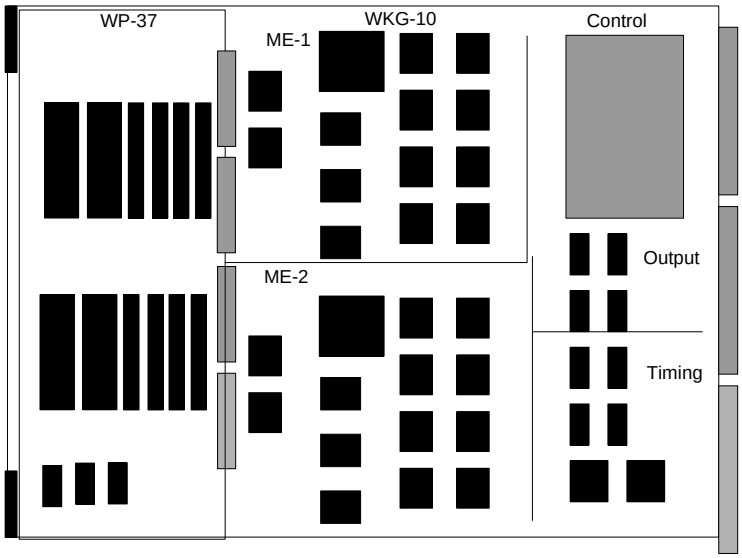
WKG-10

Wipe Solids

WKG-10 Wipe Solids
Wipe Generator

PDF Edition

WKG-10 and WP-37 Enhanced Wipe Generator Option BKDS-6070

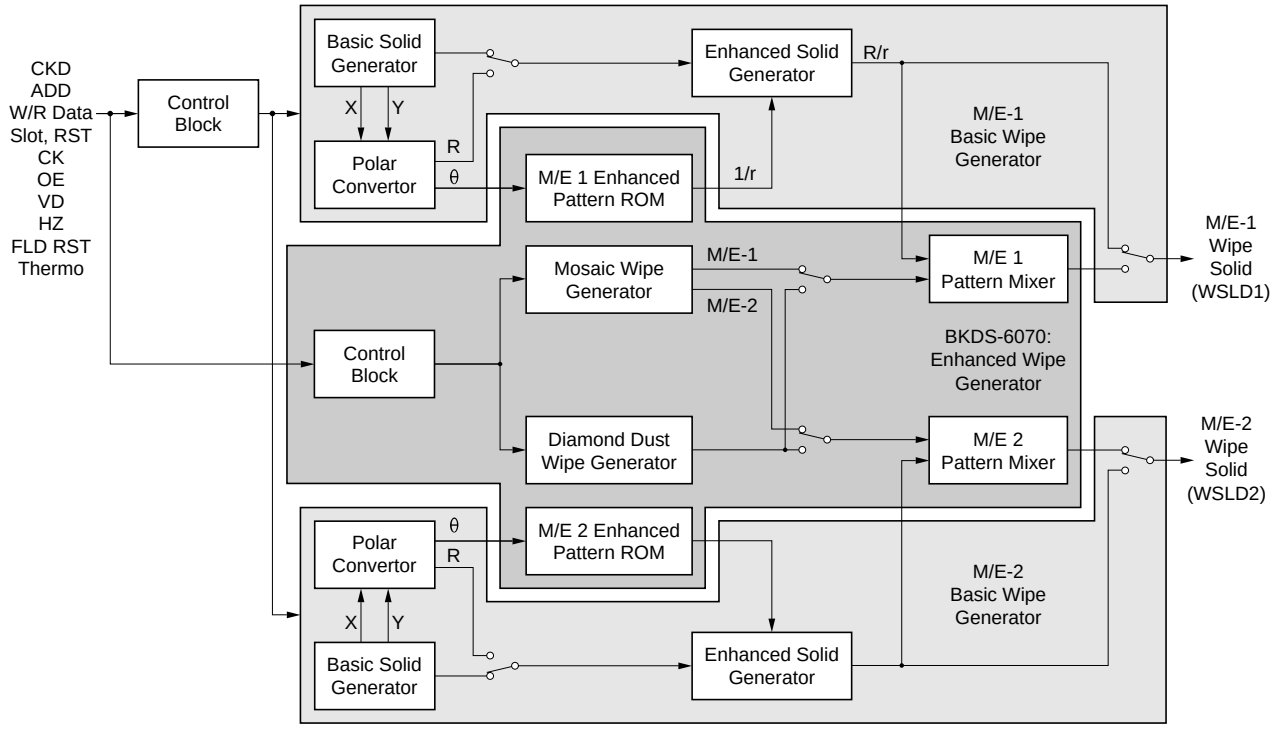


WKG-10

Direct Access digital wipe pattern generation

WP-37 Option

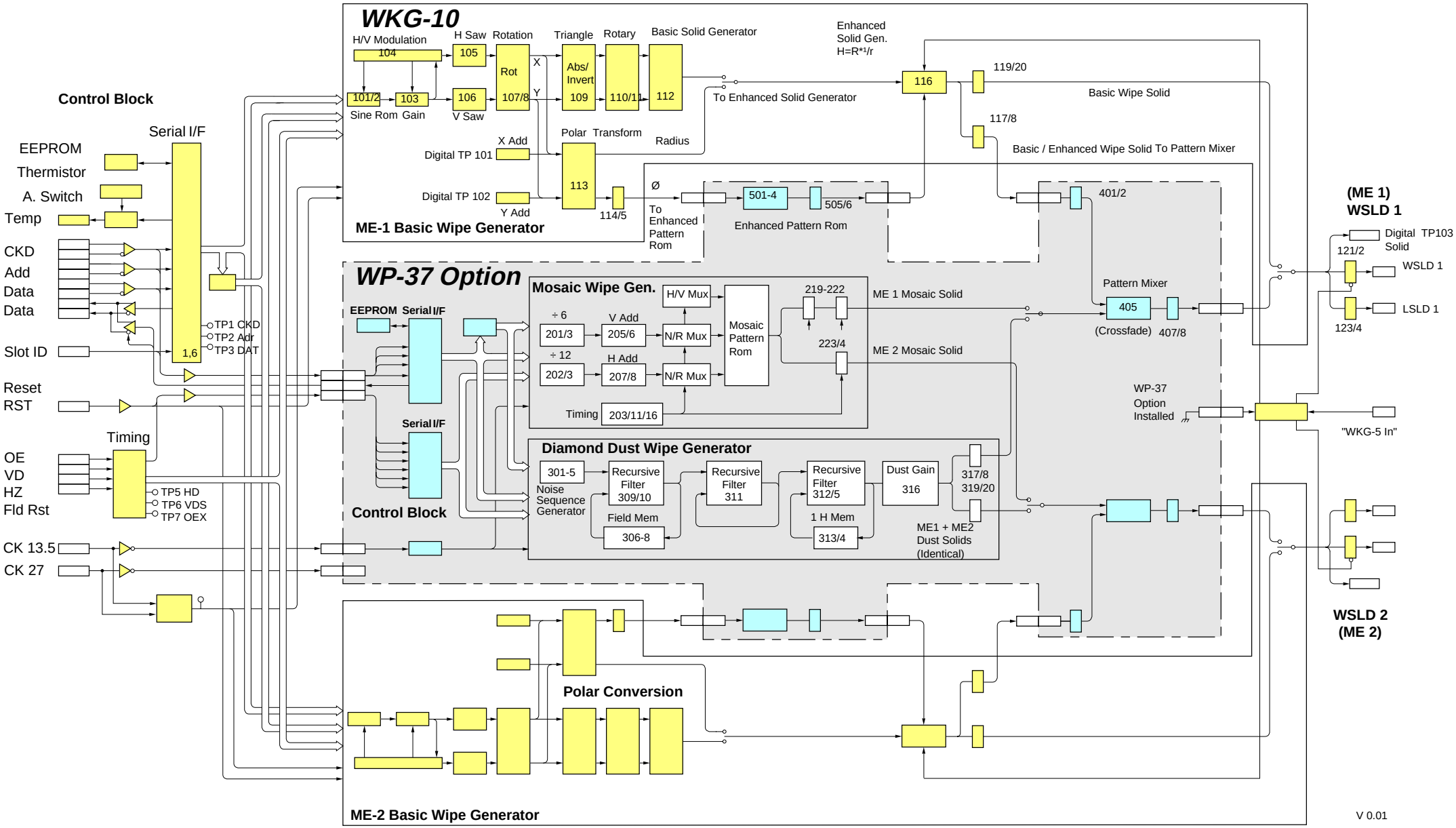
Mosaic and Diamond Dust generators,
Heart and Star wipes
Pattern mixing



Kim/ Phil Spiegelhalter May 94 6-32Wkg10W

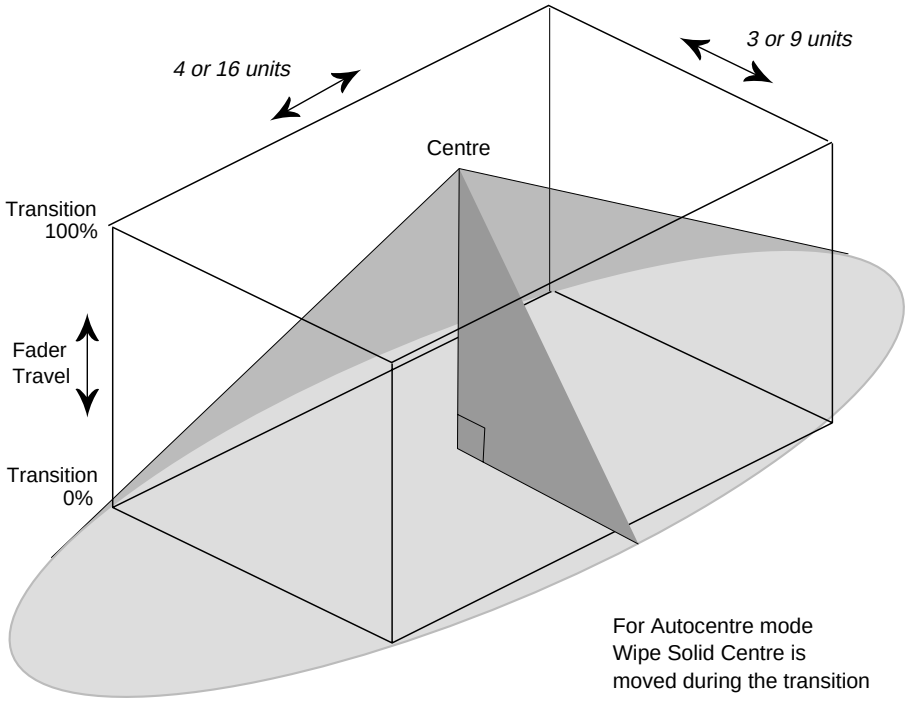
High speed roms hold the reciprocal form of the wipe shape to 14 bits

DVS-6000C WKG-10 Basic Wipe Generator and WP-37 Enhanced Wipe Option



V 0.01

Wipe Solids



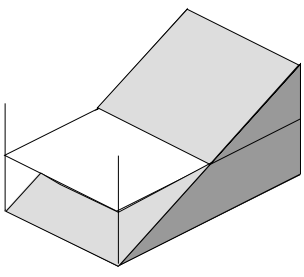
WSLD = "Wipe Solid"

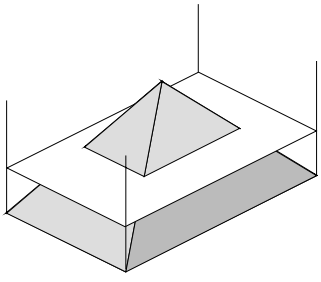
The geomtric solid shape or object, which represents in 3-D, the wipe transition.

Eg: Box Wipe = Rectangular-Based Pyramid
Circle Wipe = Cone
Horizontal Wipe = a Wedge

At any point during a transition, the displayed result is given by the intersection of the "Screen Plane", with the Wipe Solid such as the cone illustrated above.

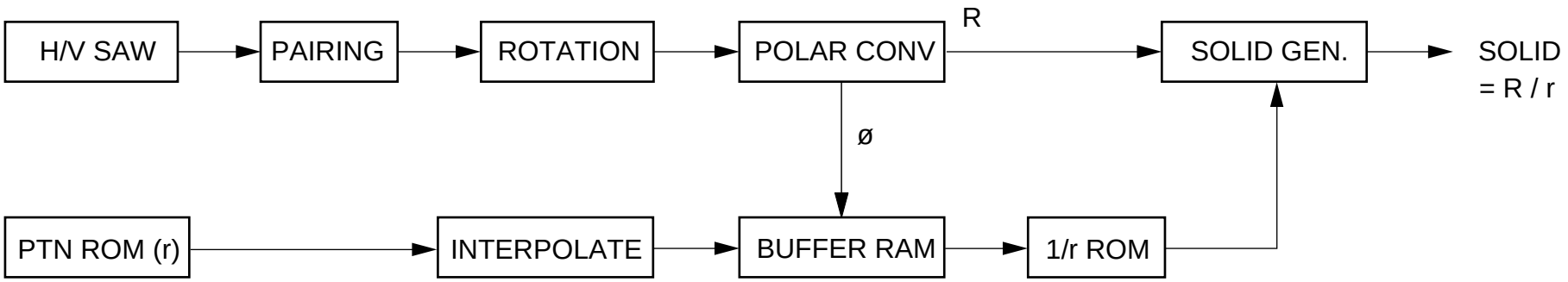
This represents the division of the screen between sources "A" and "B" during the "raster scan" of the Screen Plane, and therefore the production on a field-by-field basis of the control signal performing the wipe transition. *(The fader position is read, and the result calculated at field rate).*



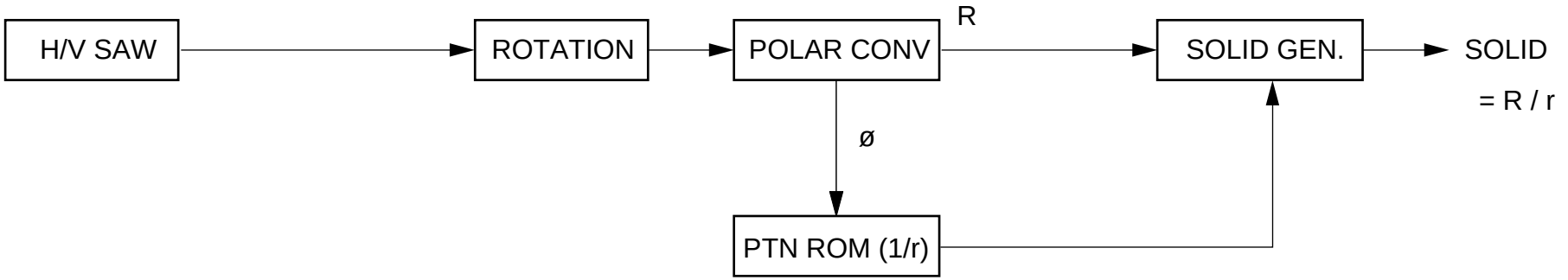


Generating Methods for Wipe Patterns

DVS-8000/C (indirect access)



DVS-6000/C (direct access)



Standard, Rotary and Circular Wipe

Standard wipe :

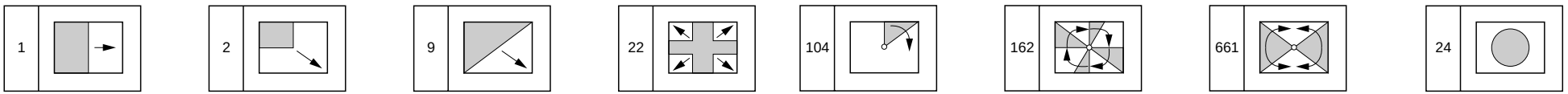
Addition or NAM of sawtooth or triangle waves in the Horizontal and Vertical Directions

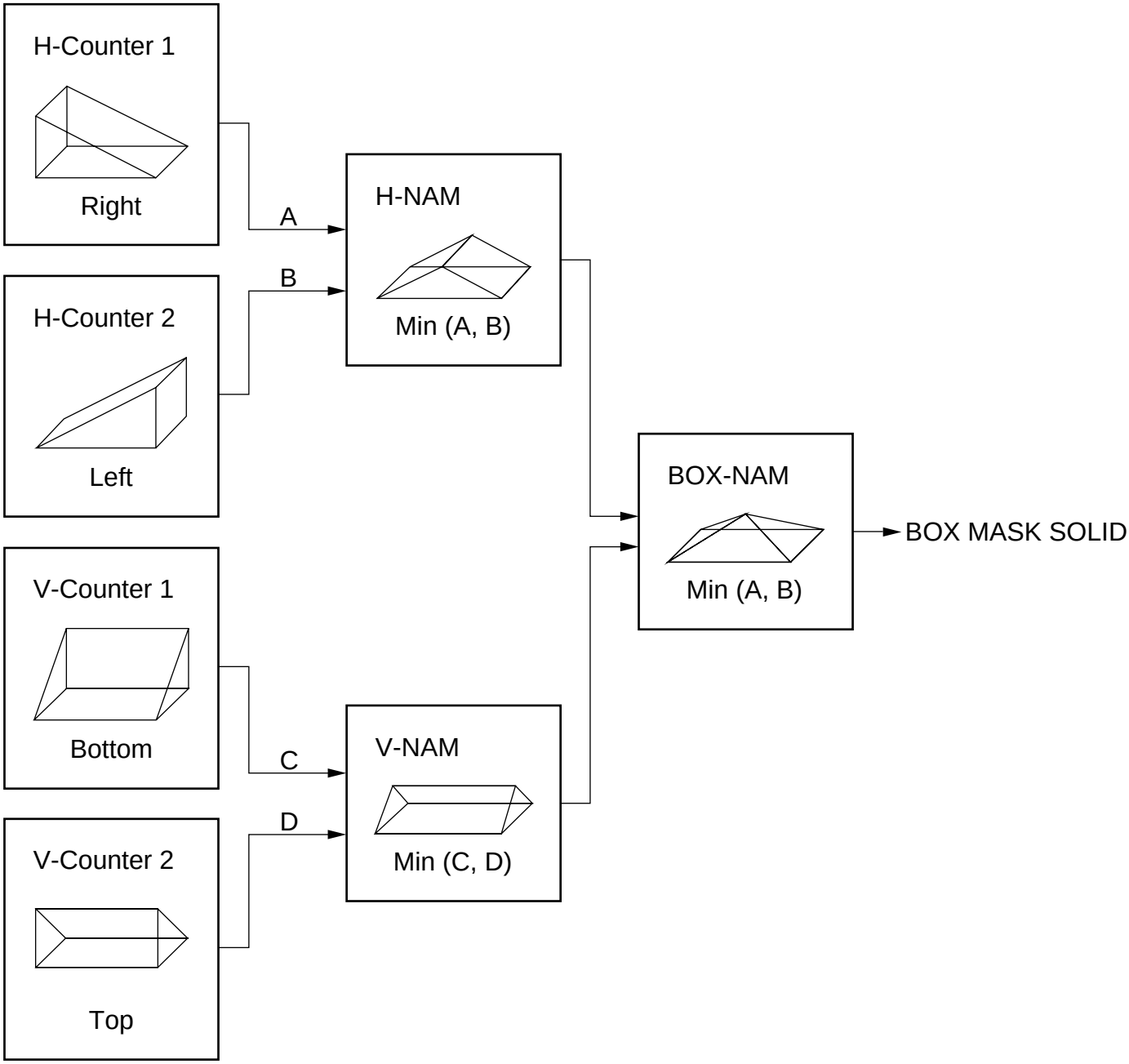
Rotary wipe :

NAM of sawtooth or triangle waves that are linked with the fader and Rotated

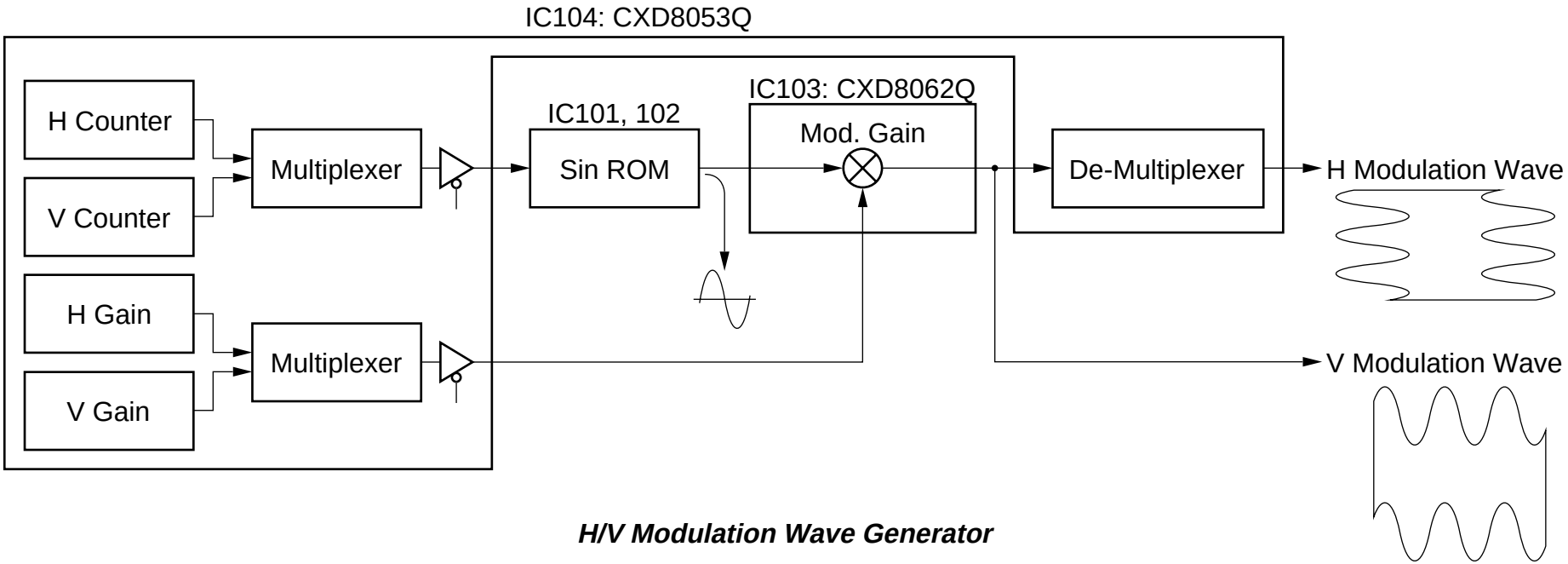
Circular wipe :.

Polar Conversion.





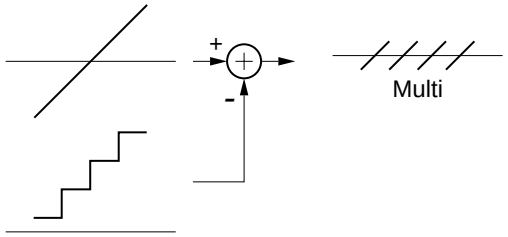
Box Generator IC100 (Box 1), IC200 (Box 2): CXD8053Q



H/V Modulation Wave Generator

H/V Sawtooth Generator

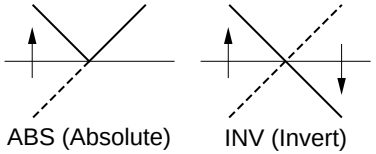
H/V Sawtooth Generator



Rotation

$$\begin{pmatrix} X \\ Y \end{pmatrix} = \begin{pmatrix} \cos(-ø) & \sin(-ø) \\ \sin(-ø) & \cos(-ø) \end{pmatrix} \begin{pmatrix} H \\ V \end{pmatrix}$$

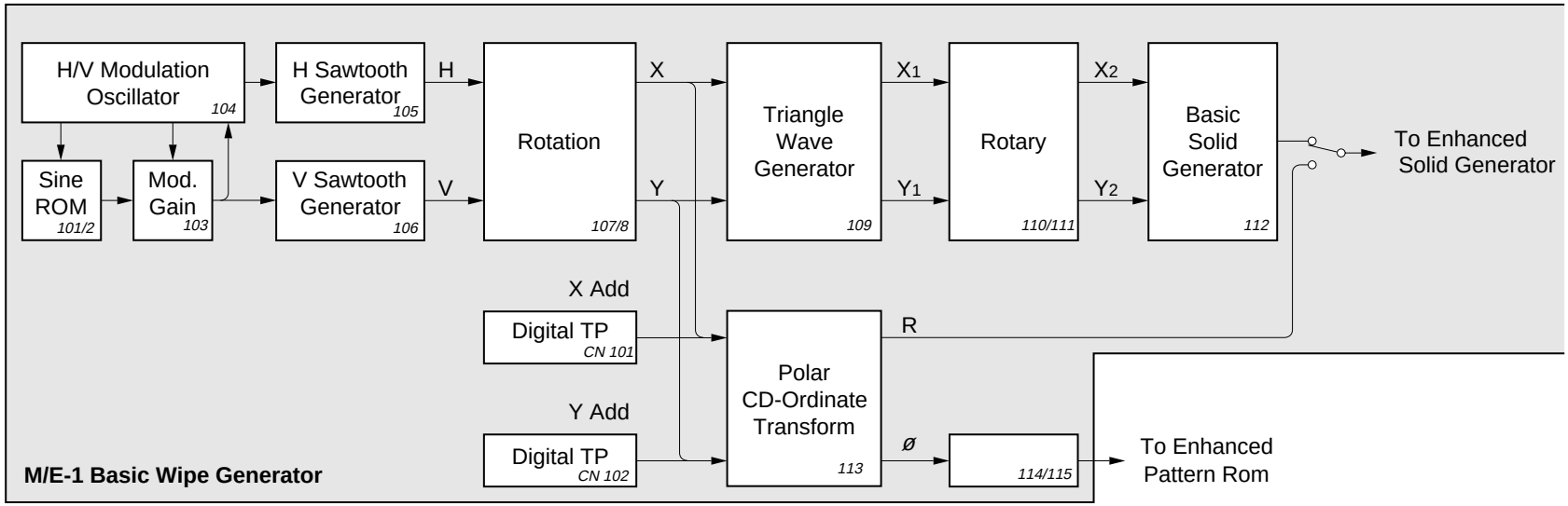
Triangle Wave Generator



Polar Coordinate Transform

$$R = \sqrt{X^2 + Y^2}$$

$$\theta = \tan^{-1}(Y/X)$$



Basic Solid Generator

MIX

$S = X_2 + Y_2 + [\text{Offset}]$

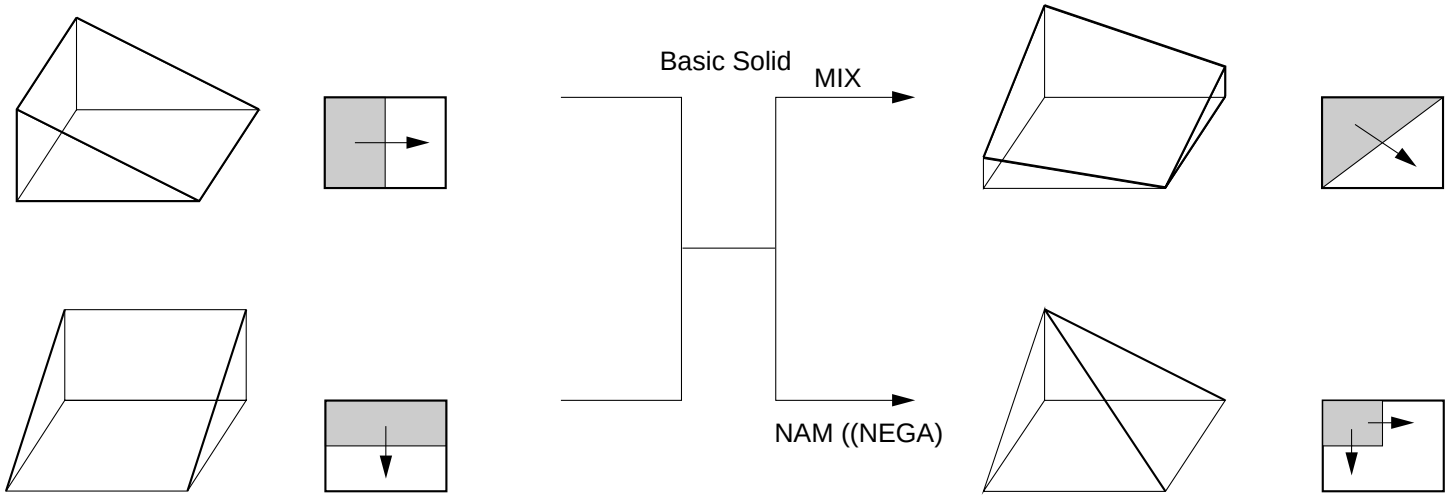
NAM (Positive)

$S = \text{Max}(X_2, Y_2) + [\text{Offset}]$

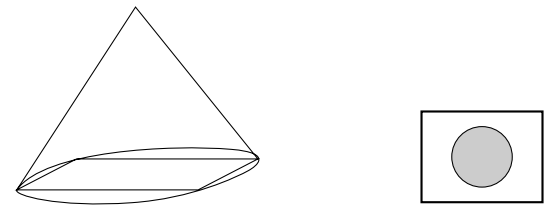
NAM (Negative)

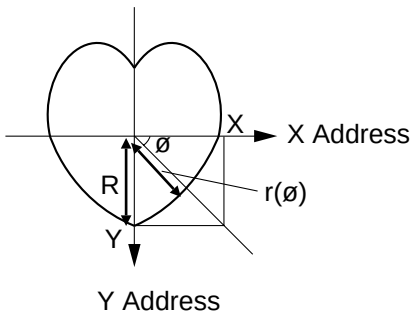
$S = \text{Min}(X_2, Y_2) + [\text{Offset}]$

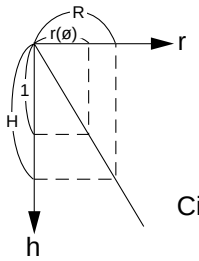
Wipe Solids



Enhanced Solid







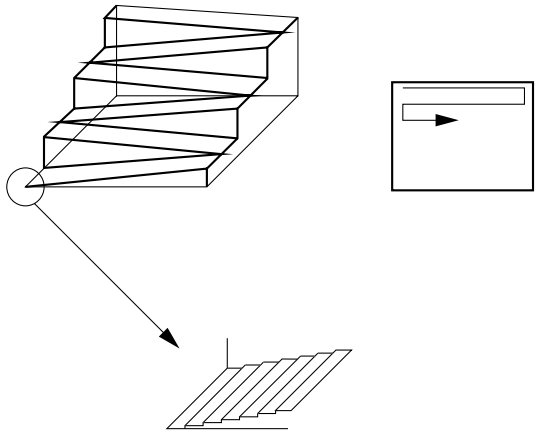
$$1 : r(ø) = H : R$$

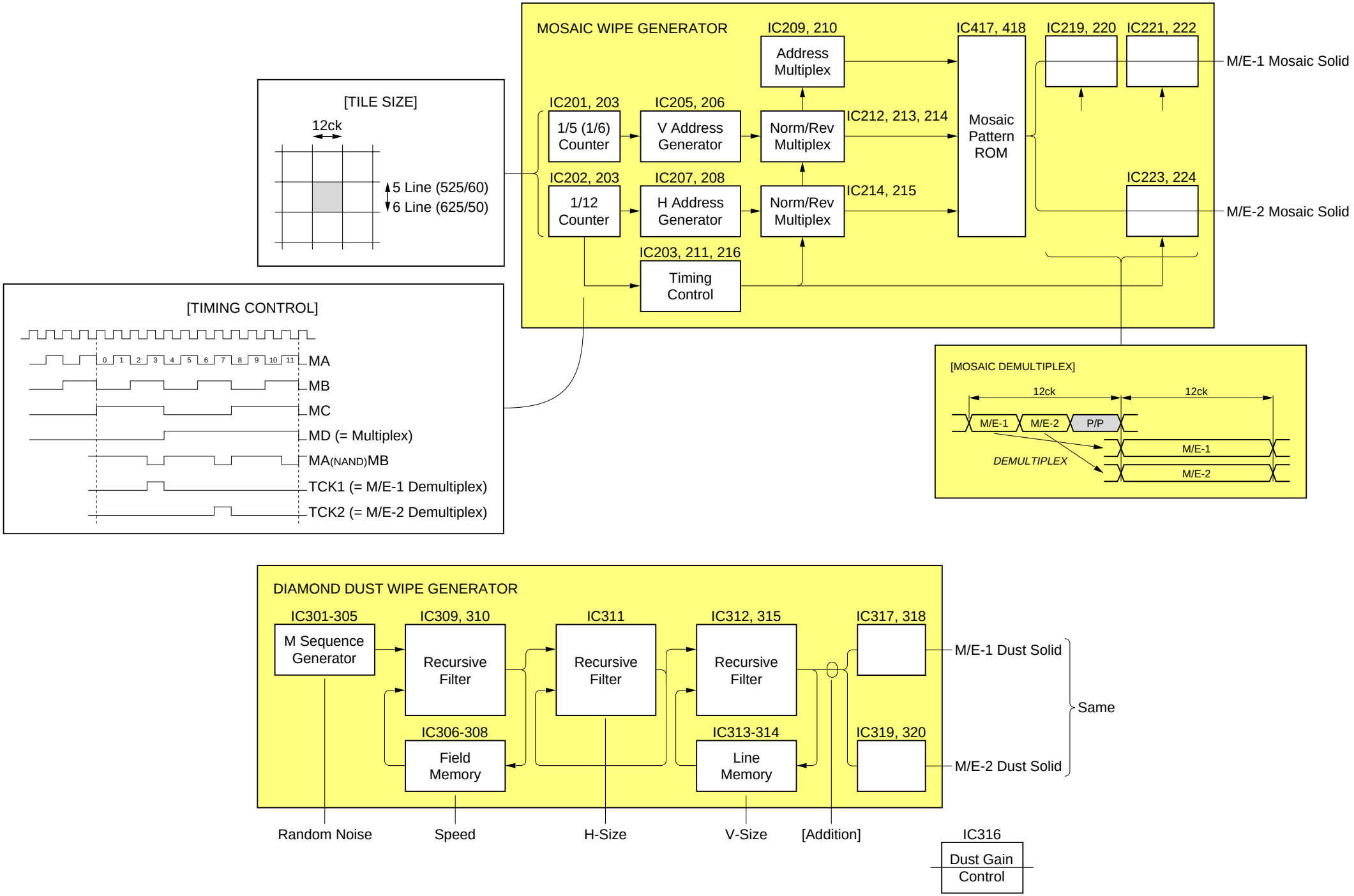
$$\frac{1}{r(ø)} = \frac{H}{R}$$

$$H = \frac{R}{r(ø)}$$

Circle Wipe : r(ø) = 1

Mosaic



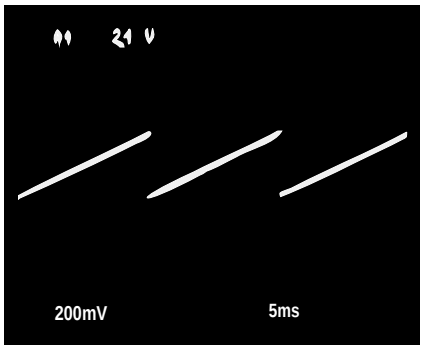


DVS-6000C Mosaic Wipe Generator which is based on the DVS-8000C (but omitting the P/P output) - note IC numbers apply to DVS-6000C ONLY

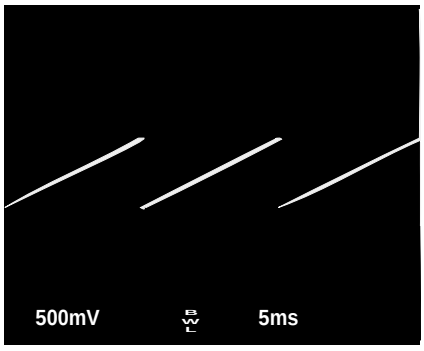
Waveforms for WKG-10 /WP-37 using Digital Test points and Test D-A Converter

(60Hz Format- interprete timings accordingly)

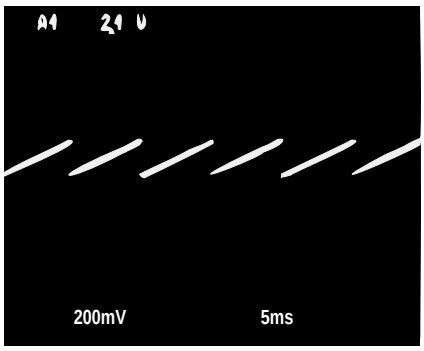
X Address



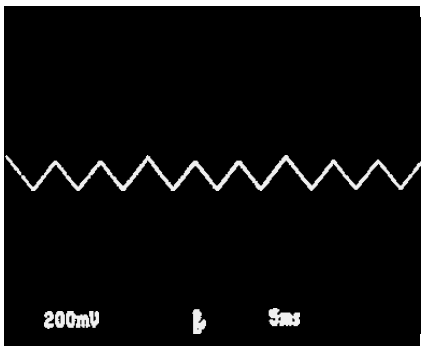
Y Address



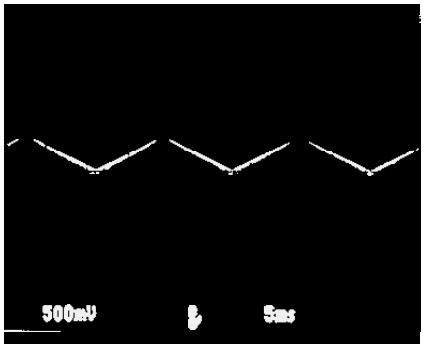
X Address (Multi)



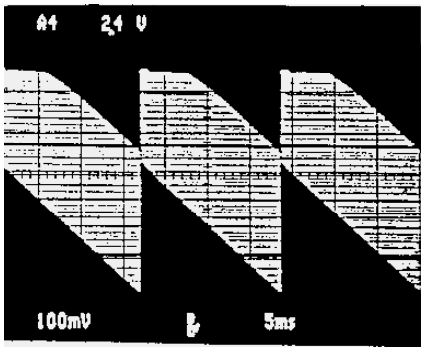
Y Address (Multi)



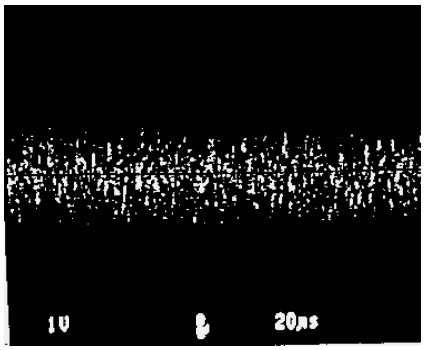
Wipe Solid WSLD (Circle)



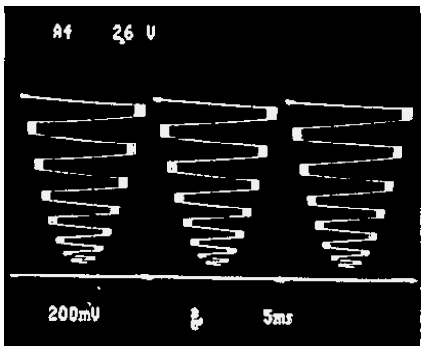
Wipe Solid WSLD (Diagonal)



WSLD (Diamond Dust)

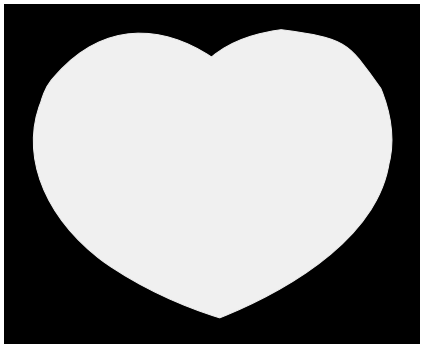


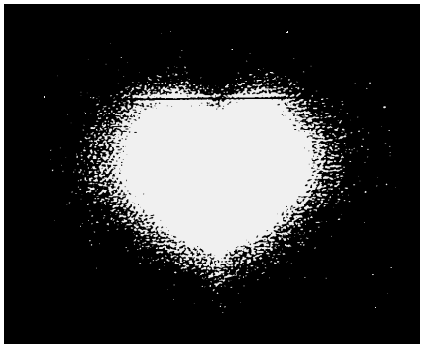
WSLD (Mosaic)



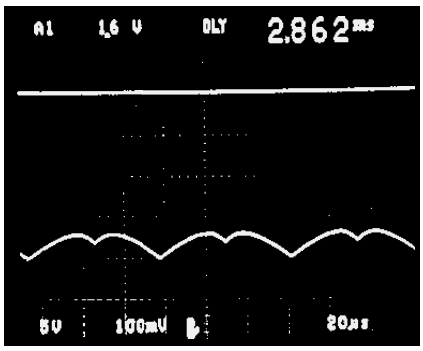
Waveforms for WKG-10 / WP-37 using Digital Test points and Test D-A Converter

Heart Pattern

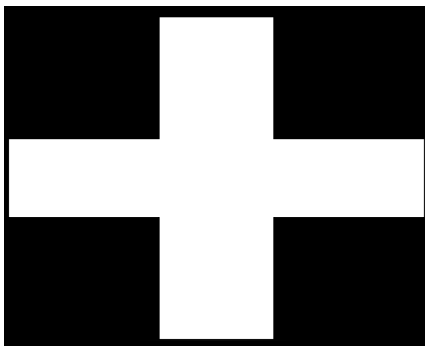




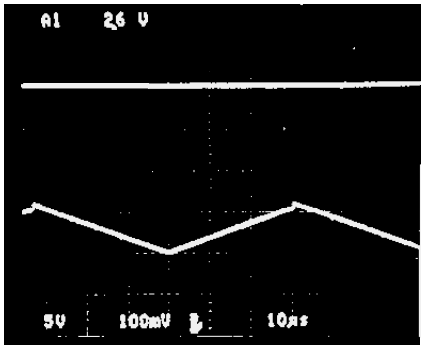
Solid



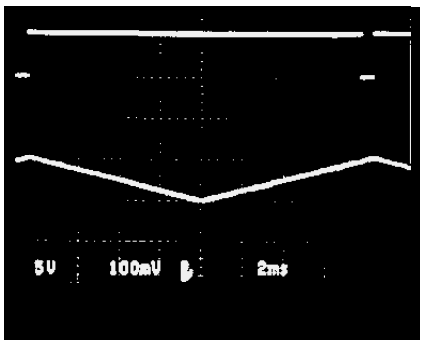
Cross Pattern Waveforms



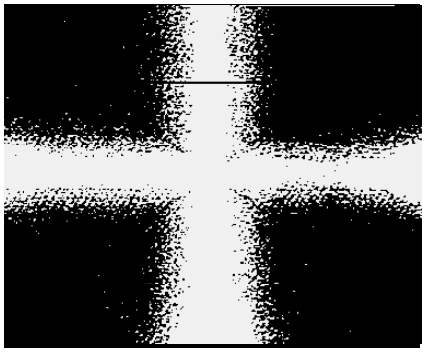
X ADD



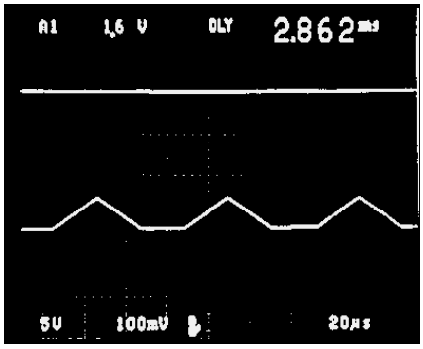
Y ADD



Cross with Diamond Dust



Solid



Frame Memory

Options

MY-51 or MY-67

MY-51 or MY-67 Options

Frame Memory

PDF Edition

Original Frame Memory Option MY-51 (BKDS-8041)

In D2 this comprises two sequential (NTSC) frames, for each channel, to avoid colour processing. In D1 this is used as a single frame / field store, *with Last X,* for each channel.

The MY-51 board has a single video input, which is shared between the two channels, and sourced from the Edit Preview bus in a DVS-8000C, or Aux 5 on a DVS-6000C.

The operation of the two channels may be "linked" together when required, allowing "Video" and "Key" to be controlled simultaneously. In this mode, the signal on the source bus is rapidly switched between two designated sources.

Later Frame Memory Option MY-67 (BKDS-6041)

For the DVS-6000C only, this uses two independant inputs, on Aux 5 and 6, but loses the "last-X" function. This is due to the use of "video Ram" allowing simultaneous reading and writing, and a potential connection to ans external SCSI interface at the rear.

When used in "Link" mode, the inputs are available simultaneously, using Aux 5 and Aux 6.

The Frame memory can be used in many ways:

The outputs are available as Primary sources via MAT-2/4 reentry Crosspoints, and also as direct Masks to the optional Chromakey boards.

Freeze:

1/ Whole frame or field grapping and display

2/ *Collage* Mode, in which successive grabs build up a complex image.

a/ The the new image can be restricted by area using the wipe of the corresponding M/E (i.e. M/E 1 wipe for Channel 1, and M/E2 wipe for Channel2), or by a box mask.

b/ The new image can be Non-additively mixed with the existing image.

c/ Methods (a) and (b) may be combined to allow NAMing only in a defined area.

Paint:

Using the corresponding M/E wipe solid generator as a "brush", any image on the source bus may be written into a defined area of the frame memory, which is continuosly adjustable using the positioning Joystick or an optional graphic tablet.

Repositioning a Still or Moving Image:

The image may be relocated in multiples of 2-pixel steps (colour), or 1-pixel steps (B+W).

The writing process may be applied continuously, giving a live repositioned (full size) image.

The B+W reposition mode is provided to allow pixel-registration adjustment of key channels to the corresponding video.

If masking an image, it is more effective to paint "black and white" into a frame memory channel, and use that as a key / mask, than to "paint out" the original image. (As in the difference between Crossfade and Clean key)

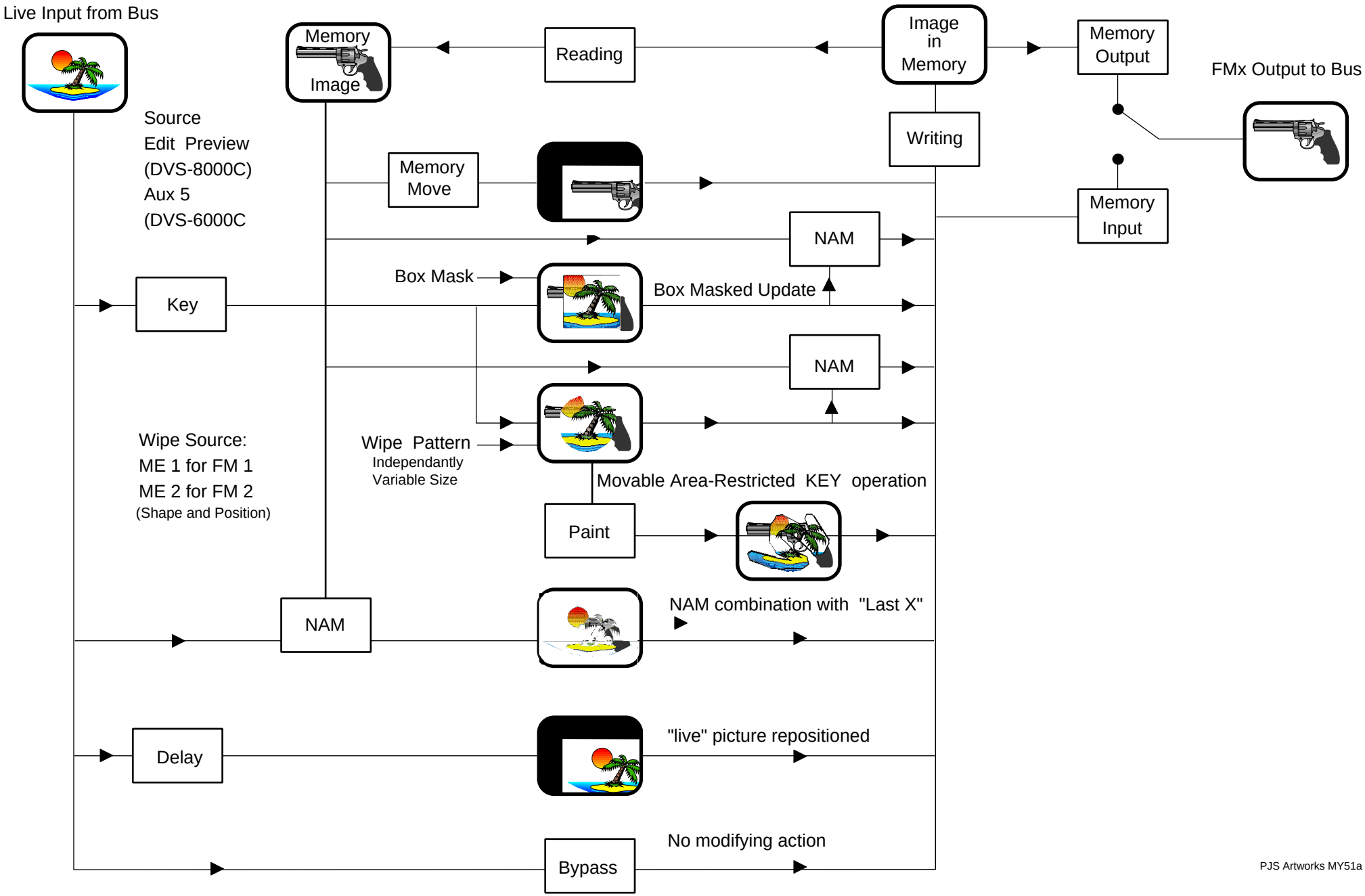
Balancing the Delay of a DME'd source.

The MY-51 provides a 1 frame throughput delay which can be used to match the same delay through a DME, at any position. As with a DME-Key transition, visible frame jumps can be avoided, wheras a single channel background DME transition will have a 1 frame jump.

The newer MY-67 board provides a 1 frame delay if the picture is at the original position, or higher, but not if the image is displayed lower down the screen (such as when matching a 4H key border drop)

Training and Engineering Information Department

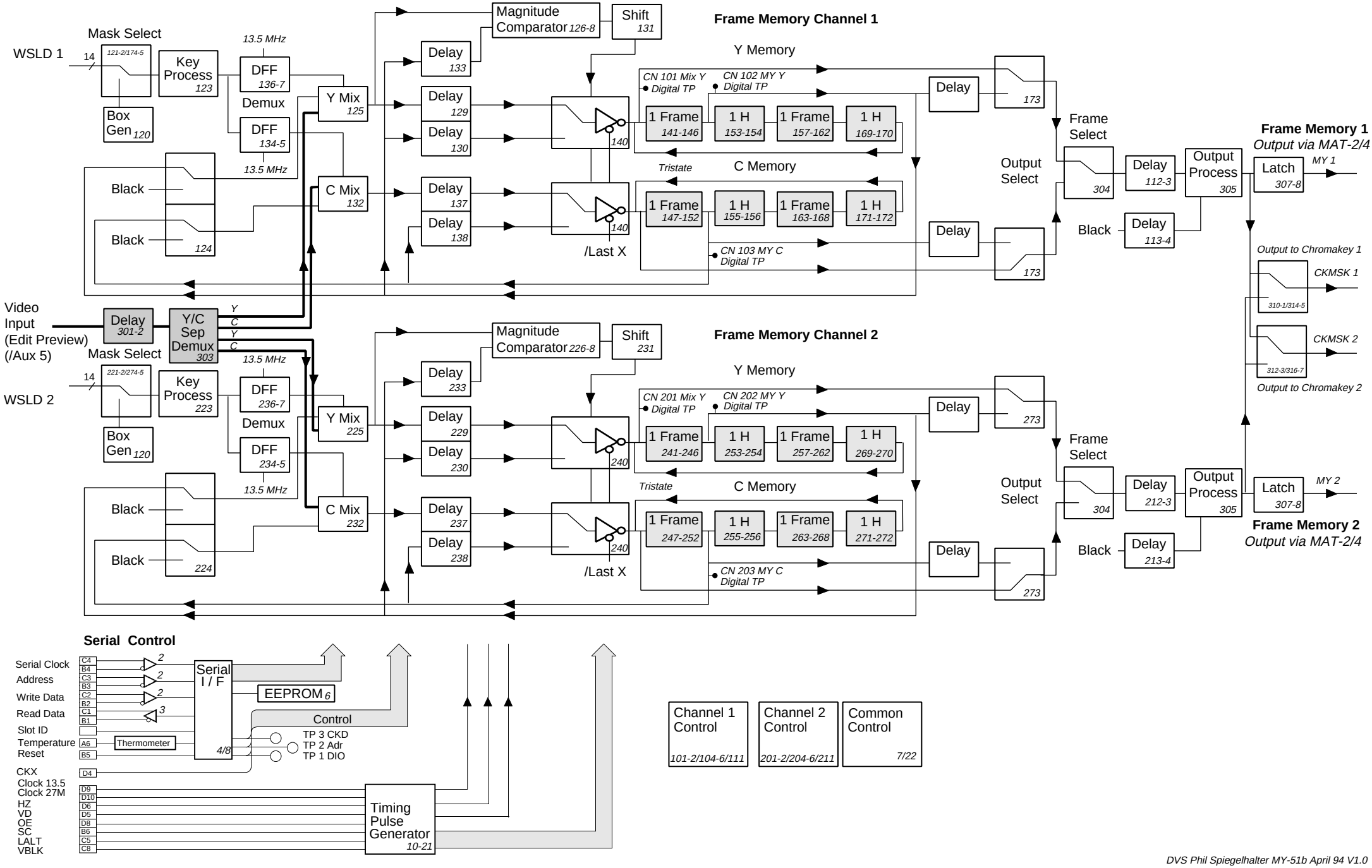
Frame Memory Option MY-51 BKDM-8041 Operational Flow Concept

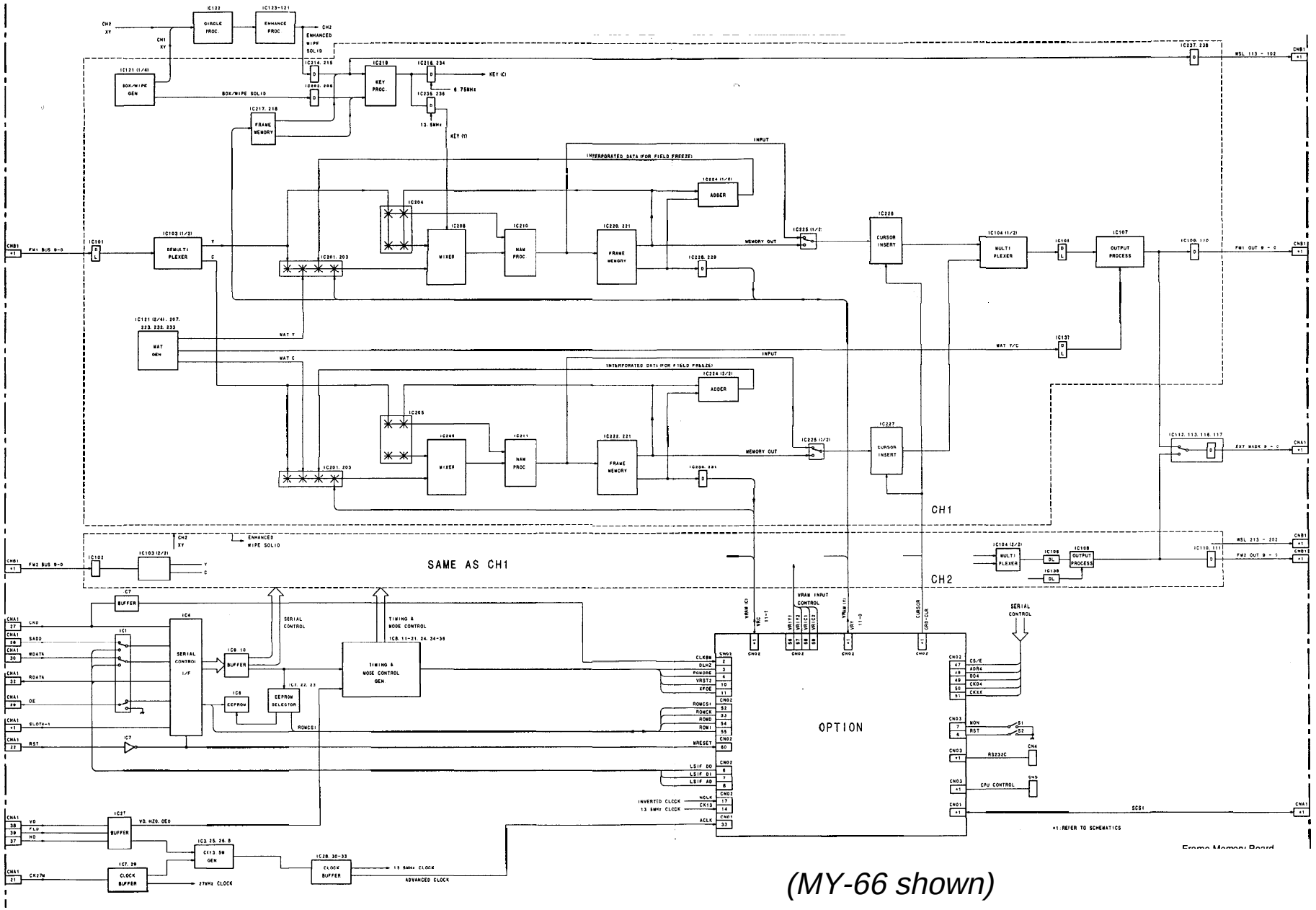


PJS Artworks MY51a

Training and Engineering
Information Department

Frame Memory Option MY-51 BKDM-8041




CH1
SAME AS CH1
CH2
OPTION
FRAME MEMORY
MIXER
KEY PROC.
ADDER
CURSOR INSERT
OUTPUT PROCESS
MULTI PLEXER
SERIAL CONTROL
TIMING & MODE CONTROL GEN.
EEPROM
BUFFER
CLOCK BUFFER
RS232C
CPU CONTROL
*1. REFER TO SCHEMATICS

(MY-66 shown)

Chromakey

Option

CRK-4

BKDS-8031

BKDS-8031
CRK-4
Option
Chromakey

PDF Edition

D1 Chromakey CRK-4

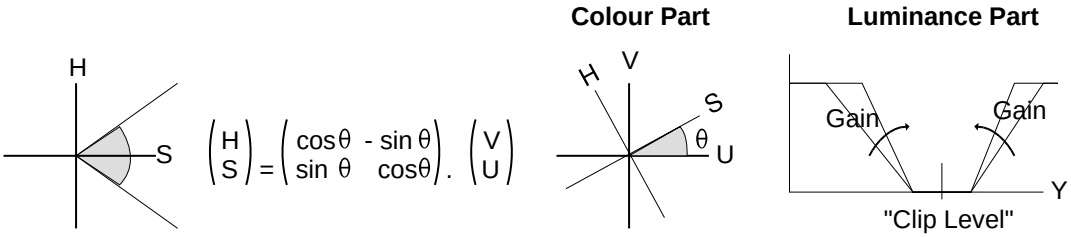
Input data is demultiplexed, the key is generated, and unwanted colour cancelled out
An independent mask, and foreground hue/gain control is provided.

Colour selection is either manual, in the conventional manner, using a "vectorscope" display on the display to select the hue, or fully automatic by positioning a variable size box on the screen, and 49 samples are then taken and averaged.

Basic Processing Method

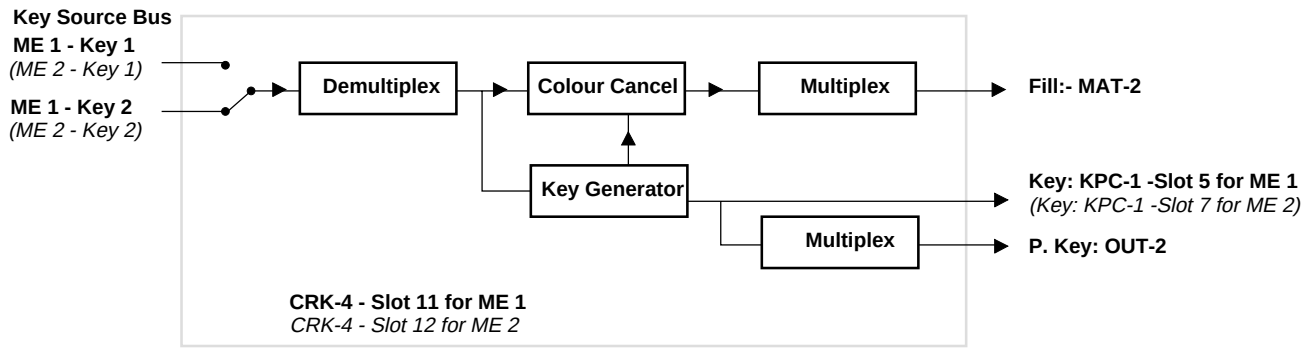
If S= Chromakey Axis, H= 90° from that axis, Y= luminance value of the key signal
The correlation to On-axis S and Off-axis H of the chosen colour is determmined by cos/sin
The absolute value of the off-axis result is taken, and has variable gain for selectivity

$$\begin{pmatrix} H \\ S \end{pmatrix} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} . \begin{pmatrix} V \\ U \end{pmatrix}$$



The two results are then summed to generate the basic key signal
The sensitivity to hues may be altered by the window adjustment
The Y balance value is then available as an offset if desired

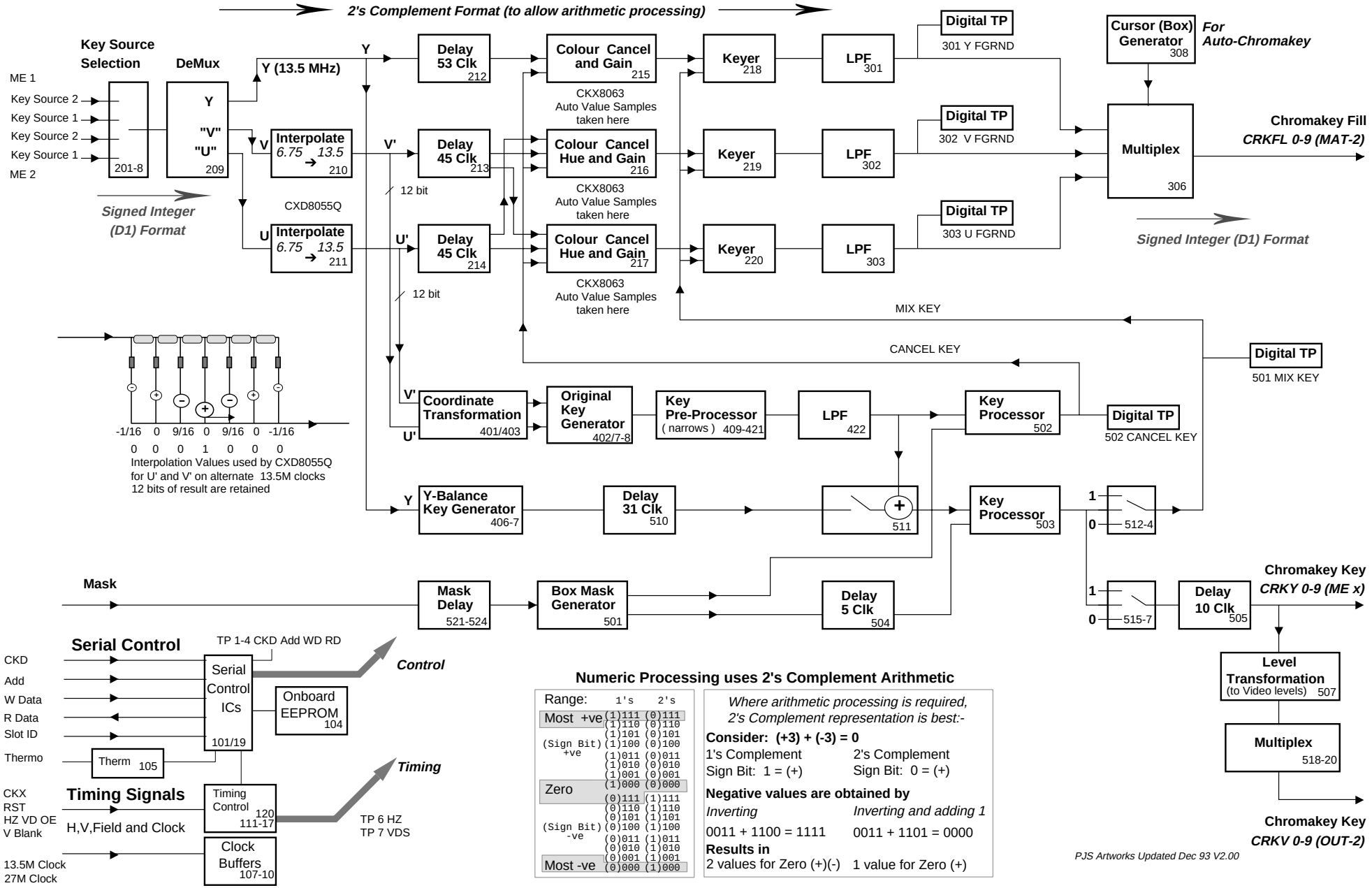
Due to the arithmetic processing, the signal is converted from signed integer (D1) to 2's compliment, by inverting the MSB.
Slot 11 is for M/E 1, Slot 12 is for M/E 2. [BKDS-8031]



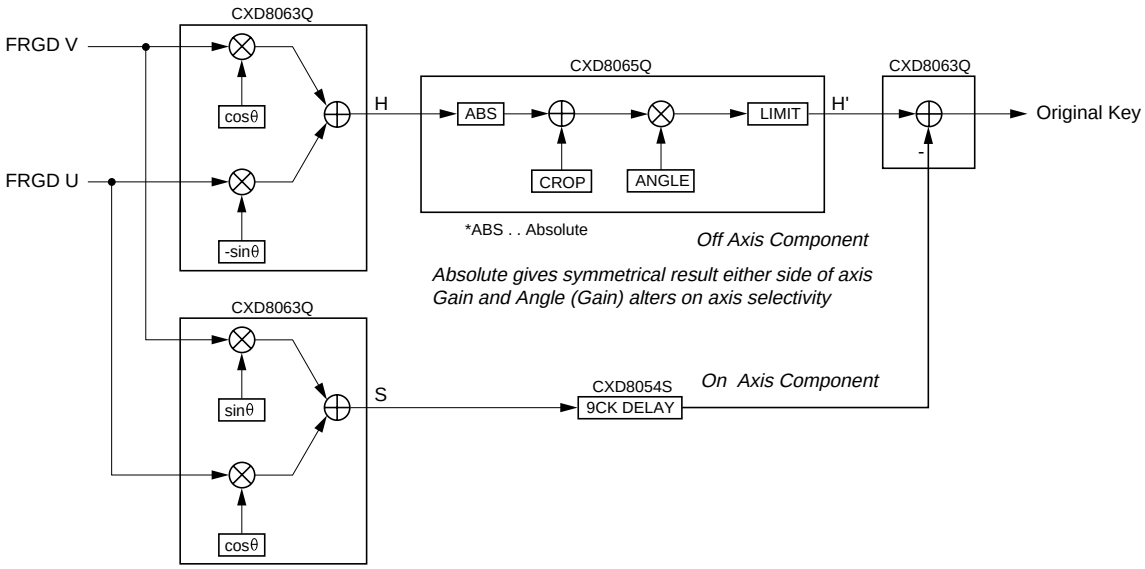
The following diagrams provide a step by step guide to the processing...

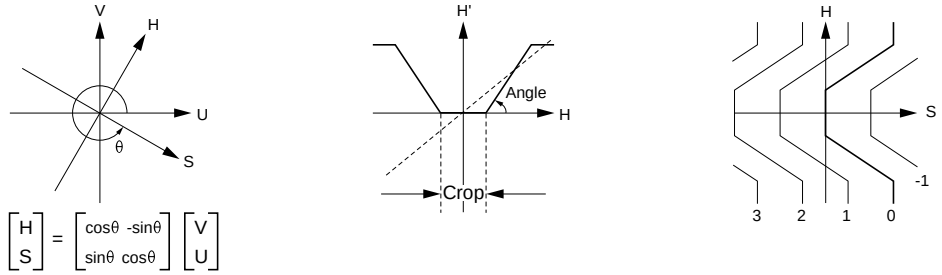
Training and Engineering Information Department

CRK-4 Chromakey Option BKDS-8031



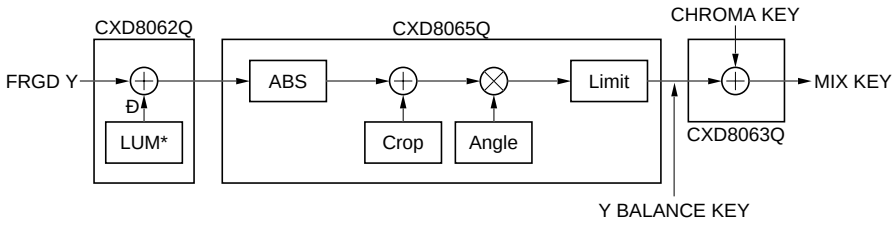
Original Key Gen.





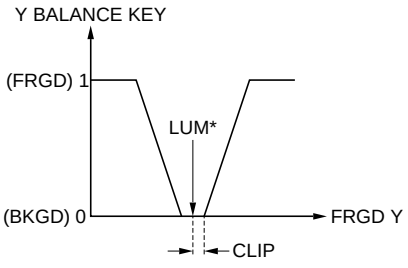
$$\begin{bmatrix} H \\ S \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V \\ U \end{bmatrix}$$

(A) Coordinate Transformation (B) Window (C) Original Key



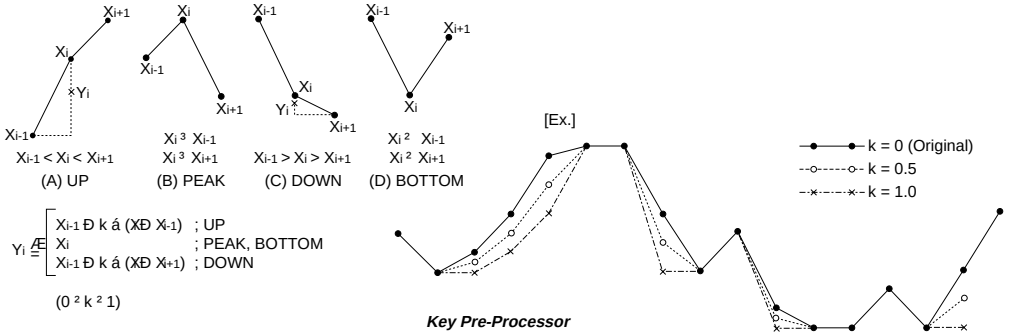
Y Balance Key Generator

*"Y Balance Luminance" must be same as 'Back Colour Luminance".

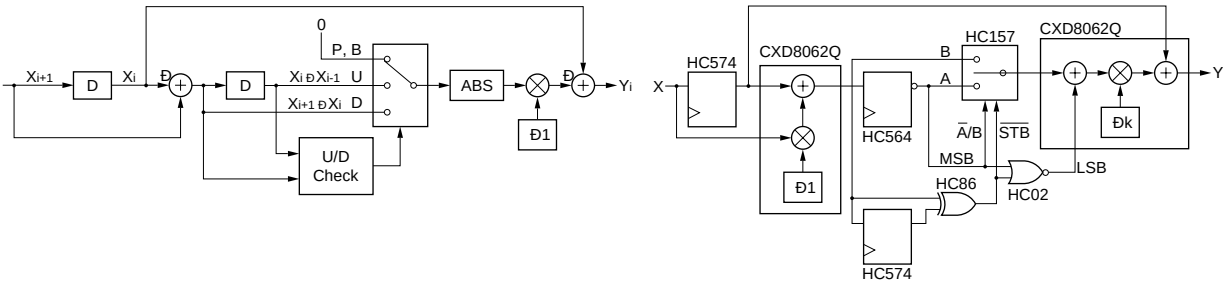


Y Balance Key

Y Balance Key Generator and Y Balance Key



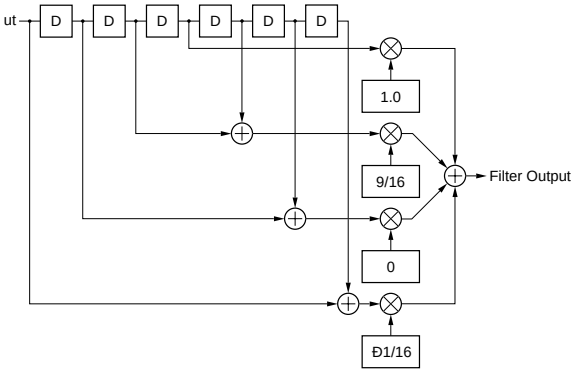
Key Pre-Processor



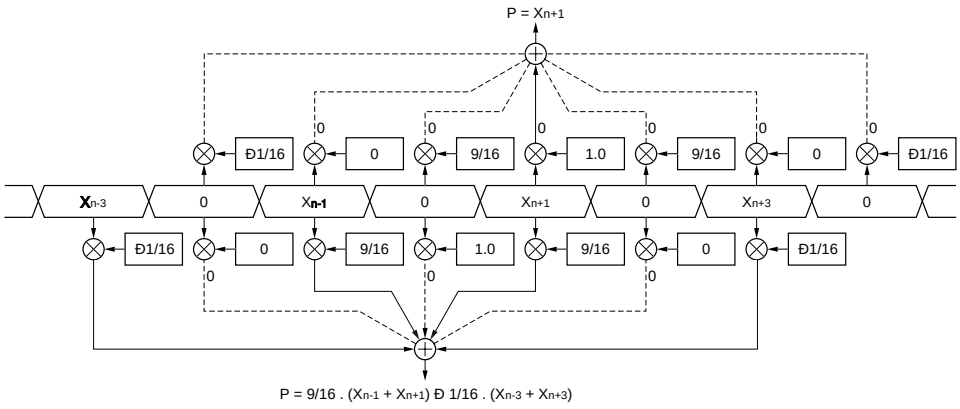
(A) Logical Circuit

Key Pre-Processor Circuit

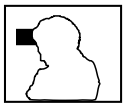
(B) Actual Circuit (CRK-4/CRK-5)



Architecture of CXD8055Q



(*1)
When Colour Cancel = ON
(Colour Cancel = OFF:
KEY = "0")

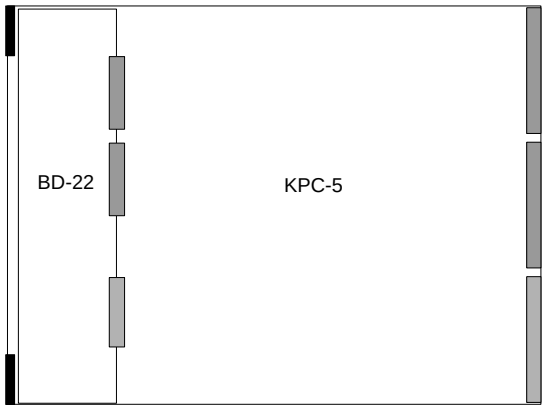
<table>
<tr><th>Auto Chroma Key</th><th>Output Key</th><th>MASK</th><th>Forced FRGD</th><th>MASK Invert</th><th>KEY for MIX</th><th>KEY for COLOUR CANCEL (*1)</th></tr>
<tr><td rowspan="9">OFF</td><td rowspan="3">OFF</td><td>OFF</td><td>X</td><td rowspan="2">X</td><td rowspan="3"> 
KEY = "1"</td><td>  </td></tr>
<tr><td rowspan="2">ON</td><td>OFF</td><td>  </td></tr>
<tr><td rowspan="2">ON</td><td>OFF</td><td>  </td></tr>
<tr><td rowspan="6">ON</td><td>OFF</td><td>X</td><td>X</td><td>  </td><td rowspan="4">  </td></tr>
<tr><td rowspan="4">ON</td><td rowspan="2">OFF</td><td>OFF</td><td>  </td></tr>
<tr><td>ON</td><td>  </td></tr>
<tr><td rowspan="2">ON</td><td>OFF</td><td>  </td><td>  </td></tr>
<tr><td>ON</td><td>  </td><td>  </td></tr>
<tr><td>ON</td><td>X</td><td>X</td><td>X</td><td>X</td><td> 
KEY = "1"</td><td> 
KEY = "0"</td></tr>
</table>

Key Process

KPC-5

PDF Edition

KPC-5 and BD-22 Option (BKDS-6071)



KPC-5 board / BD-22 (Option)
Key Processor for M/E 1 (Slot 5) or M/E 2 (Slot 7)

Mask with Clip, Gain, and Box Generator
Key Process with Clip, Gain, Invert
Transition Processor: Fader, Wipe Border, Wipe Softness
Mach cancel rounds off Luminace key / Pattern Key transitions ($\sin^2 x$)

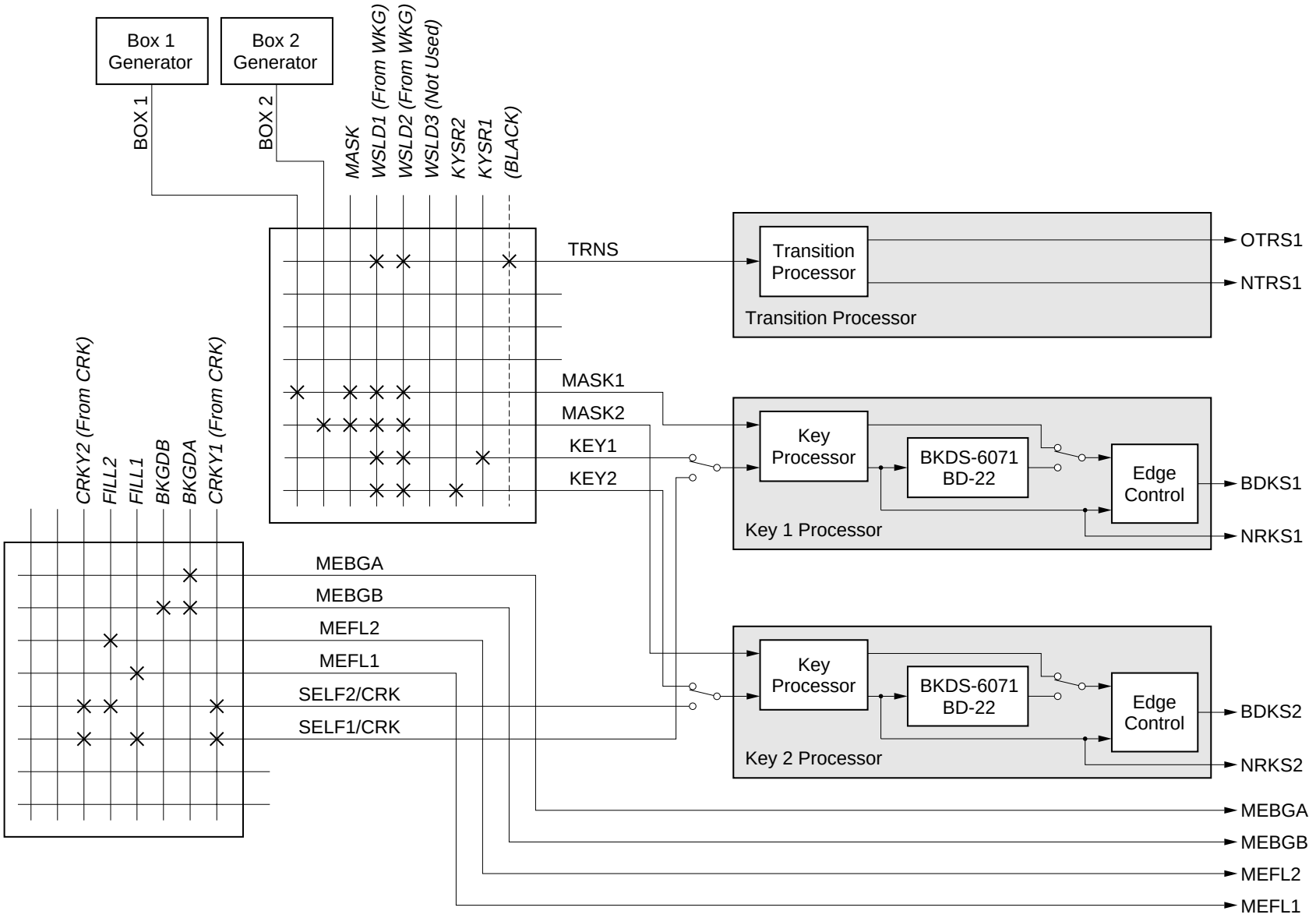
BD-22 (Option)
Key Edge Processor: Typw, Width, Position, Softness
2 x 4 lines of delay (4H drop or 8H drop modes)

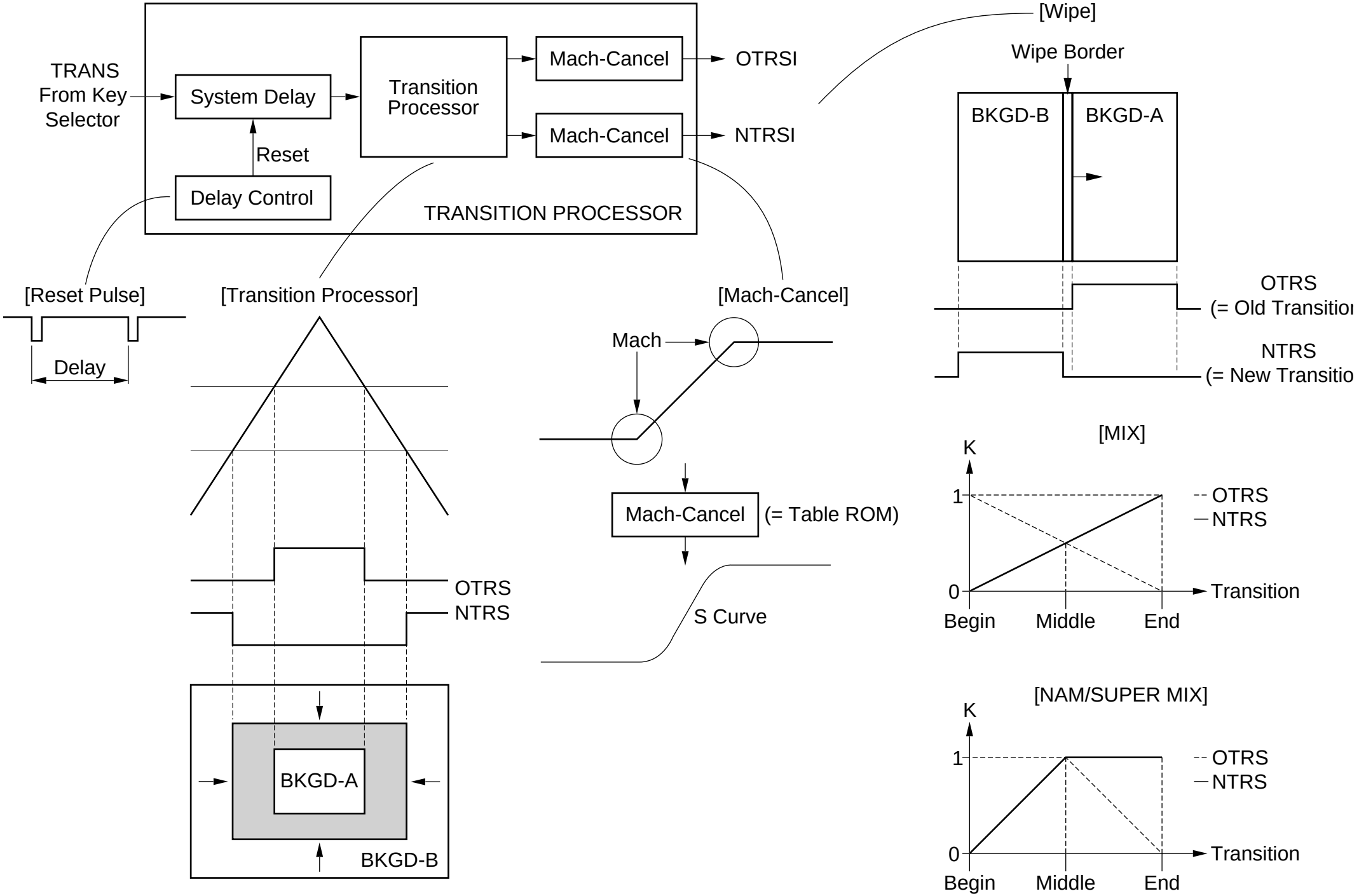
Results sent to:
MIX-8(A) Video mixing for M/E 1 (Slot 6) or M/E 2 (Slot 8)

When the “Next Transition” is set to Key only, the background B bus leaving this board for the MIX-8(A) carries the same signal as the Background A bus, allowing the result of the next transition to be previewed correctly.

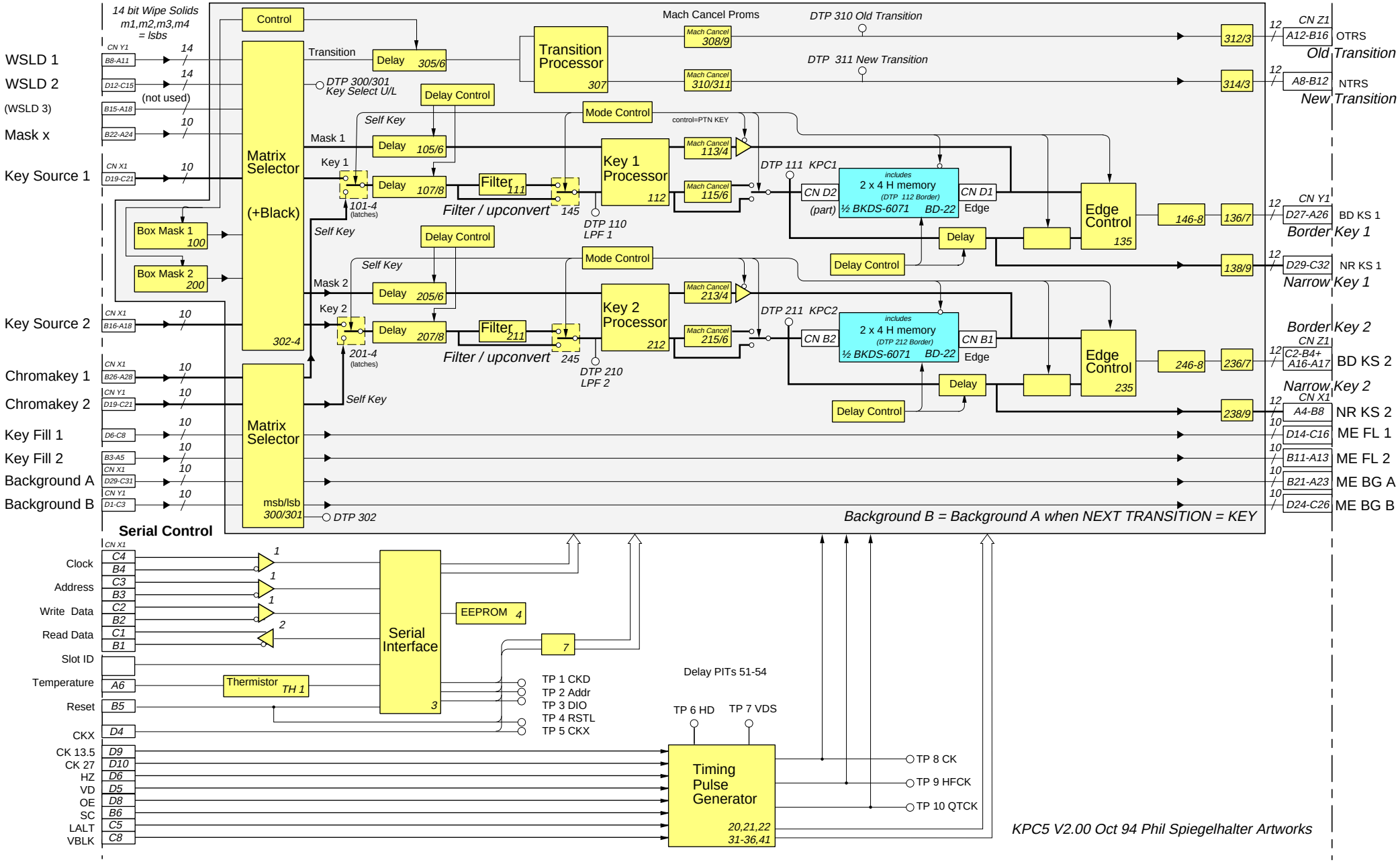
Note:
DSK-9(A) (Slot 9)
Functionally similar to KPC-5, but with only 1 Key.
Mixing Stage dissimilar to MIX-8(A) since a Cascade X-fade is used to provide an intermediate Clean output.

KPC-5 Board + BD-22 Board (BKDS-6071: Key Border Processor)

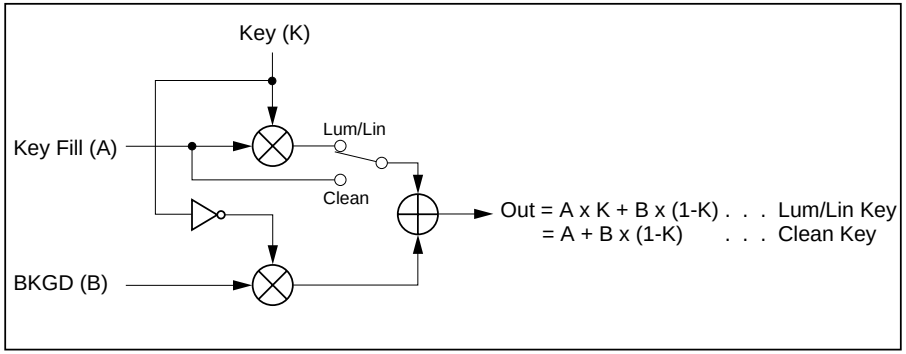


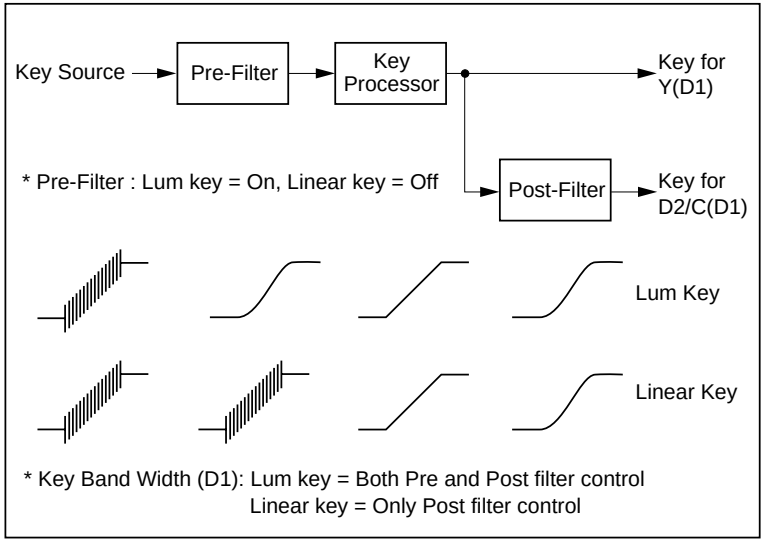


Transition Processor

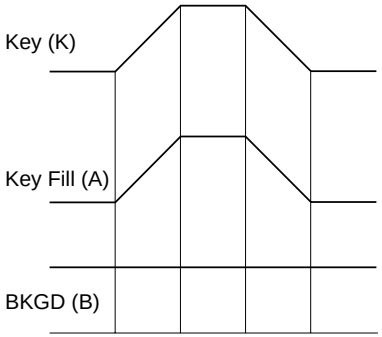

14 bit Wipe Solids
m1,m2,m3,m4
= lsbs
WSLD 1
WSLD 2
(not used)
(WSLD 3)
Mask x
Key Source 1
Key Source 2
Chromakey 1
Chromakey 2
Key Fill 1
Key Fill 2
Background A
Background B
Control
Matrix Selector
(+Black)
302-4
Box Mask 1 100
Box Mask 2 200
Matrix Selector
msb/lsb
300/301
DTP 302
Transition
DTP 300/301
Key Select U/L
Delay 305/6
Delay Control
Transition Processor 307
Mach Cancel Proms
Mach Cancel 308/9
Mach Cancel 310/311
DTP 310 Old Transition
DTP 311 New Transition
312/3
314/3
CN Z1
A12-B16
OTRS
Old Transition
A8-B12
NTRS
New Transition
Self Key
Mask 1
Key 1
Delay 105/6
Delay 107/8
Filter 111
101-4
(latches)
Filter / upconvert
145
DTP 110
LPF 1
Mode Control
control=PTN KEY
Key 1 Processor 112
Mach Cancel 113/4
Mach Cancel 115/6
DTP 111 KPC1
includes
2 x 4 H memory
(DTP 112 Border)
½ BKDS-6071 BD-22
CN D2
(part)
CN D1
Edge
Edge Control 135
146-8
136/7
CN Y1
D27-A26
BD KS 1
Border Key 1
Delay
Delay Control
138/9
D29-C32
NR KS 1
Narrow Key 1
Mask 2
Key 2
Delay 205/6
Delay 207/8
Filter 211
201-4
(latches)
Filter / upconvert
245
DTP 210
LPF 2
Key 2 Processor 212
Mach Cancel 213/4
Mach Cancel 215/6
DTP 211 KPC2
includes
2 x 4 H memory
(DTP 212 Border)
½ BKDS-6071 BD-22
CN B2
CN B1
Edge
Edge Control 235
246-8
236/7
Border Key 2
CN Z1
C2-B4+
A16-A17
BD KS 2
Narrow Key 2
238/9
CN X1
A4-B8
NR KS 2
D14-C16
ME FL 1
B11-A13
ME FL 2
B21-A23
ME BG A
D24-C26
ME BG B
Background B = Background A when NEXT TRANSITION = KEY
Serial Control
Clock
Address
Write Data
Read Data
Slot ID
Temperature
Reset
CKX
CK 13.5
CK 27
HZ
VD
OE
SC
LALT
VBLK
Serial Interface 3
EEPROM 4
7
Thermistor TH 1
TP 1 CKD
TP 2 Addr
TP 3 DIO
TP 4 RSTL
TP 5 CKX
Delay PITs 51-54
TP 6 HD
TP 7 VDS
Timing Pulse Generator
20,21,22
31-36,41
TP 8 CK
TP 9 HFCK
TP 10 QTCK
KPC5 V2.00 Oct 94 Phil Spiegelhalter Artworks

Clean Key, Lum Key, Linear Key

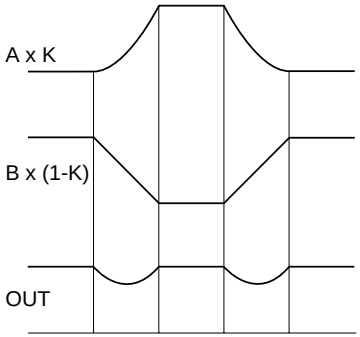




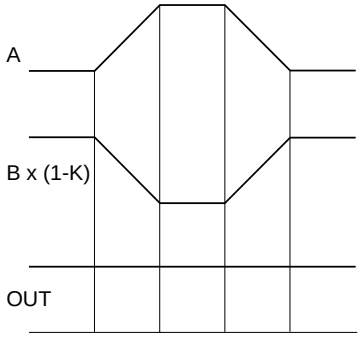
Input from Anti-Aliased Key Source



Lum/Lin Key



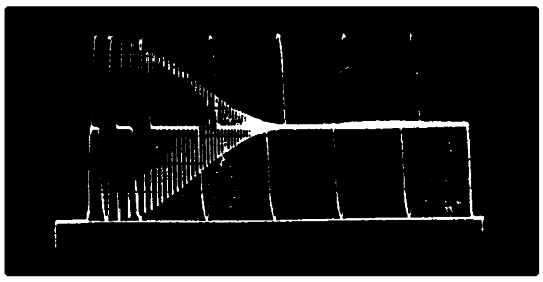
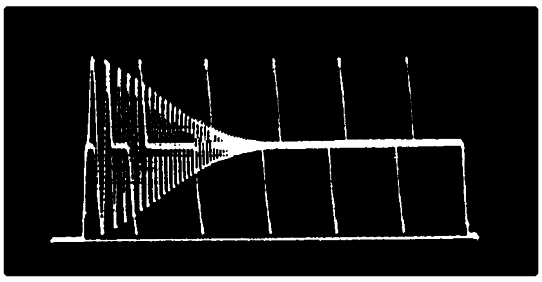
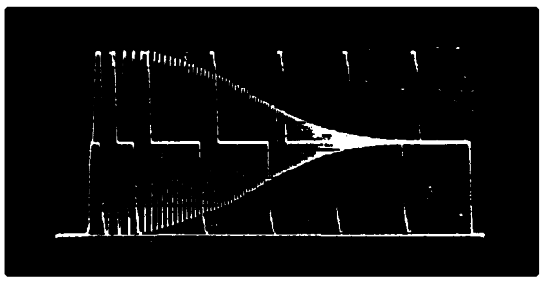
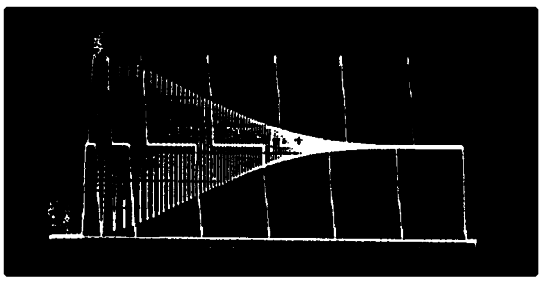
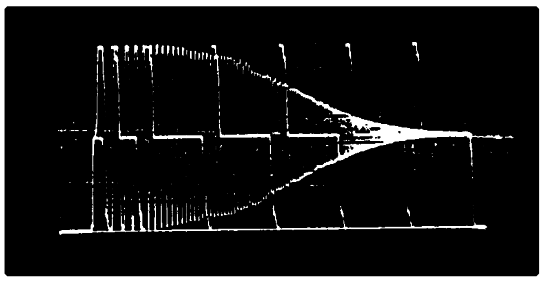
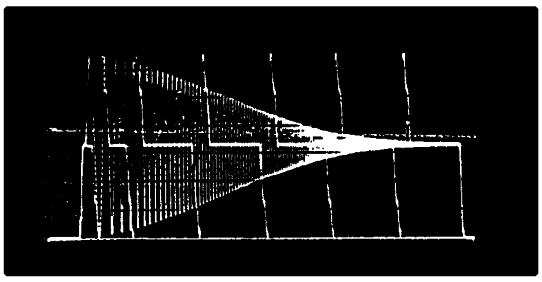
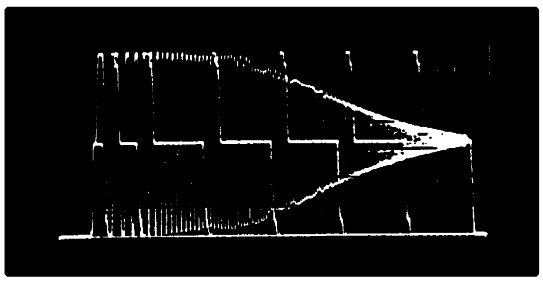
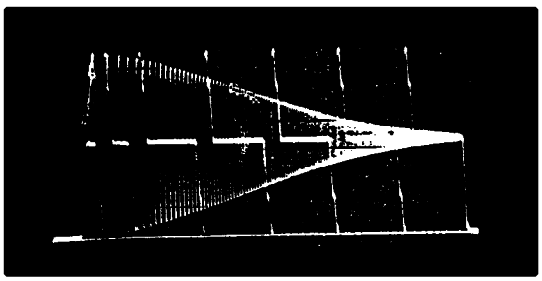
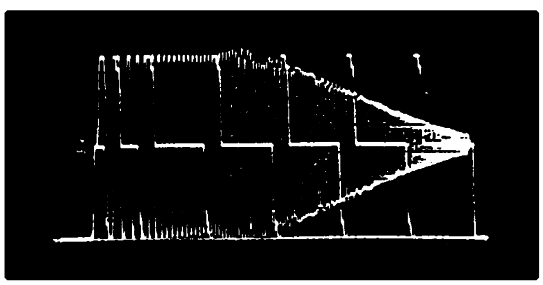
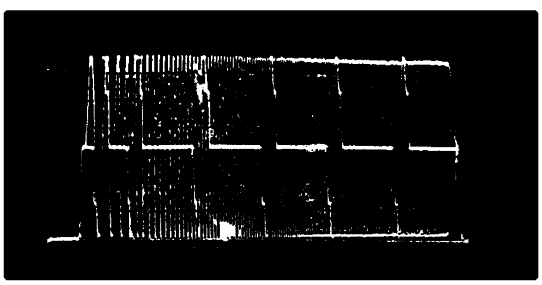
Clean Key



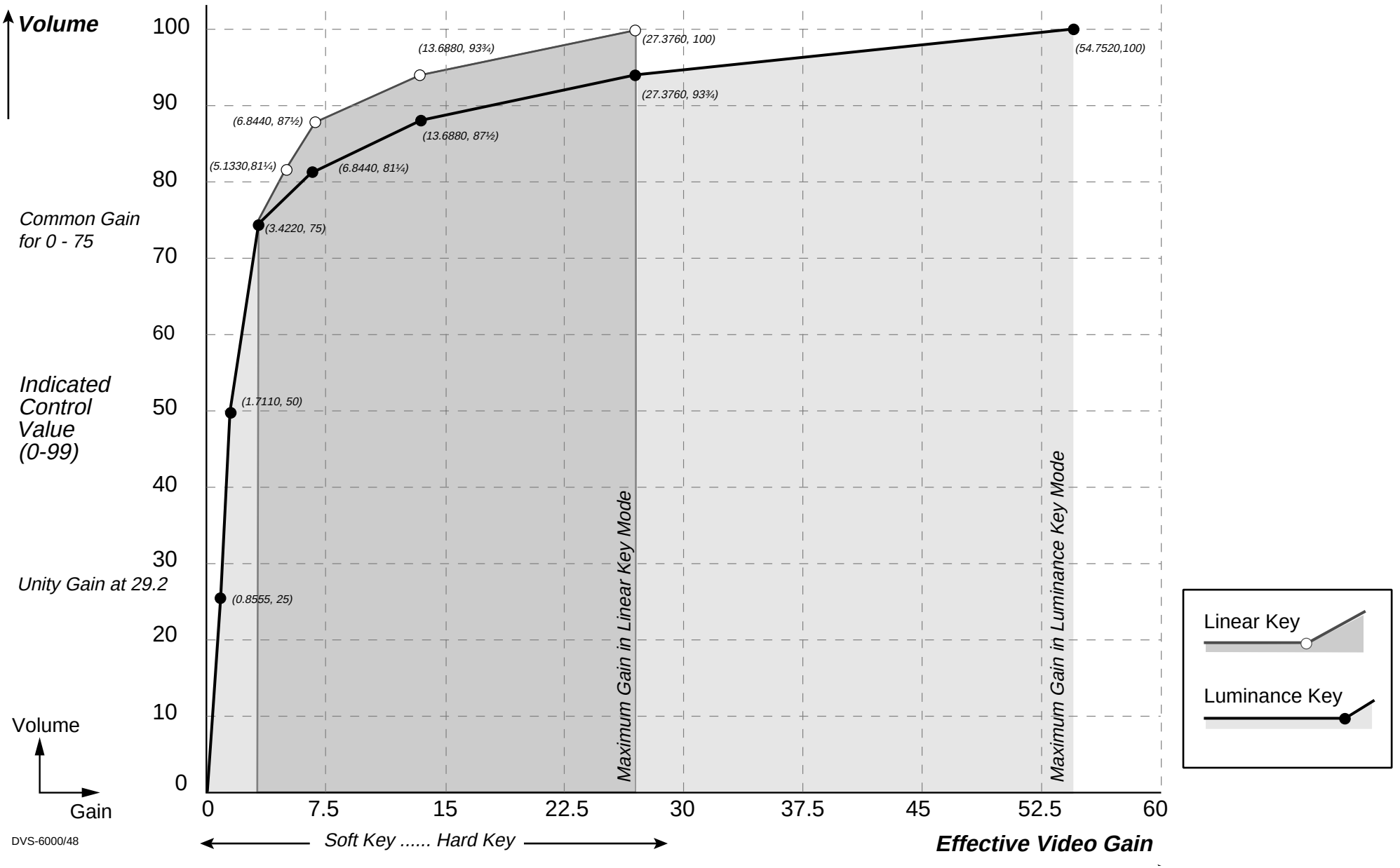
* Clean key: Key Mask Modify and Key Edge Modify are not available.

Technical
Training

Luminance v Linear Key Bandwidth (5 steps)

Luminance		Linear
	Type 1	
		
	Type 2	
		
	Type 3	
		
	Type 4	
		
	Type 5	
		

Key Gain v Volume Chart for DVS-8000C / DVS-6000C



DVS-6000/48

Conversion Table of the KEY GAIN and VOLUME for DVS-8000 / C
(As is May 27, 1992)

Table #1

Conversion table from the Volume to the Key Gain.
Upper ( ) --- Magnification
Lower --- Gain = (Magnification) x (a Multiply : D1 --- 0.8555, D2 --- 0. 5469)

Gain / Volume	D2 x 0.5469		D1 x 0.8555	
	LUM KEY	LIN KEY	LUM KEY	LIN LEY
000	(0.0) 0.0	(0.0) 0.0	(0.0) 0.0	(0.0) 0.0
250	(1.0) 0.5469	(1.0) 0.5469	(1.0) 0.8555	(1.0) 0.8555
500	(2.0) 1.0938	(2.0) 1.0938	(2.0) 1.7110	(2.0) 1.7110
750	(4.0) 2.1876	(4.0) 2.1876	(4.0) 3.4220	(4.0) 3.4220
812.5	(8.0) 4.3752	(6.0) 3.2814	(8.0) 6.8440	(6.0) 5.1330
875	(16.0) 8.7504	(8.0) 4.3752	(16.0) 13.6880	(8.0) 6.8440
937.5	(32.0) 17.5008	(16.0) 8.7504	(32.0) 27.3760	(16.0) 13.6880
999 (=1000)	(64.0) 35.0016	(32.0) 17.5008	(64.0) 54.7520	(32.0) 27.3760

Note : *The gain curve has non-linear characteristic. But using above table, it is easy to calculate the gain of any necessary volume.
**The Gain 1.0 means the unity gain. (The definition of the unity is, 100 % or 100 IRE level difference are required between white level and black level of the key signal.)

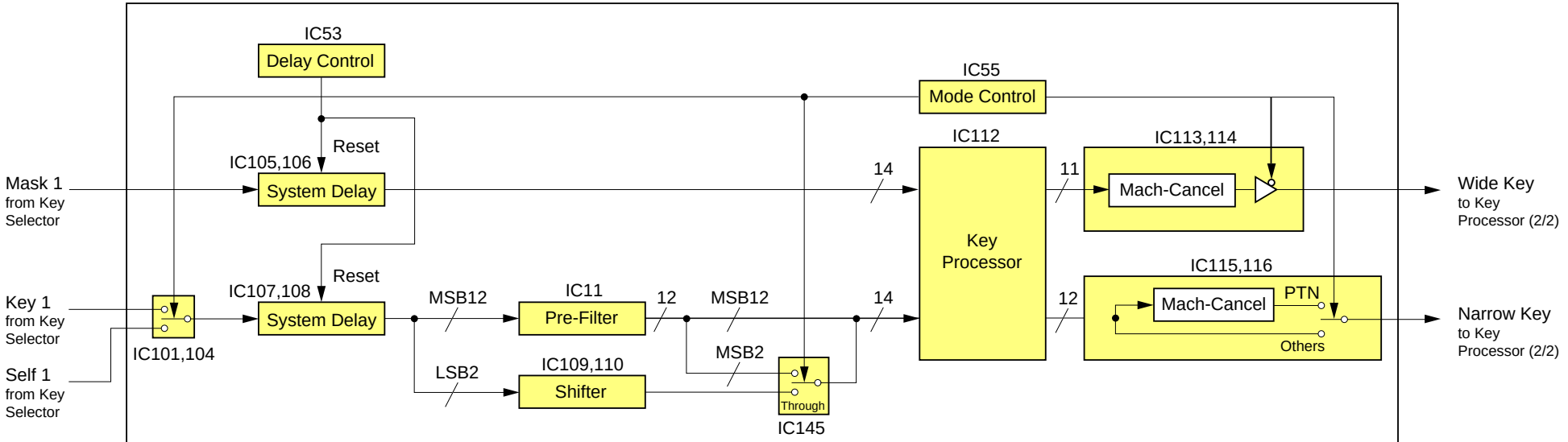
Table #2

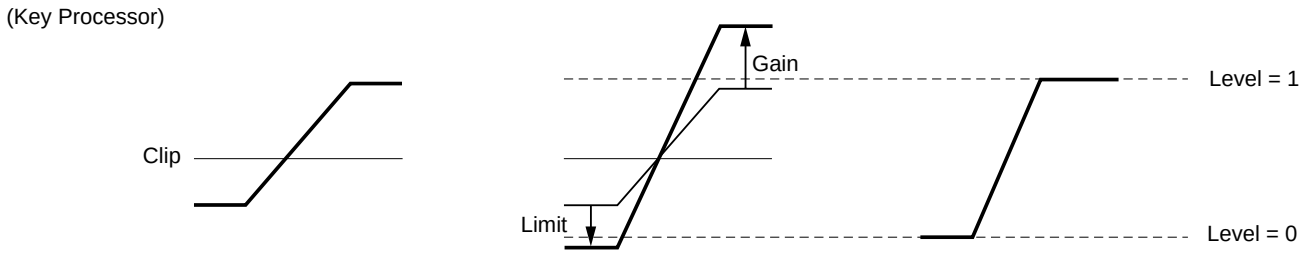
Conversion table from the Key Gain to the Volume.

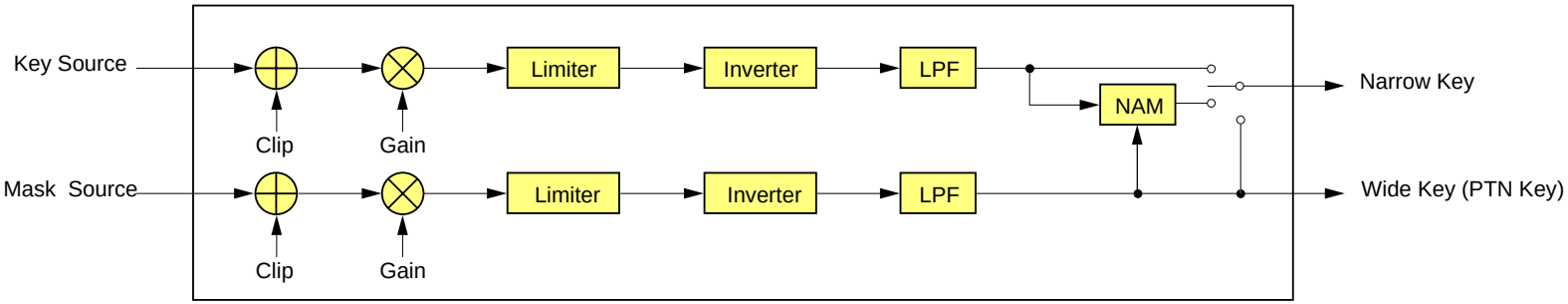
Volume / Gain	D2		D1	
	LUM KEY	LIN KEY	LUM KEY	LIN LEY
0.5	229	229	147	147
1.0	458 Default 460 = 1.0063	458 Default 460 = 1.0063	293 Default 300 = 1.0266	293 Default 300 = 1.0266
2.0	708	708	543	543
4.0	802	854	761	772
6.0	836	899	798	845
8.0	865	927	824	886
10.0	884	947	842	904
20.0	947	-	904	966
30.0	983	-	944	-
50.0	-	-	990	-

Note : *Default means the factory default setting of Sony. (around 1.0 gain)
**The Gain curve has non-linear characteristic. Therefore using above table, it is difficult to interpolate necessary volume. (ex. 9.0 gain is not located just a middle of 8.0 to 10.0 gain.)

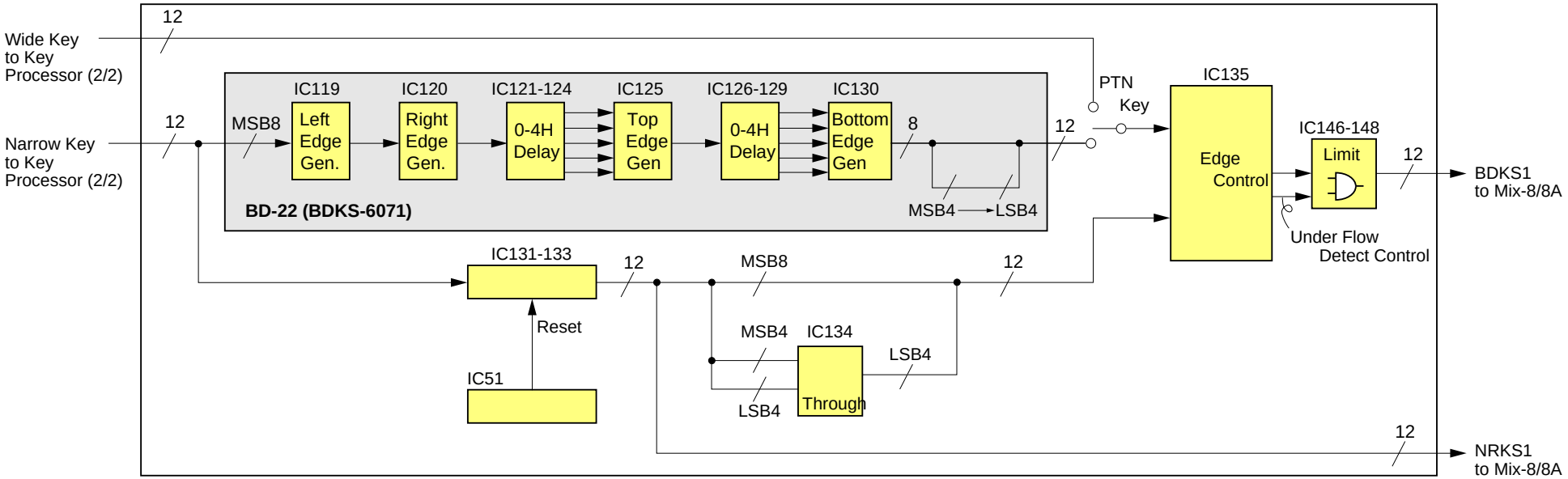
Key 1 Processor (1/2)



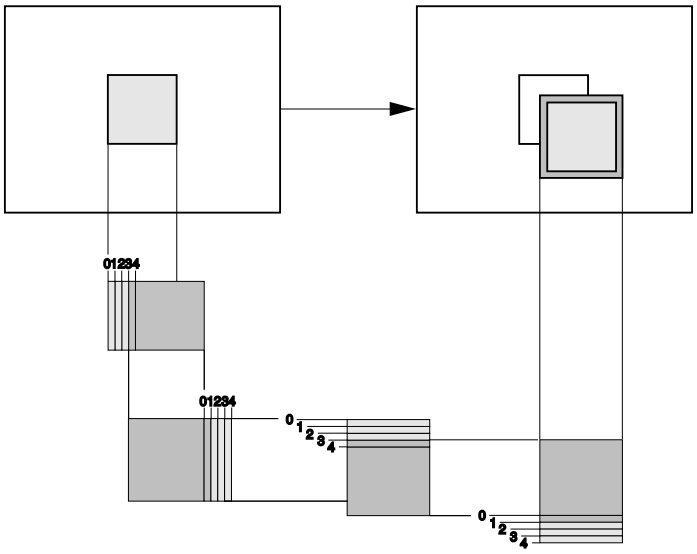




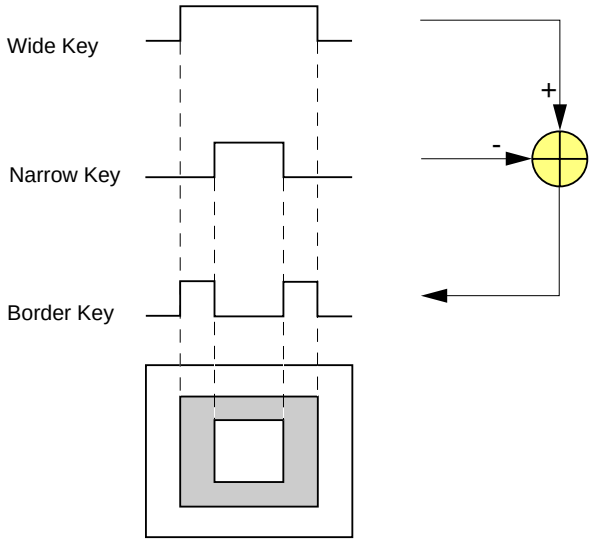
Key 1 Processor (2/2)



(Key Board Processor)



(Edge Control)



Downstream Keyer

KPC-9(A)

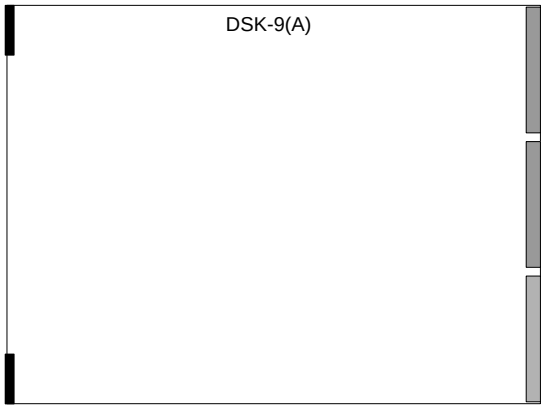
M/E Mixer

MIX-8(A)

MIX-8(A) KPC-9(A)
M/E Mixer *Downstream Keyer*

PDF Edition

DSK-9(A)



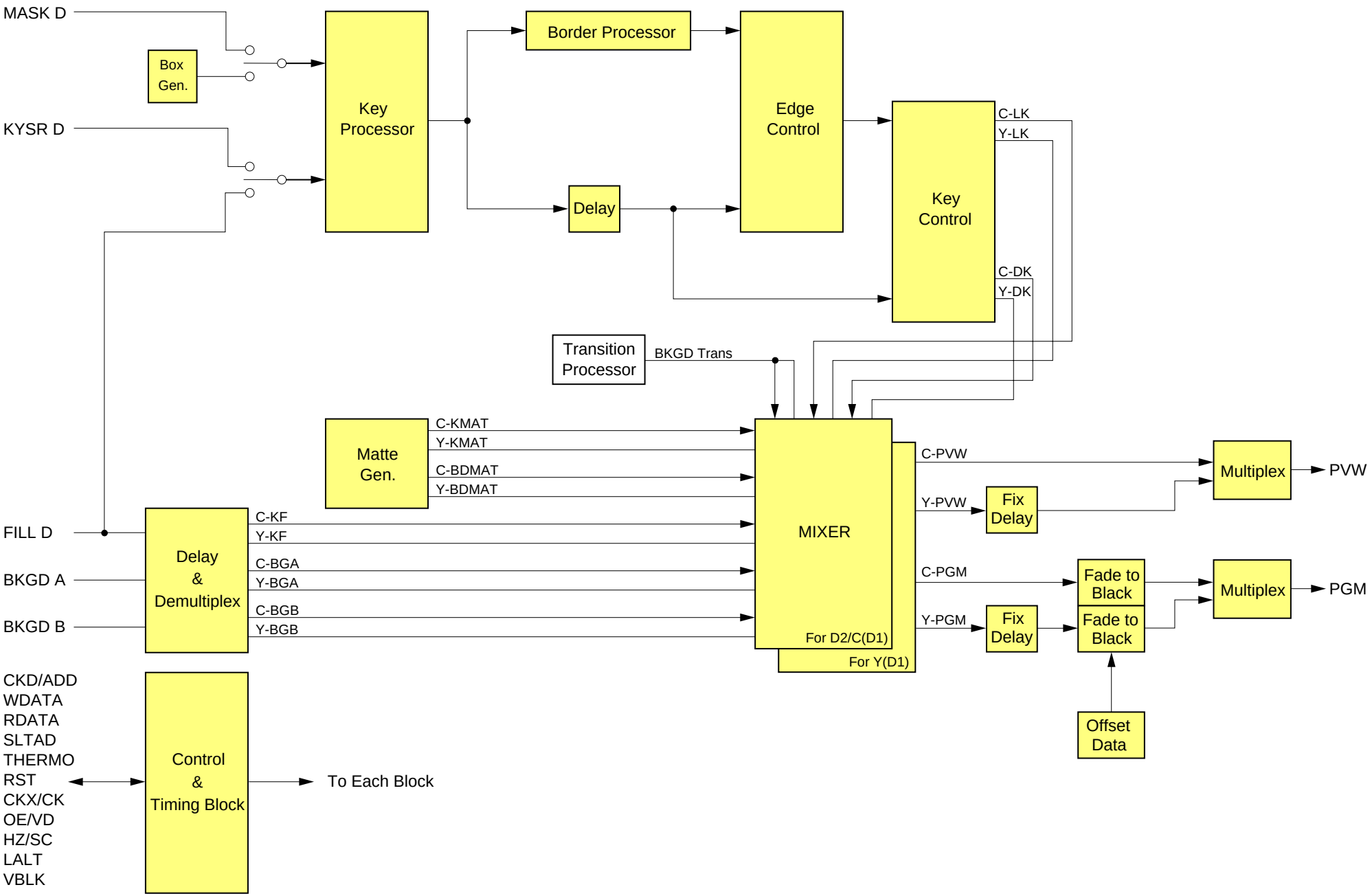
DSK-9(A) (Slot 9)

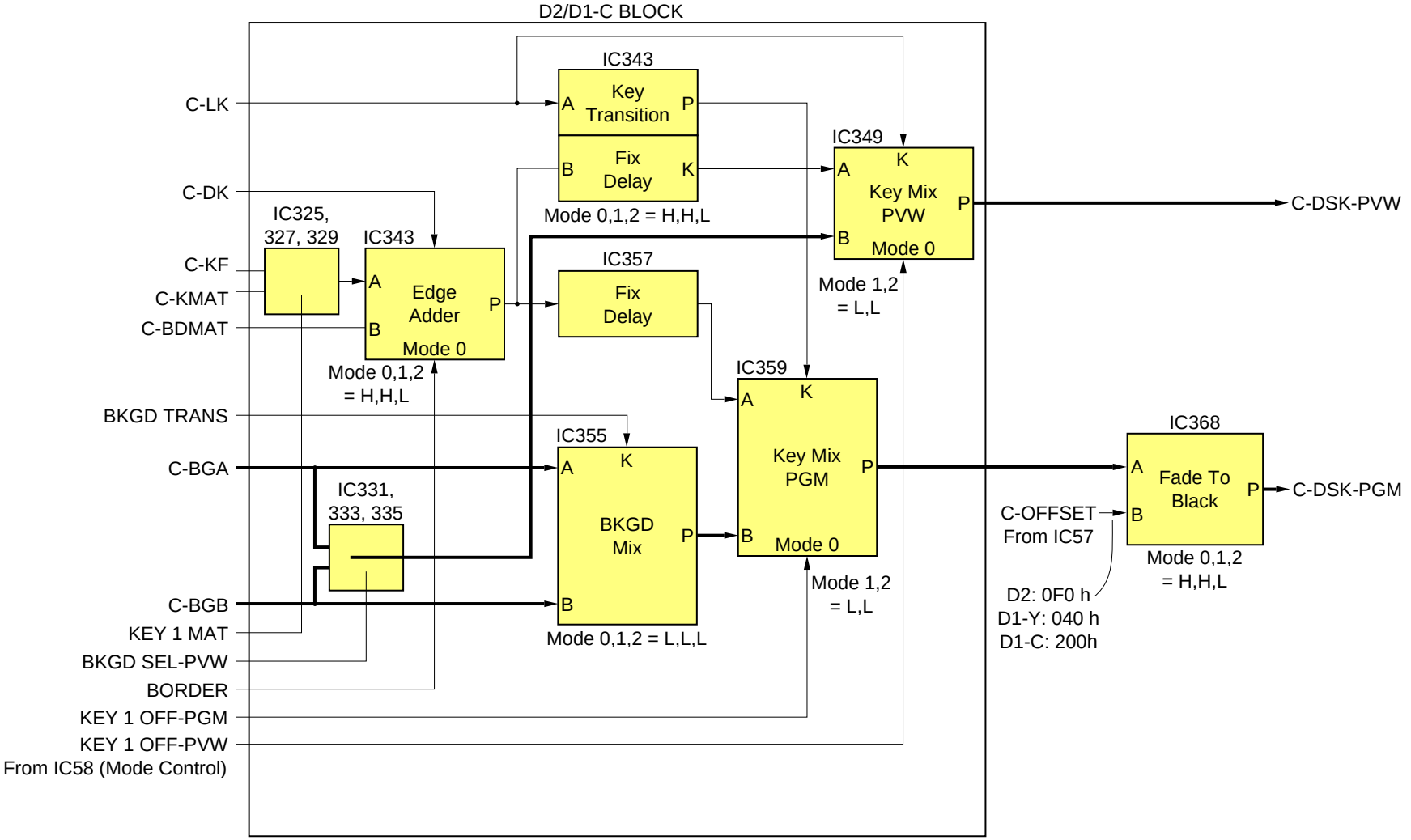
Selection of M/E 1 or M/E 2 output is made with the background mixing (Crossfade) function or CUT of the DSK-9(A) board.
Video inputs are labelled “Background A and Background B” in some diagrams due to functional similarity with MIX-6(A) board of DVS-8000(C), where the sources are from the Preset / Programme bank - In the case of the DVS-6000C, these sources are hard wired from the outputs of the MIX-8(A) boards.

Transition times for Background Crossfade, downstream Key, and Fade to black are independant. No wipe transition is available.

DSK sources are from the DSK fill and source busses, but with a limited choice of 10 buttons assignable to any available source

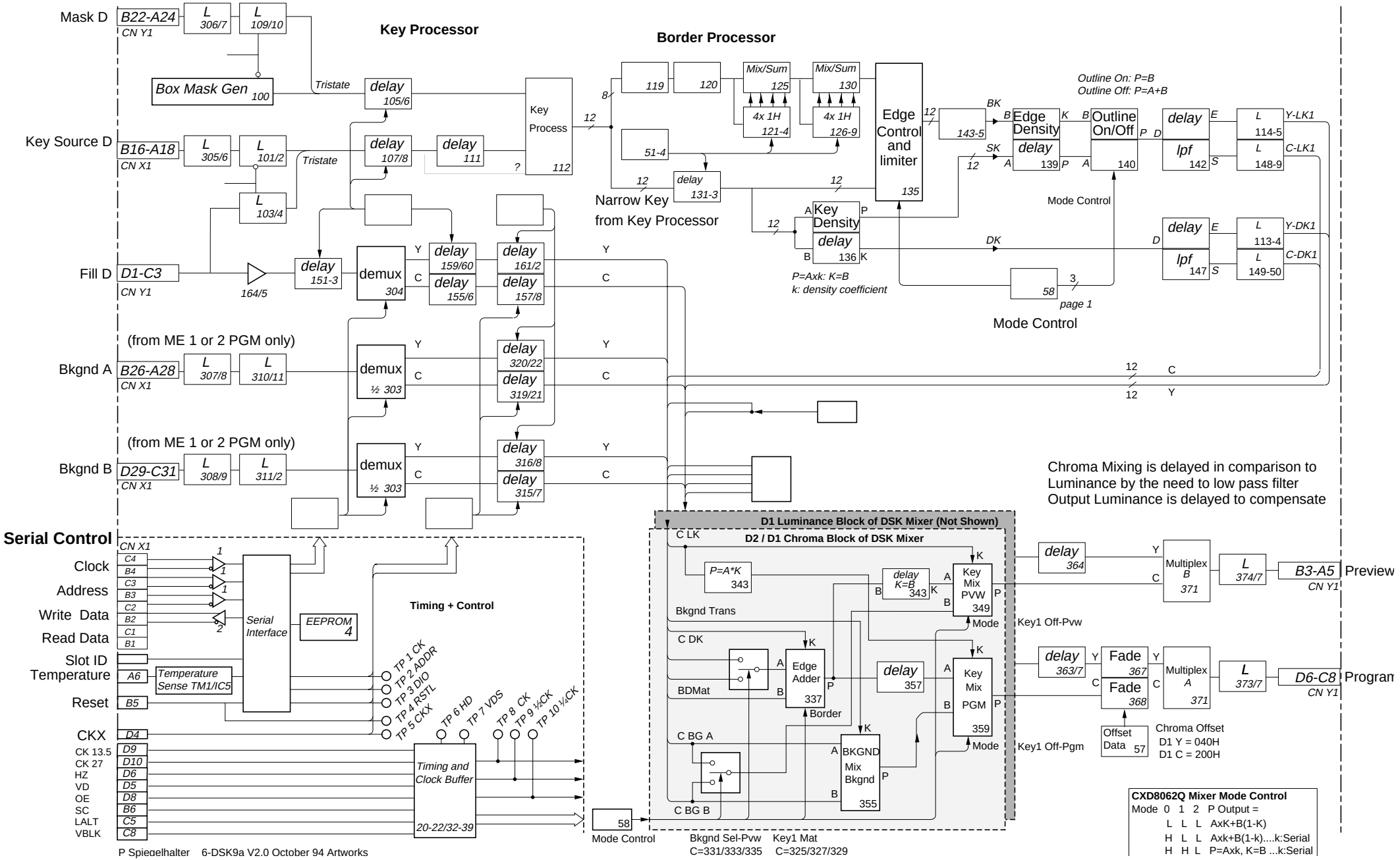
DSK Mask Process:	Clip, Gain, Box Generator / Mask Bus
DSK Key Process:	Clip, Gain, Invert
Transition process:	Auto transition “Fader” process
Key Control:	On/Off, Density
Key Edge:	Type, On/Off, Density
Mixing:	Cascaded Crossfade Mixers - Background, DSK, Fade to Black Provides a Clean output from 1st stage
Matte generation:	2 flat matte generators - DSK Fill and DSK Edge
Fade to Black:	Programme output, May be disabled
Safe Area Generator:	Programme Output Only (Preview Safe Title is on *Edit* Preview SD-30 / DA-72)


MASK D
Box Gen.
KYSR D
Key Processor
Border Processor
Delay
Edge Control
Key Control
C-LK
Y-LK
C-DK
Y-DK
Transition Processor
BKGD Trans
Matte Gen.
C-KMAT
Y-KMAT
C-BDMAT
Y-BDMAT
FILL D
BKGD A
BKGD B
Delay & Demultiplex
C-KF
Y-KF
C-BGA
Y-BGA
C-BGB
Y-BGB
MIXER
For D2/C(D1)
For Y(D1)
C-PVW
Y-PVW
Fix Delay
Multiplex
PVW
C-PGM
Y-PGM
Fade to Black
Fade to Black
Fix Delay
Multiplex
PGM
Offset Data
CKD/ADD
WDATA
RDATA
SLTAD
THERMO
RST
CKX/CK
OE/VD
HZ/SC
LALT
VBLK
Control & Timing Block
To Each Block

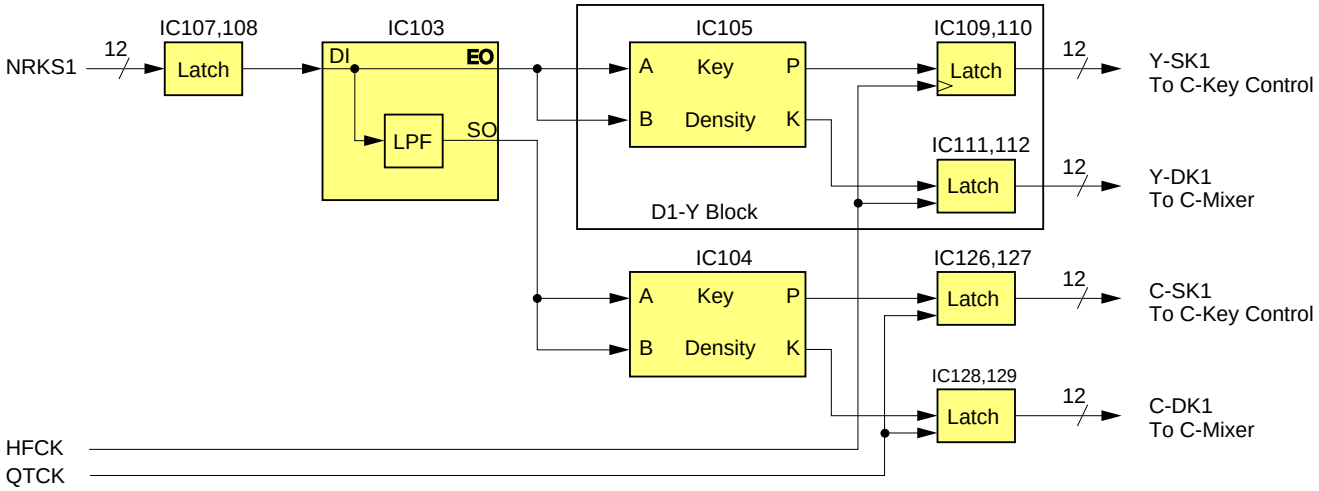


CXD8062Q
Mode 0,1,2 = L,L,L: P = A x K + B (1-K)
Mode 0,1,2 = H,L,L: P = A x k + B (1-k) - - - k: Serial
Mode 0,1,2 = H,H,L: P = A x k, K = B - - - k: Serial

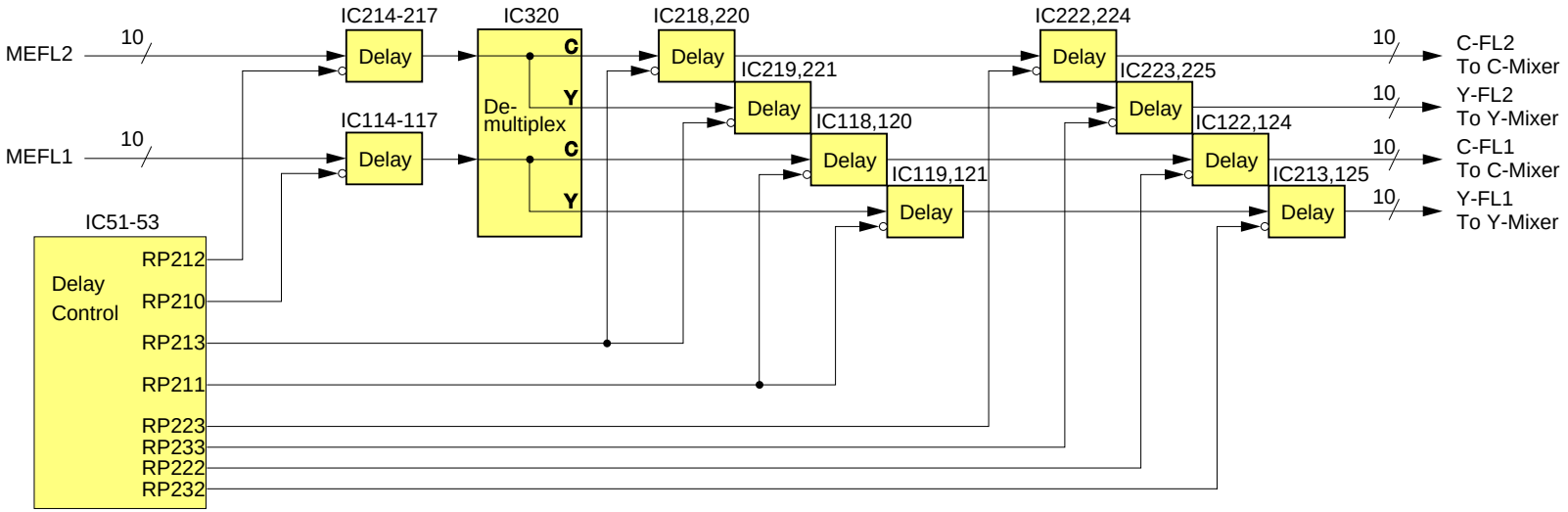
DSK-9(A) Down Stream Keyer

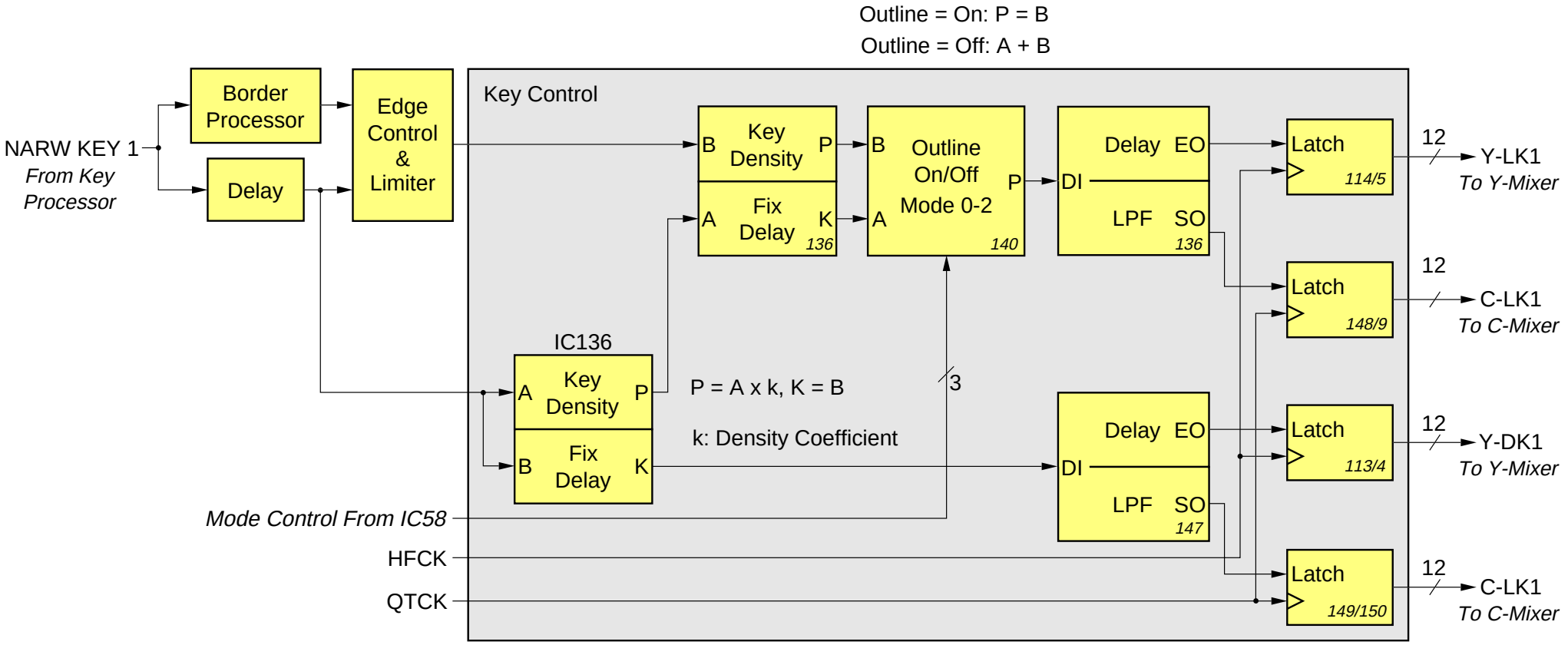


LPF and Key Density



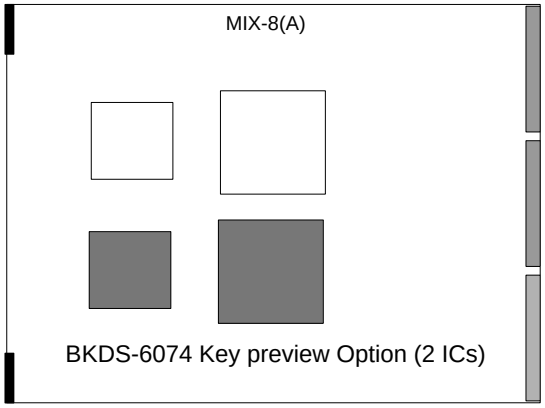
Delay and Demultiplex




Outline = On: P = B
Outline = Off: A + B
NARW KEY 1
From Key Processor
Border Processor
Delay
Edge Control & Limiter
Key Control
B Key Density P
A Fix Delay K
136
B Outline On/Off Mode 0-2 P
A
140
DI Delay EO
LPF SO
136
Latch
114/5
12
Y-LK1
To Y-Mixer
Latch
148/9
12
C-LK1
To C-Mixer
IC136
A Key Density P
B Fix Delay K
P = A x k, K = B
k: Density Coefficient
3
DI Delay EO
LPF SO
147
Latch
113/4
12
Y-DK1
To Y-Mixer
Mode Control From IC58
HFCK
QTCK
Latch
149/150
12
C-LK1
To C-Mixer

Key Control

MIX-8(A) M/E Mixer



MIX-8(A) Video mixing for M/E 1 (Slot 6) or M/E 2 (Slot 8)

Preview facility is an option, otherwise the board is functionally similar to the '8000's MIX-4A.

Transition Control:	Type, Mode, Wipe Border
Key Control:	On/Off, Density, Key priority (Over/Under)
Key edge:	Type, On/Off, Density
Mixer:	Mixing of Key - Edge - Background
Matte generatiors:	Key 1 fill, Key 1 edge, Key 2 fill, Key 2 edge, Wipe Border (5 matte generators, flat colour fill)

All video background, fill and key signals have come via the KPC-5 board.
When the "Next Transition" is set to Key only, the background B bus incoming to this board carries the same signal as the Background A bus, allowing the result of the next transition to be previewed correctly.

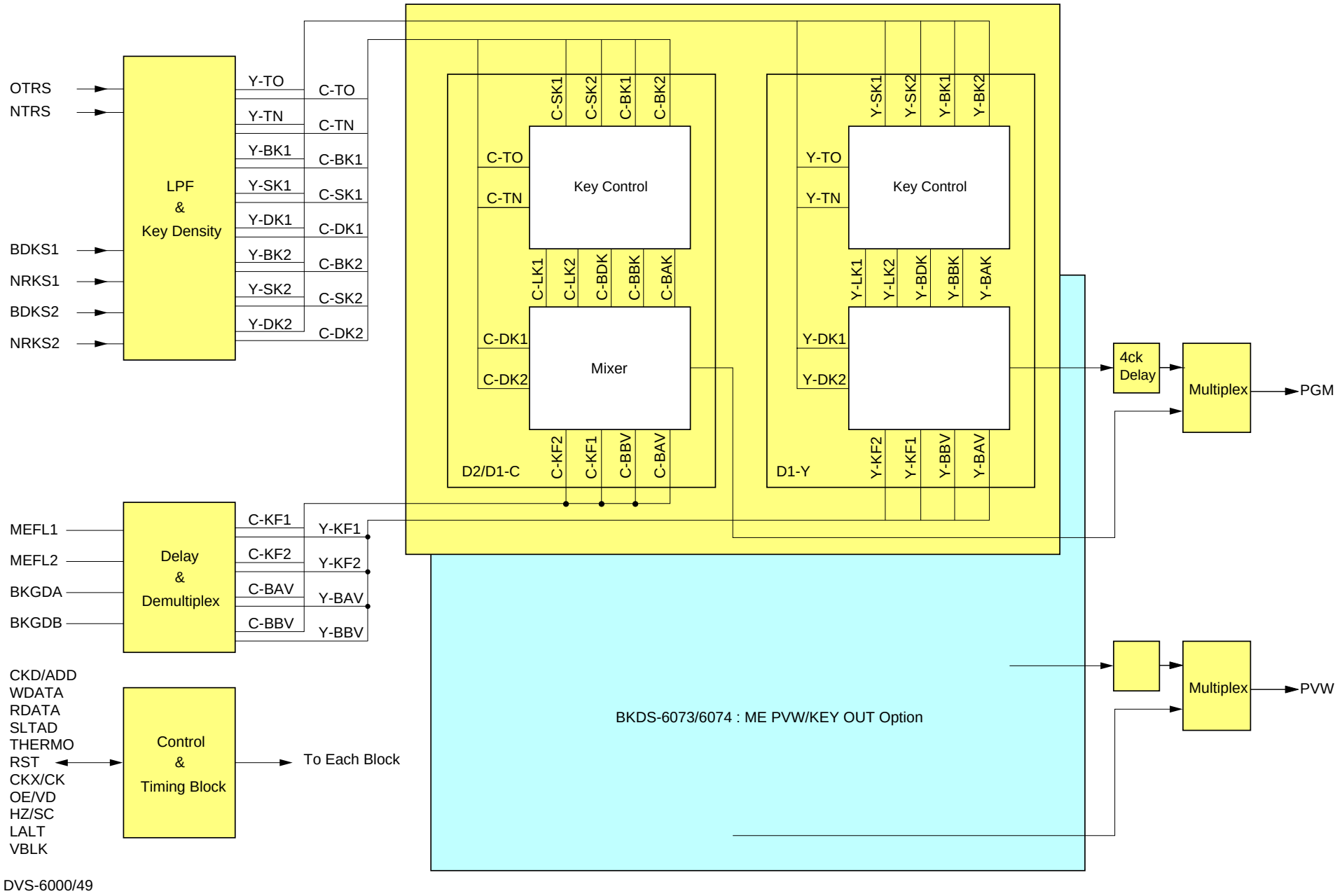
Mixing is achieved in a Parallel Mixing Stage, at 13.5MHz on separate Y and C paths.
For NTSC (D2) use, only the "Chroma" path ICs are mounted on a MIX-8 board.

"Preview" output (optional) may be changed to Key output by menu selection, allowing the M/E Key output to be output for recording via a suitable Aux Bus (using the Crosspoints located on the OUT-3 board).

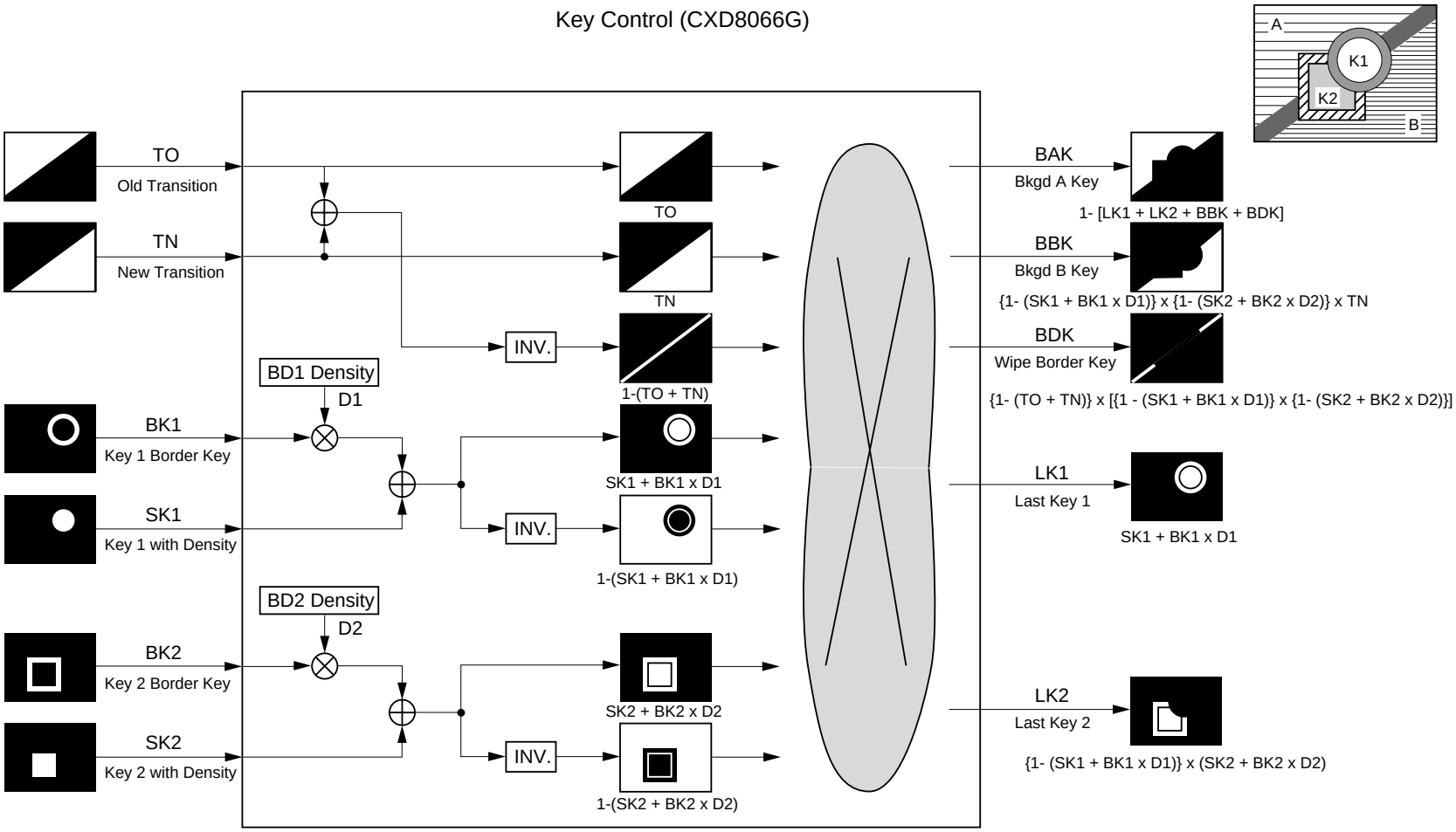
Re-entrant programme outputs are passed to the MAT-4 board for selection onto any bus.

The Programme output is also sent directly to the DSK-9(A) board "Background" bus inputs (M/E-1 = Background A, M/E-2 = Background B)

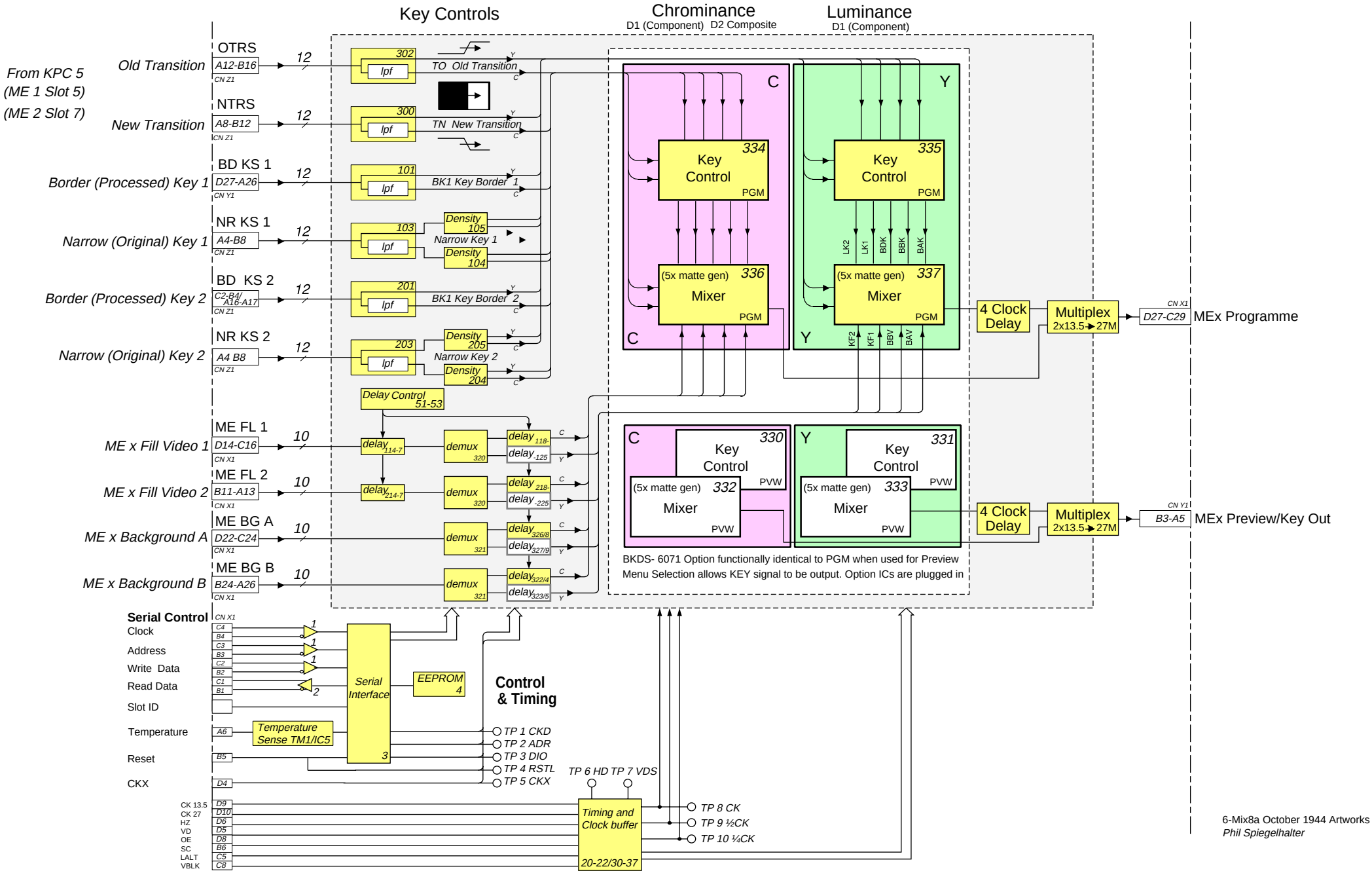
Mix-8/8A Board + BKDS-6071 (ME PVW/KEY OUT Option Kit)



Key Control (CXD8066G)



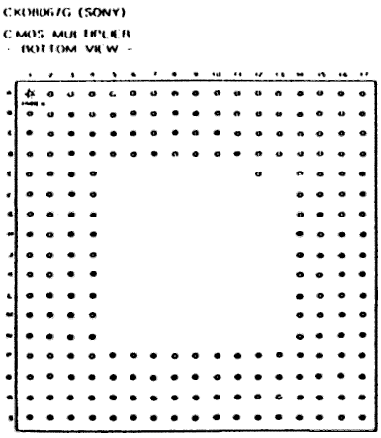
MIX-8(A) and ME Preview / Key Out Option (BKDS-6071)

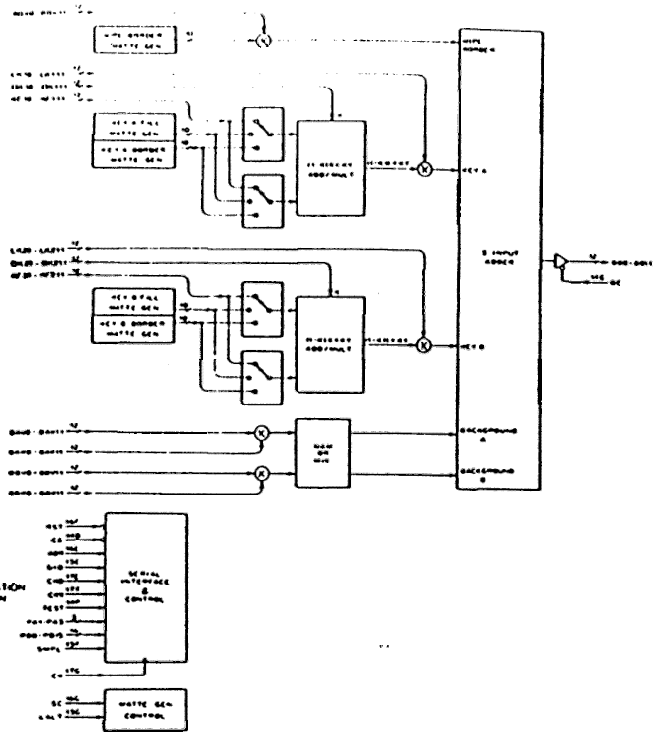


CXD8067Q Multiplier

MIX-4A *IC 332, 333, 336, 337*

MIX-6A ---

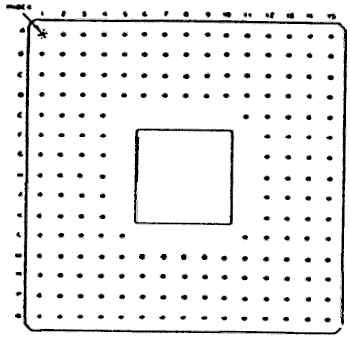


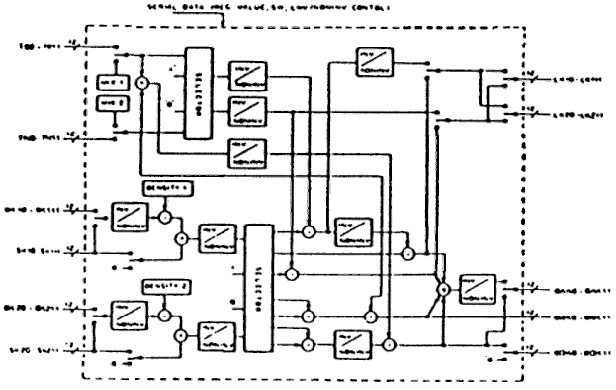


CXD8066G Key Control

MIX-4A *IC 330, 331, 334, 335*

MIX-6A *IC 307*





CXD8062Q Wipe Mixer

MIX-4A *IC 104,105, 204, 205*

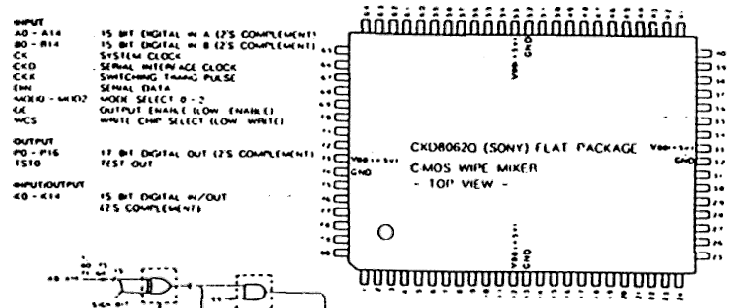
MIX-6A *IC 135-6, 337-8, 342-4, 349-56, 359-60, 367, 368*

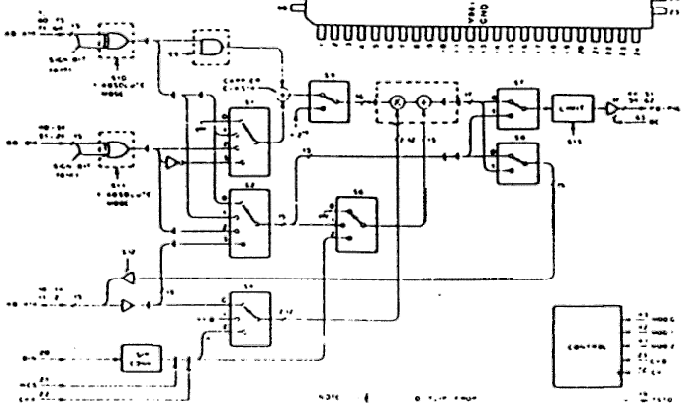
MAT-2 *110,120,122, 210, 220, 222*

KPC-1 *135*

WKG-5 *202, 306-7, 315, 435,436-7*

WKG-4 *104, 113, 114, 117, 138, 154-5, 163-4, 204, 213-4, 217, 238, 254-5, 263-4*





Output Carrier Board

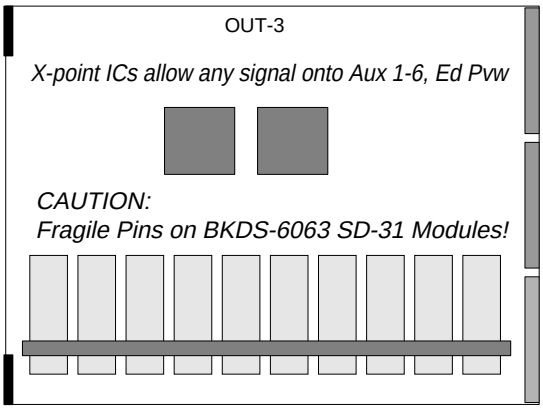
OUT-3 / SD-31 modules

Edit Preview Modules

SD-30 / DA-72

Output Carrier Board
OUT-3 / SD-31 modules
Edit Preview Modules
SD-30 / DA-72

OUT-3



Retaining Bar is used to remove modules

OUT-3 (Slot 10)

Acts as the carrier board for individual output modules.

Contains Serial control circuitry, its own identifying EEProm and EEprom selection to read the identifying EEproms on each module.

Crosspoint ICs allow Programme, Clean Output, M/E Preview /Key and viewable / recordable versions of the Chromakey KEY signals to be selected onto any Aux Bius or Edit Preview outputs.

The Edit Preview signal is passed in parallel form to the SG-211 board for the optional SD-30 / DA-72 edit Preview Outputs. (LE-118 is standard)

Safe Title circuitry is provided for the Programme Output (2x 13.5MHz Character generators) (Edit Preview Safe Title is located on the SD-30 / DA-72 board)

Each Output Module has 4 sdi outputs, but only the Programme position passes them through to external connectors; on the remaining boards, the unused outputs are terminated on the OUT-3 board.

The ASSIGN Output (also called “Flex” output is sourced only from the OUT-3 Crosspoint ICs, and may be assigned by menu.

Aux / Edit Preview Selection

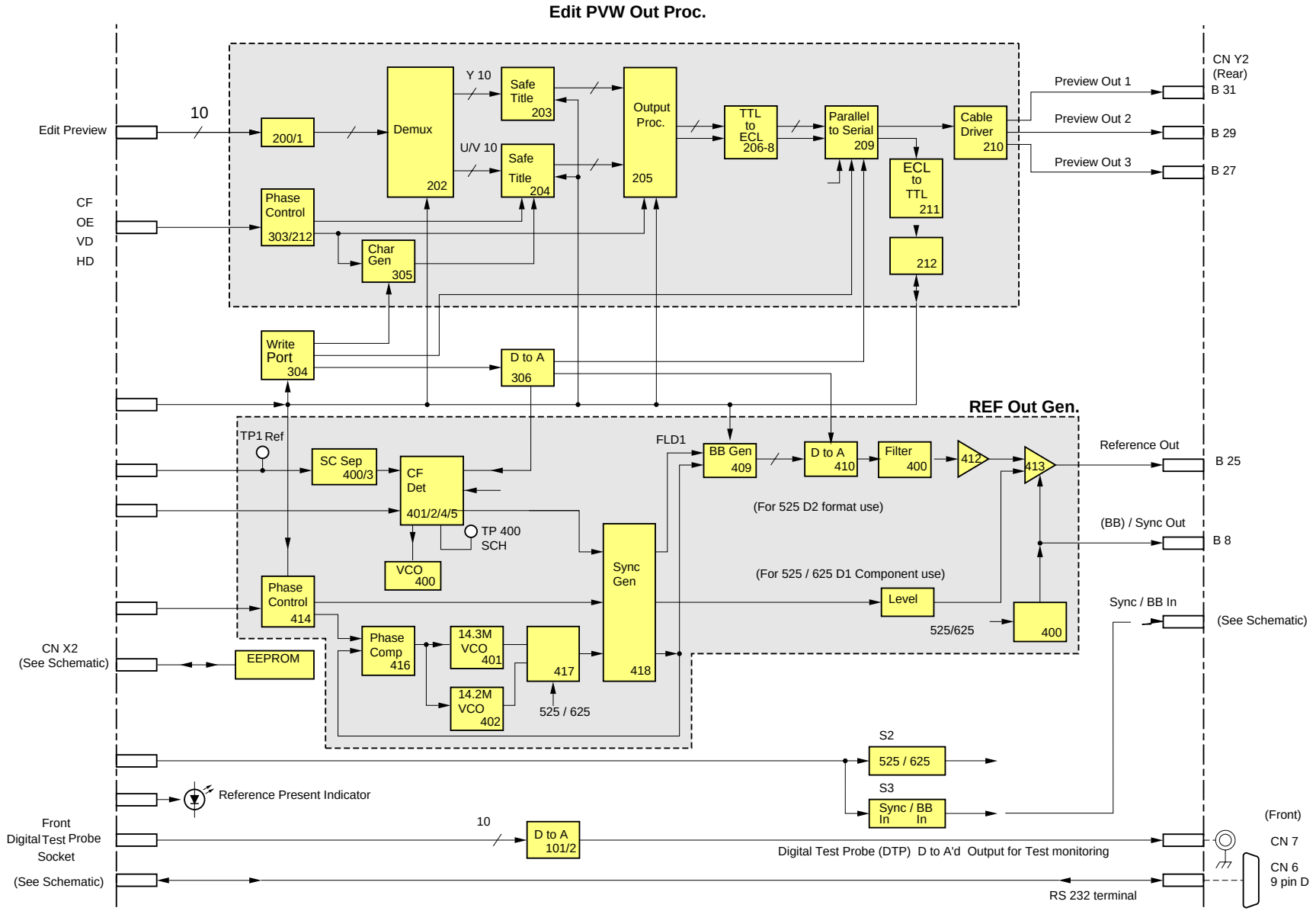
When sourced from the OUT-3 crosspoint ICs, the incoming signal from the Aux / Ed pvw bus is disabled at its tri-state latch at the board input. The Crosspoint IC tristate output is disabled when the Bus source is used.

Parallel buses from the OUT-3

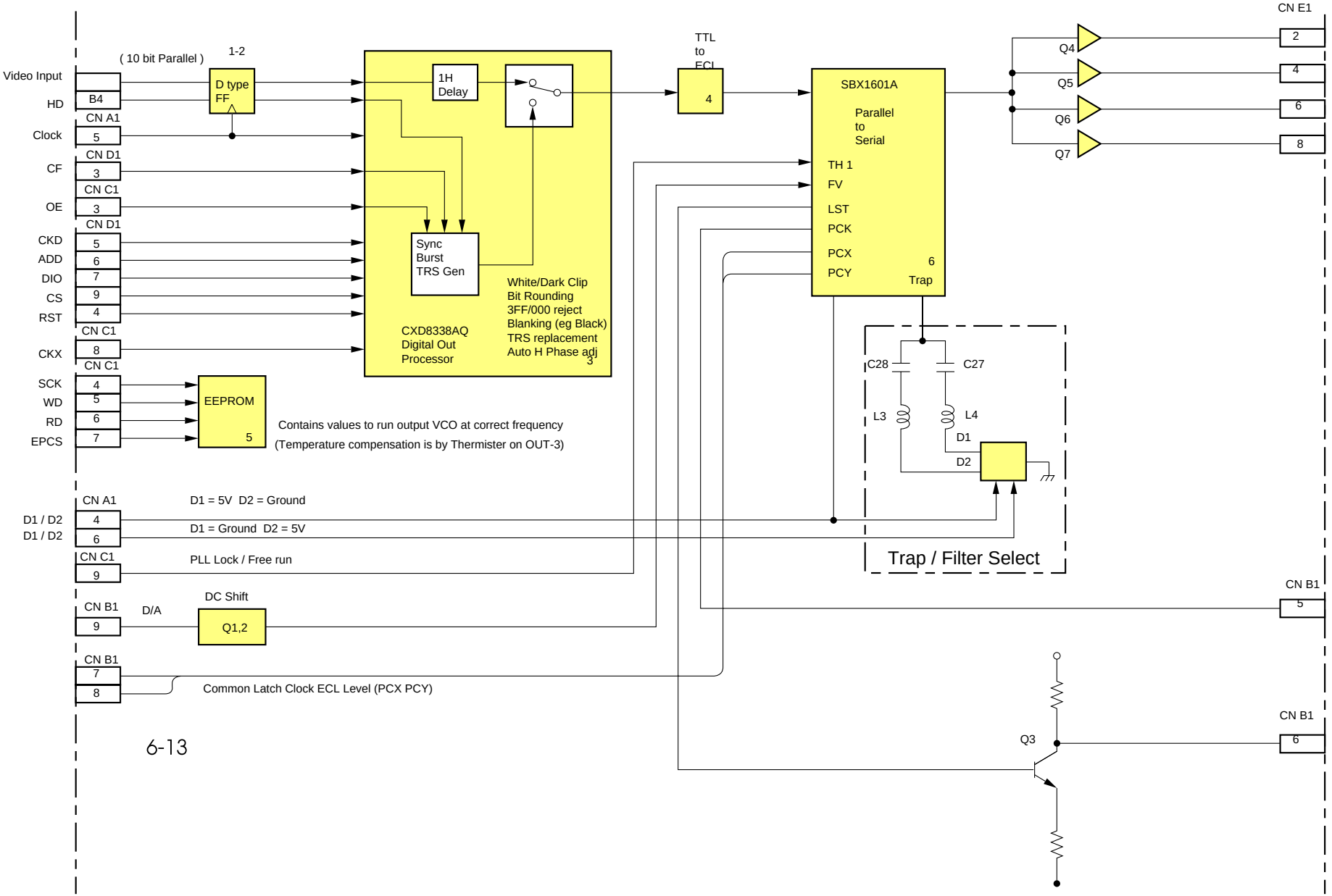
Aux 5 (and Aux 6) are sources to the BKDS-8041 / 6041 Frame Memory options.

For the BKDS-8041, Aux 5 can switch between two signals when the channels are “linked”.

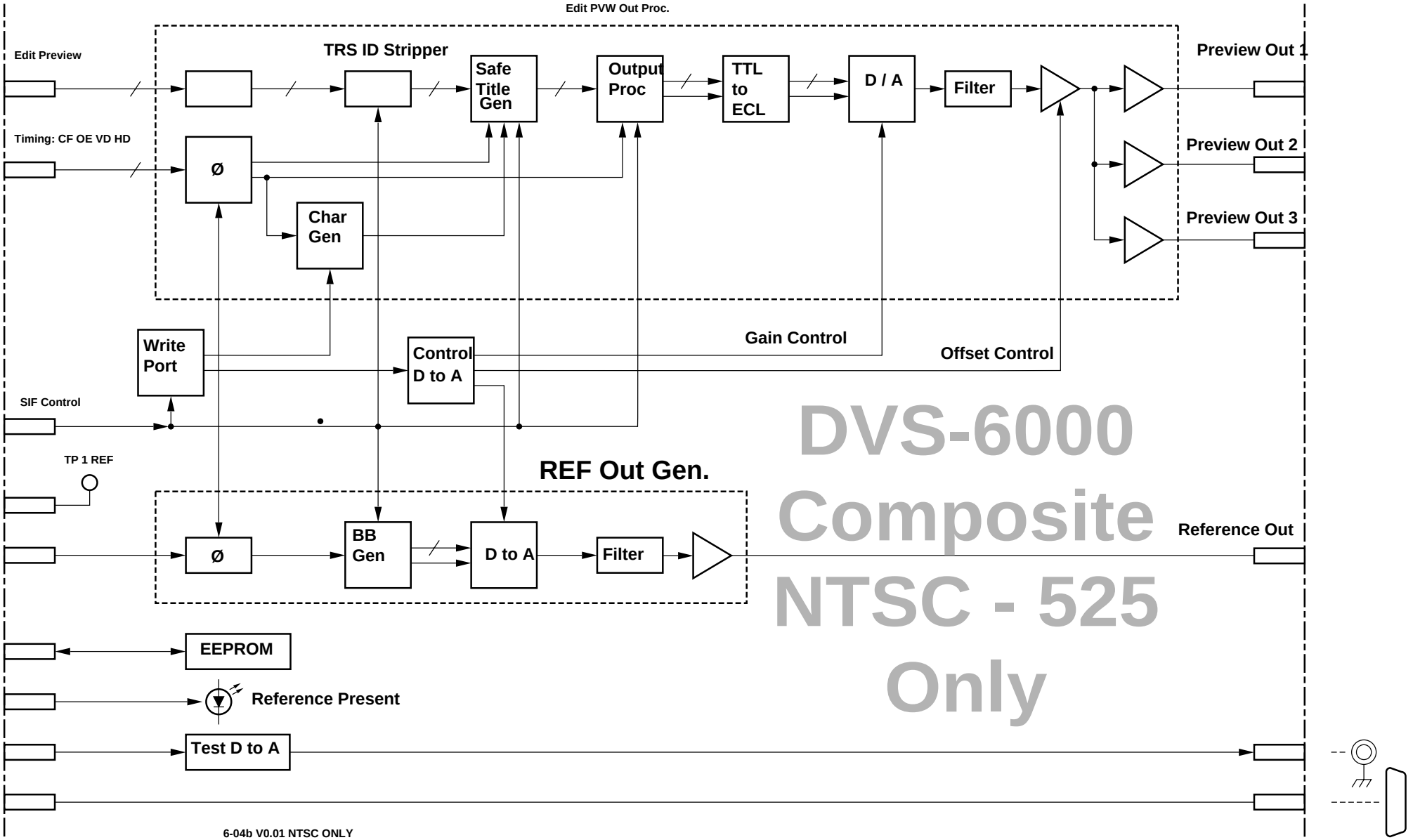
SD-30 Serial-Digital Edit Preview and Reference Out (BKDS-6060)



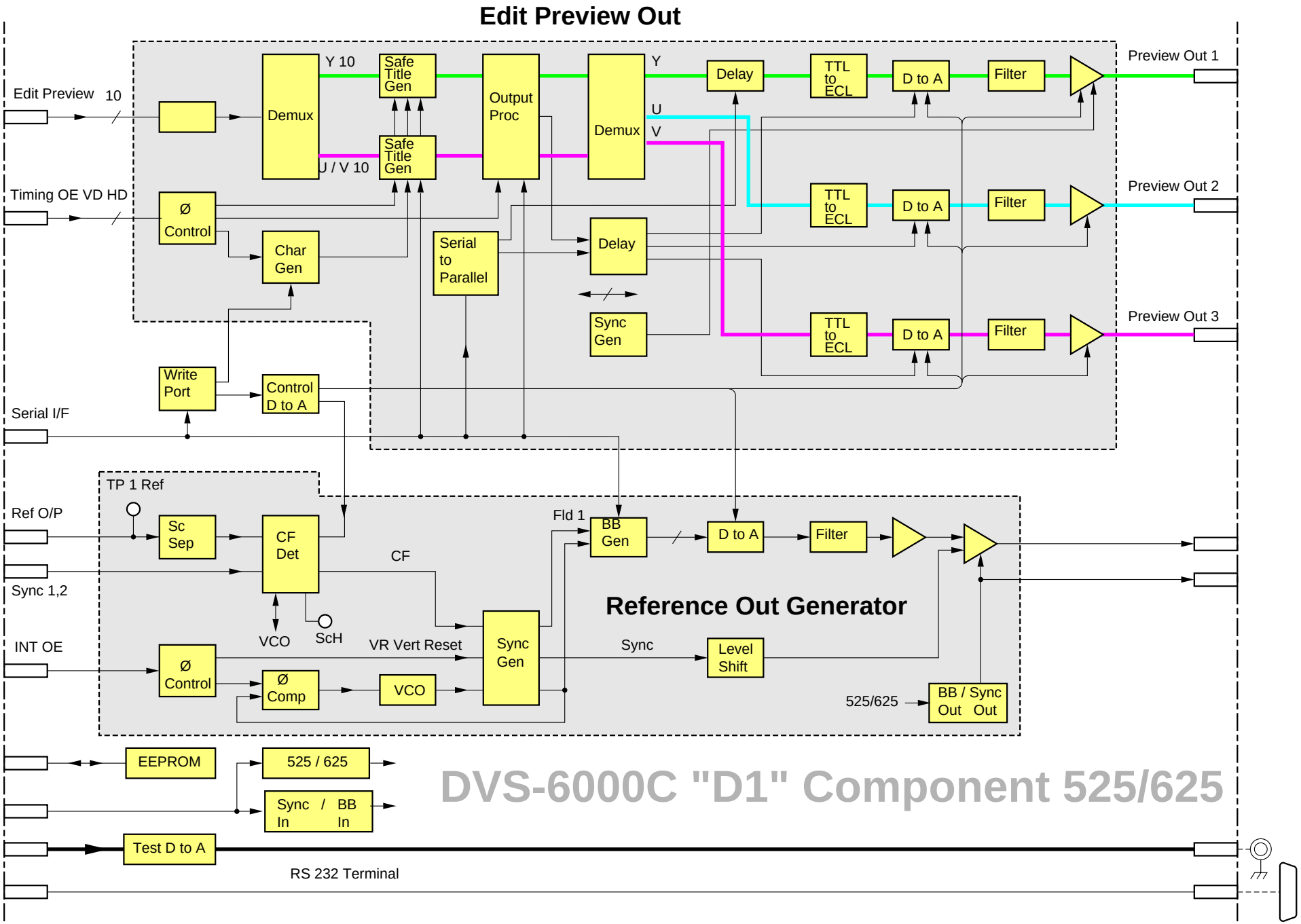
SD-31 (BKDS-6063) ; Output Modules located on OUT-3 Output Boards



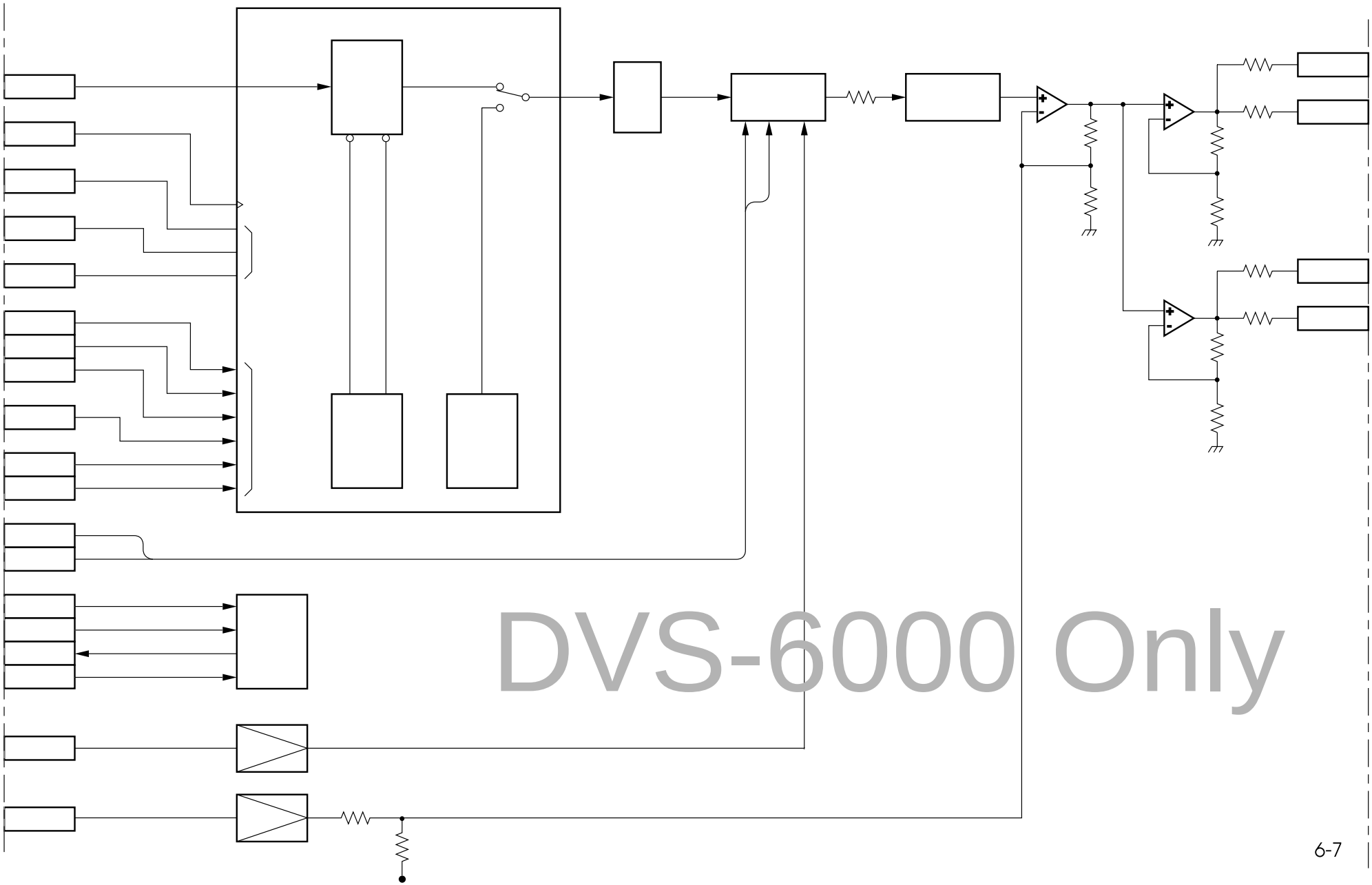
DA-71 Edit Preview with Analogue Composite Output (BKDS-6061) - NTSC Only



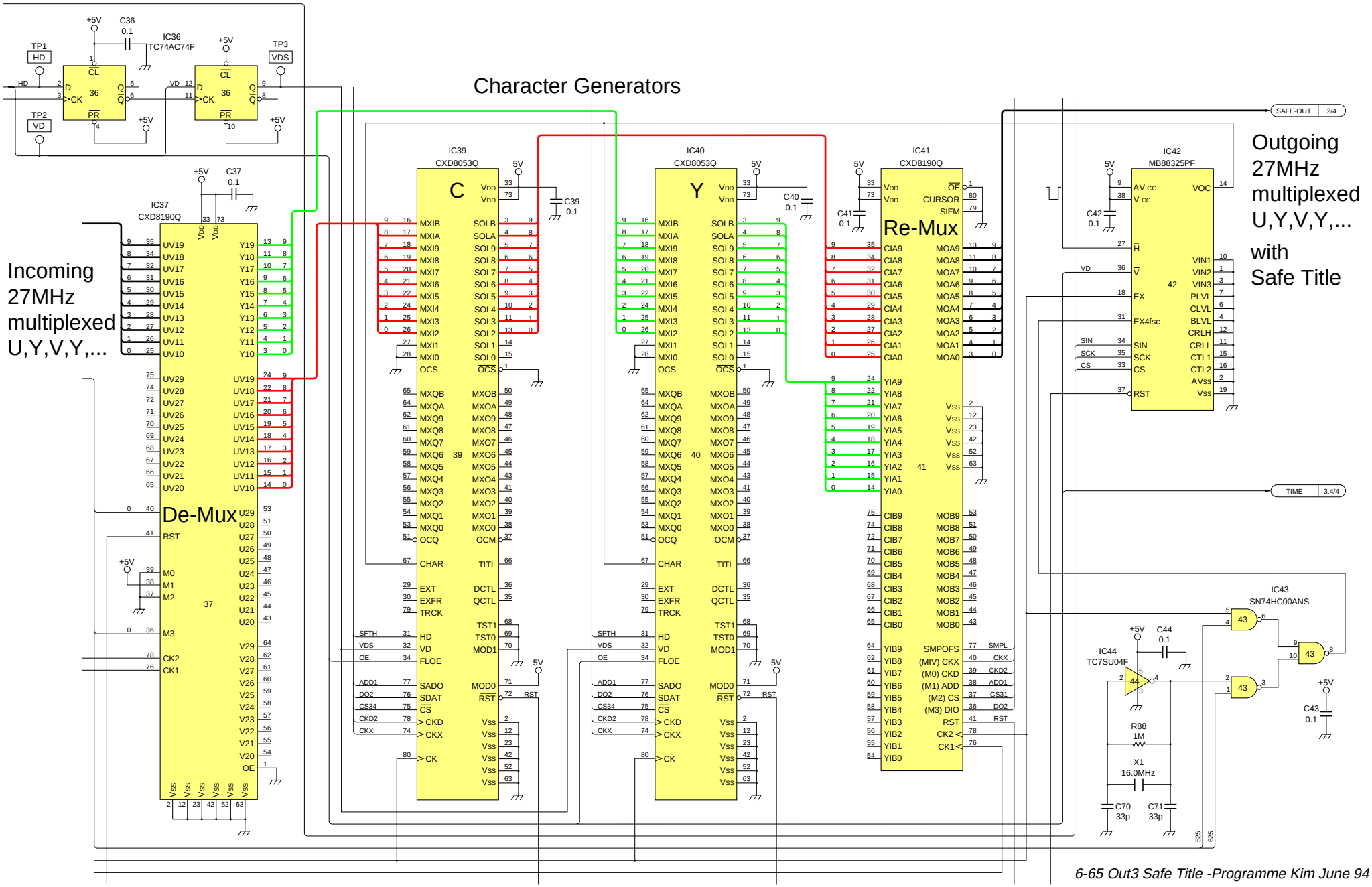
DA-72 Edit Preview Option with Analogue Component Output (BKDS-6062)



DA-73 (BKDS-6064) : Analogue Output Board Option



Out-3 Board Safe Title Superimpose on Programme Out



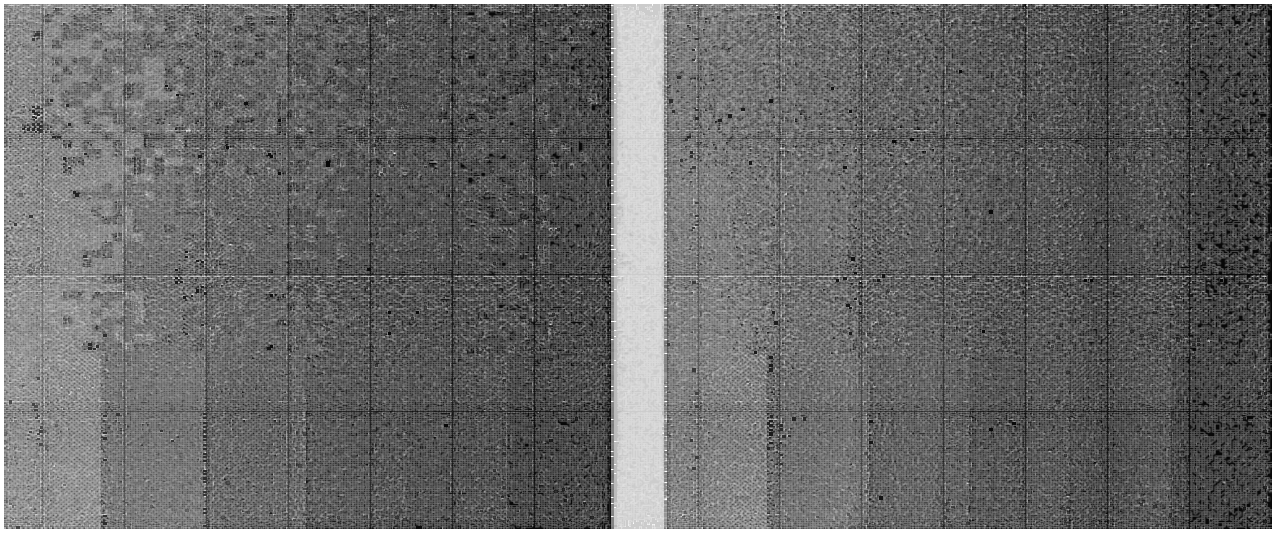
10 bit to 8 Bit Conversion:

The vision mixers accept 10 bit input and provide 10 bit output, with internal distribution as high as 14 bits, in order to maintain the maximum image quality.
However, many external devices may only be designed to handle 8 bit signals.

If no action is taken, a 10 bit signal would simply be truncated when reaching such a device. Depending on the picture content, this may be noticable, and therefore an objectionable degredation of the signal. This would be most apparent on a slowly rising ramp signal which was completely noise free (as in a colour background blend produced by a DVS / DME).

If, however, a small amplitude of “dither” signal is applied, before the signal is truncated, the degredation is camouflaged. This is demonstrated in the illustrations below:

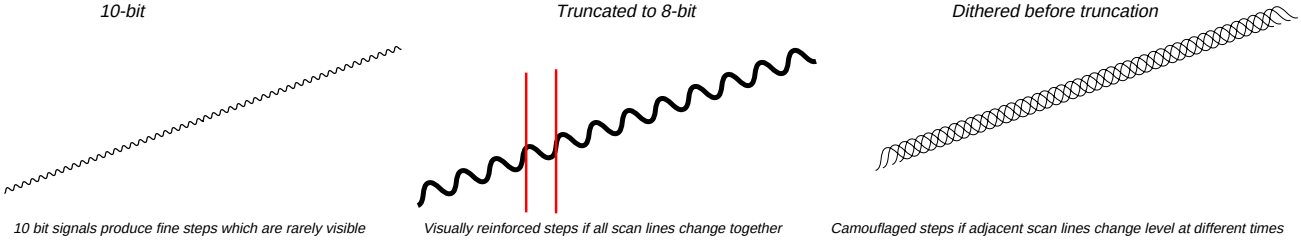
A grey scale step waveform, with 3 levels of dither added in each case



Large Visible Pixels More realistic, Small Pixels

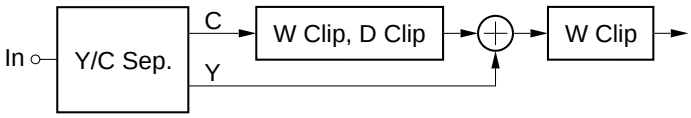
(Individual pixels should never be visible, if an appropriate sampling frequency is chosen!)

Three levels of dither are shown: Bottom: None, Middle ±0.5, Top ±1 level

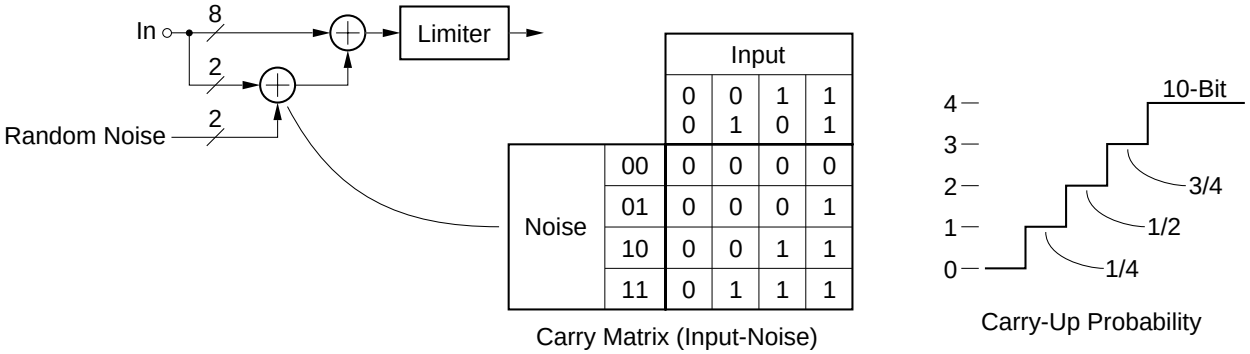


This rounding process is individually selectable on each individual hardware output.
A composite signal with “normal” levels of subcarrier, or a “noisy” signal inherently carries its own dither, and therefore would not benefit from this process.

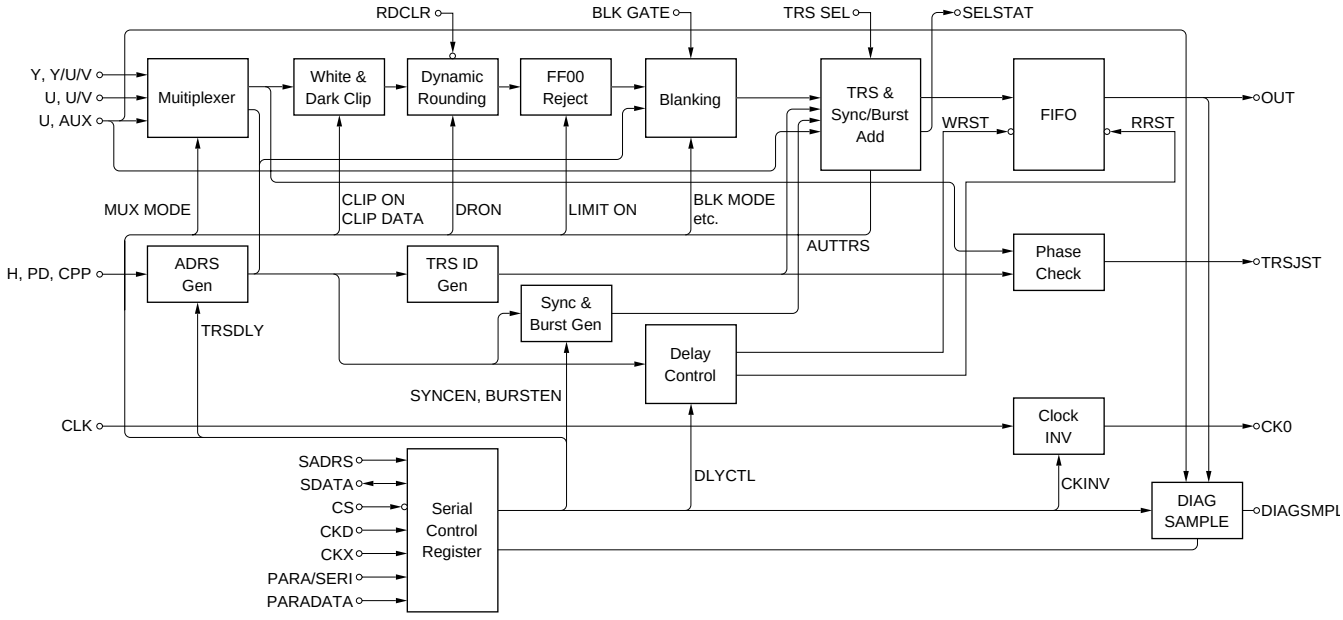
Bit Rounding on Digital Outputs



White Clip/Dark Clip Circuit



Bit Rounding Circuit



Sync Generator

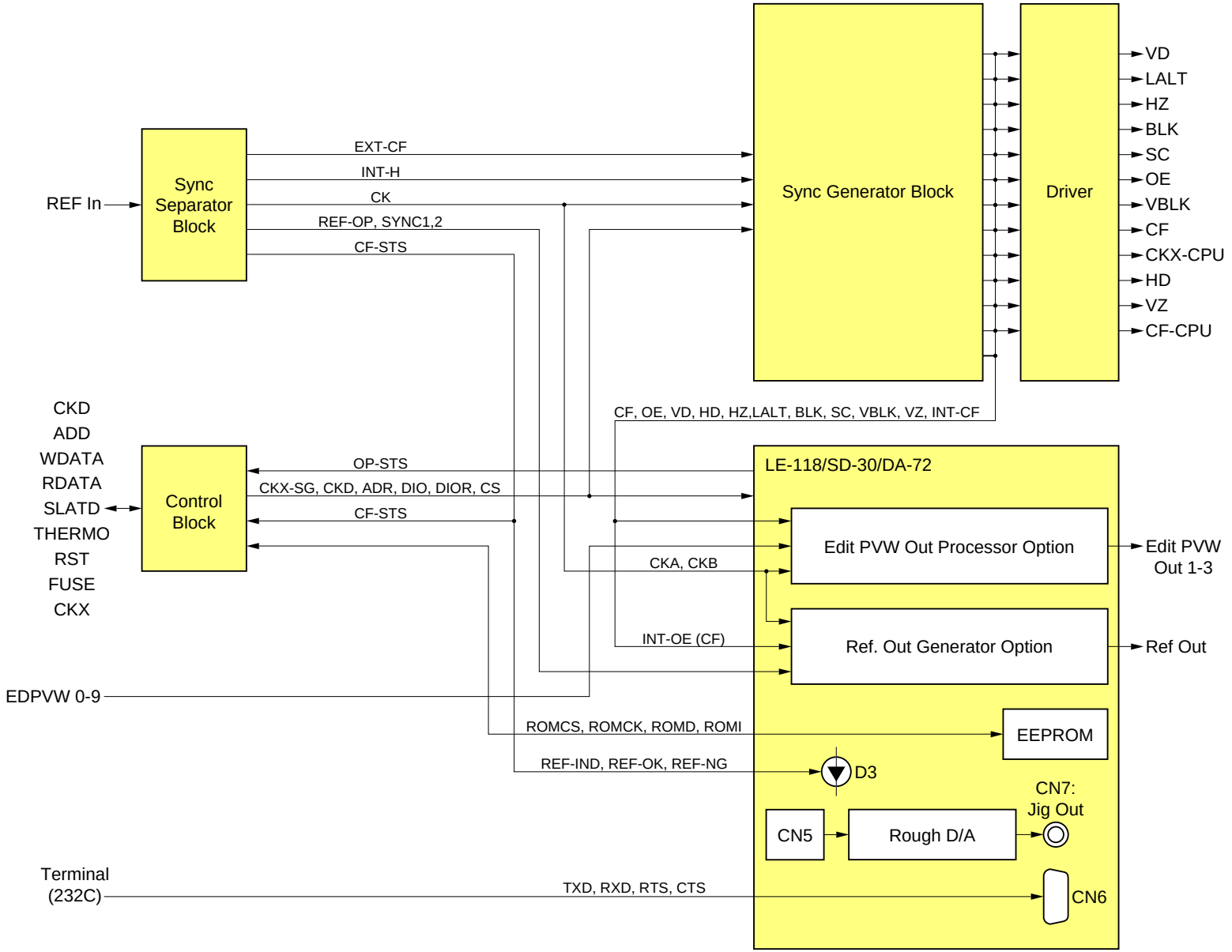
SG-211

(D1: 525 / 625)

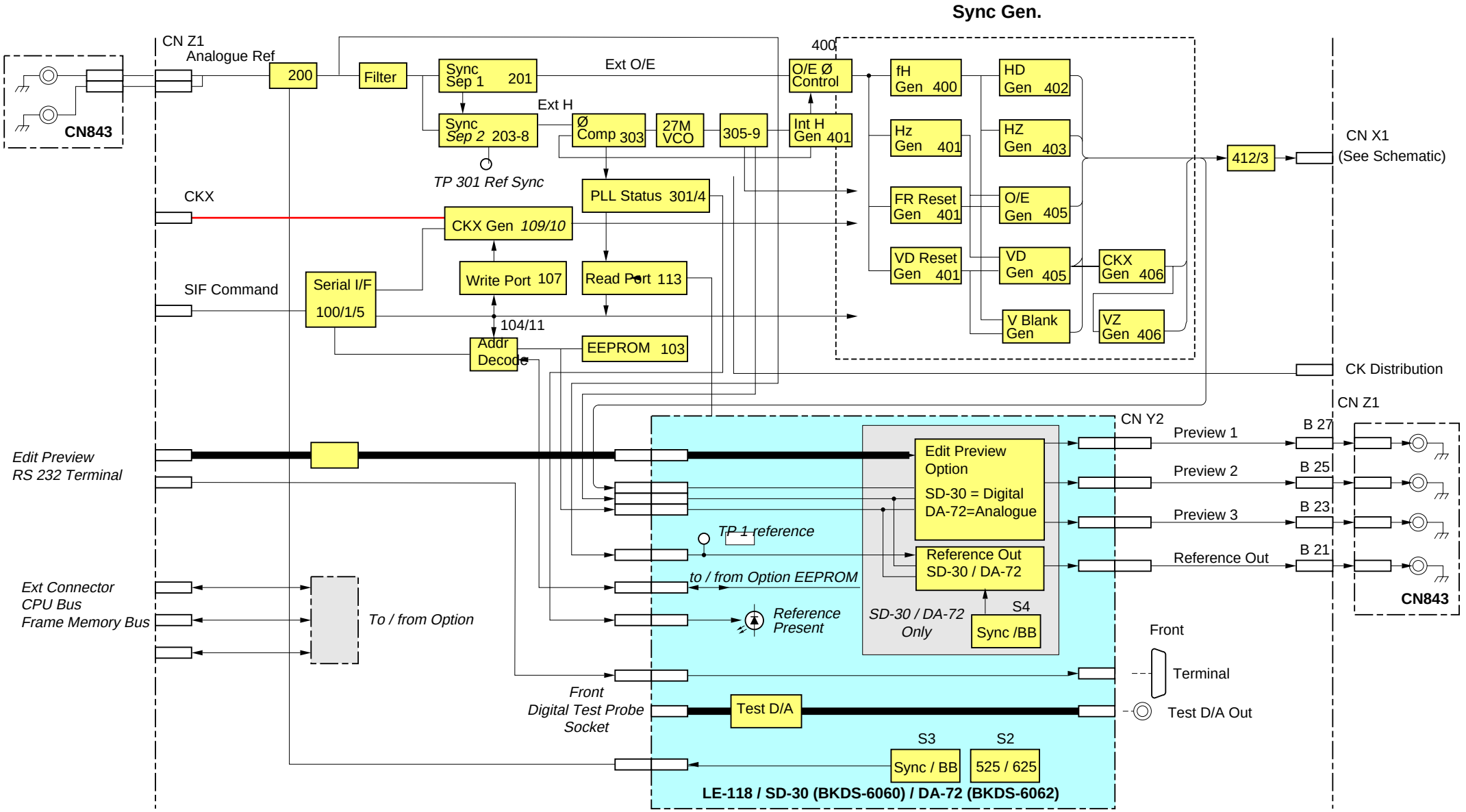
Sync Generator SG-211 (D1: 525 / 625)

PDF Edition

SG-211 + LE-118/Option (SD-30/DA-72)



SG-211 D-1 (Component) Sync Generator and LE-118 (Default) / SD-30 / DA-72 Options

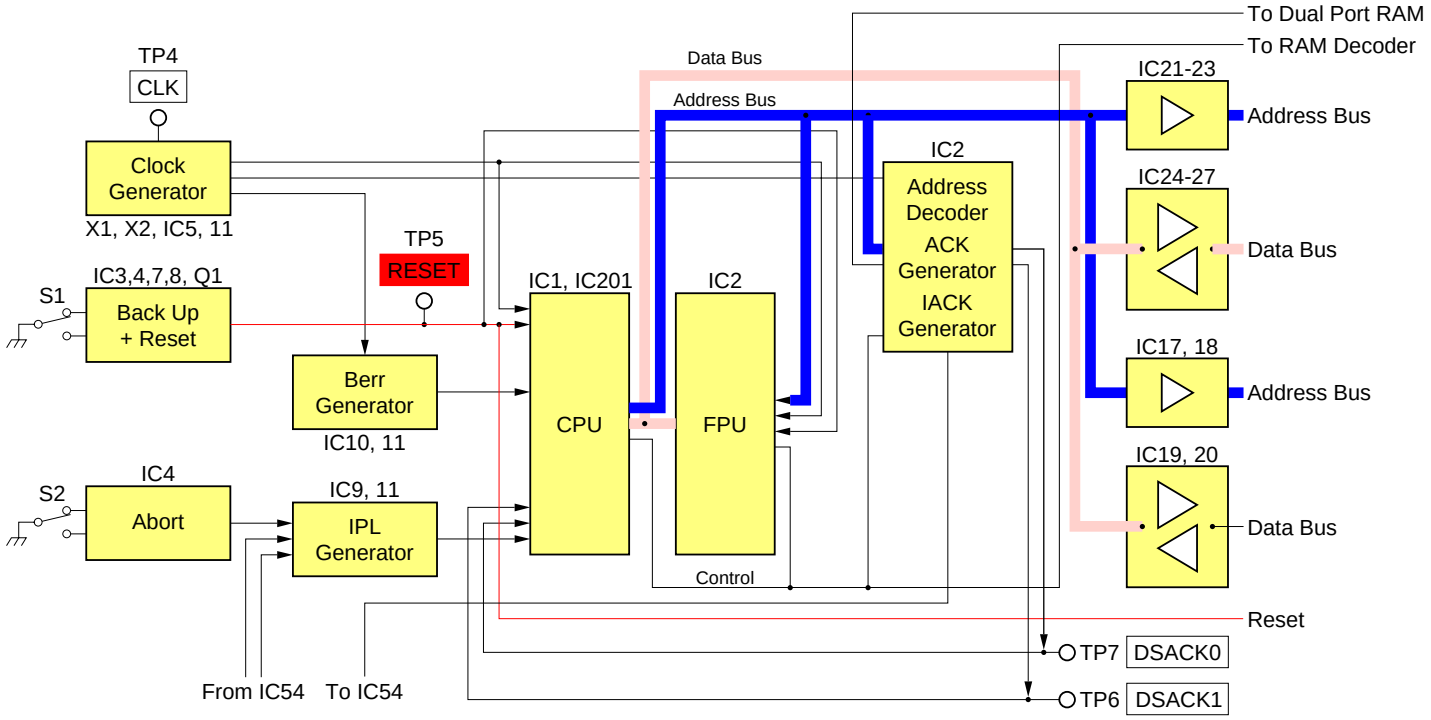


CPU - 147

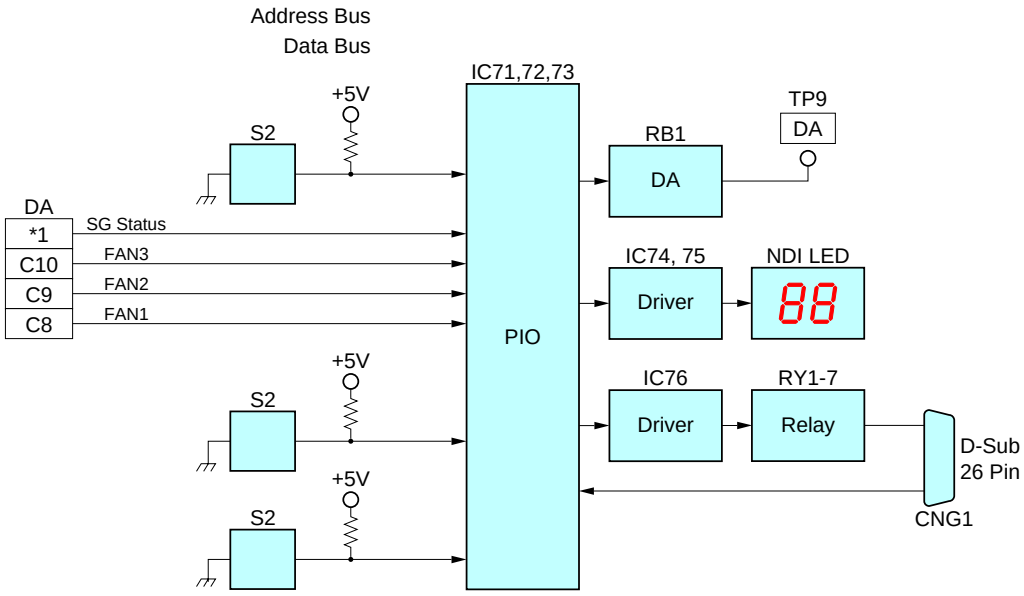
Control Processor

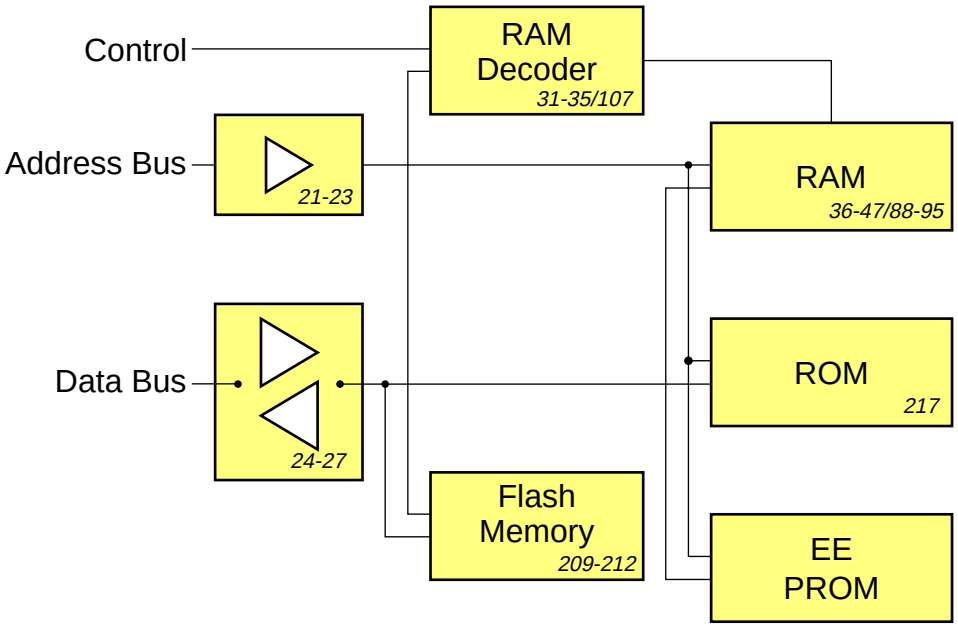
CPU - 147 Control Processor

PDF Edition

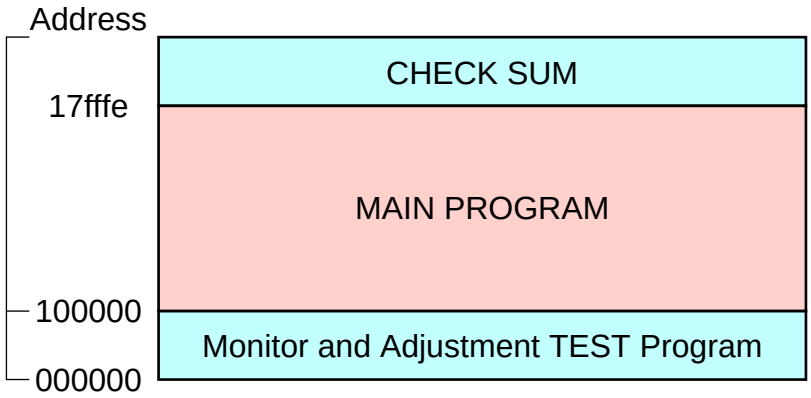

To Dual Port RAM
To RAM Decoder
TP4
CLK
Clock Generator
X1, X2, IC5, 11
Data Bus
Address Bus
IC21-23
Address Bus
IC2
Address Decoder
ACK Generator
IACK Generator
IC24-27
Data Bus
TP5
RESET
IC3,4,7,8, Q1
S1
Back Up + Reset
IC1, IC201
IC2
CPU
FPU
IC17, 18
Address Bus
Berr Generator
IC10, 11
IC19, 20
Data Bus
IC4
S2
Abort
IC9, 11
IPL Generator
Control
Reset
TP7
DSACK0
TP6
DSACK1
From IC54
To IC54

CPU Block


Address Bus
Data Bus
IC71,72,73
+5V
S2
TP9
DA
RB1
DA
DA
*1
C10
C9
C8
SG Status
FAN3
FAN2
FAN1
IC74, 75
NDI LED
Driver
88
PIO
+5V
S2
IC76
RY1-7
Driver
Relay
D-Sub 26 Pin
CNG1
+5V
S2



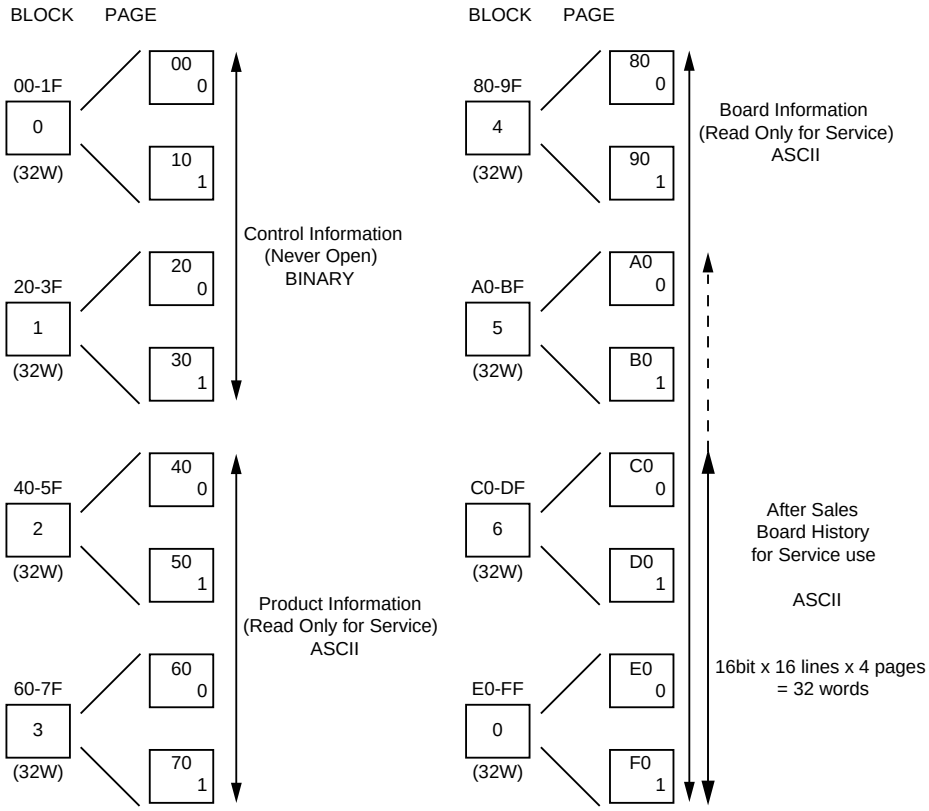
Memory Block



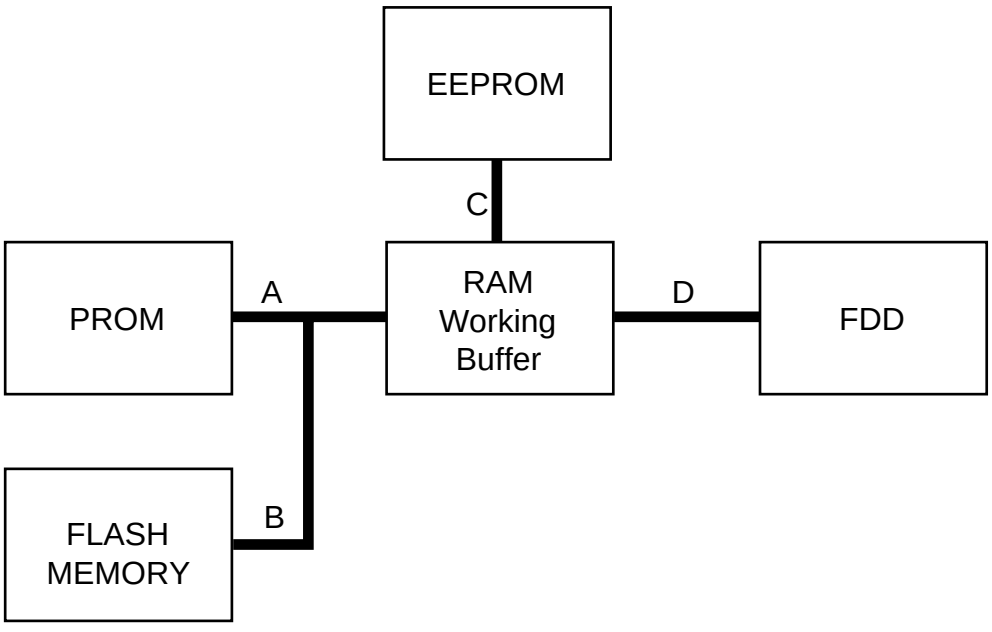
Flash Memory/ROM

Memory Maps

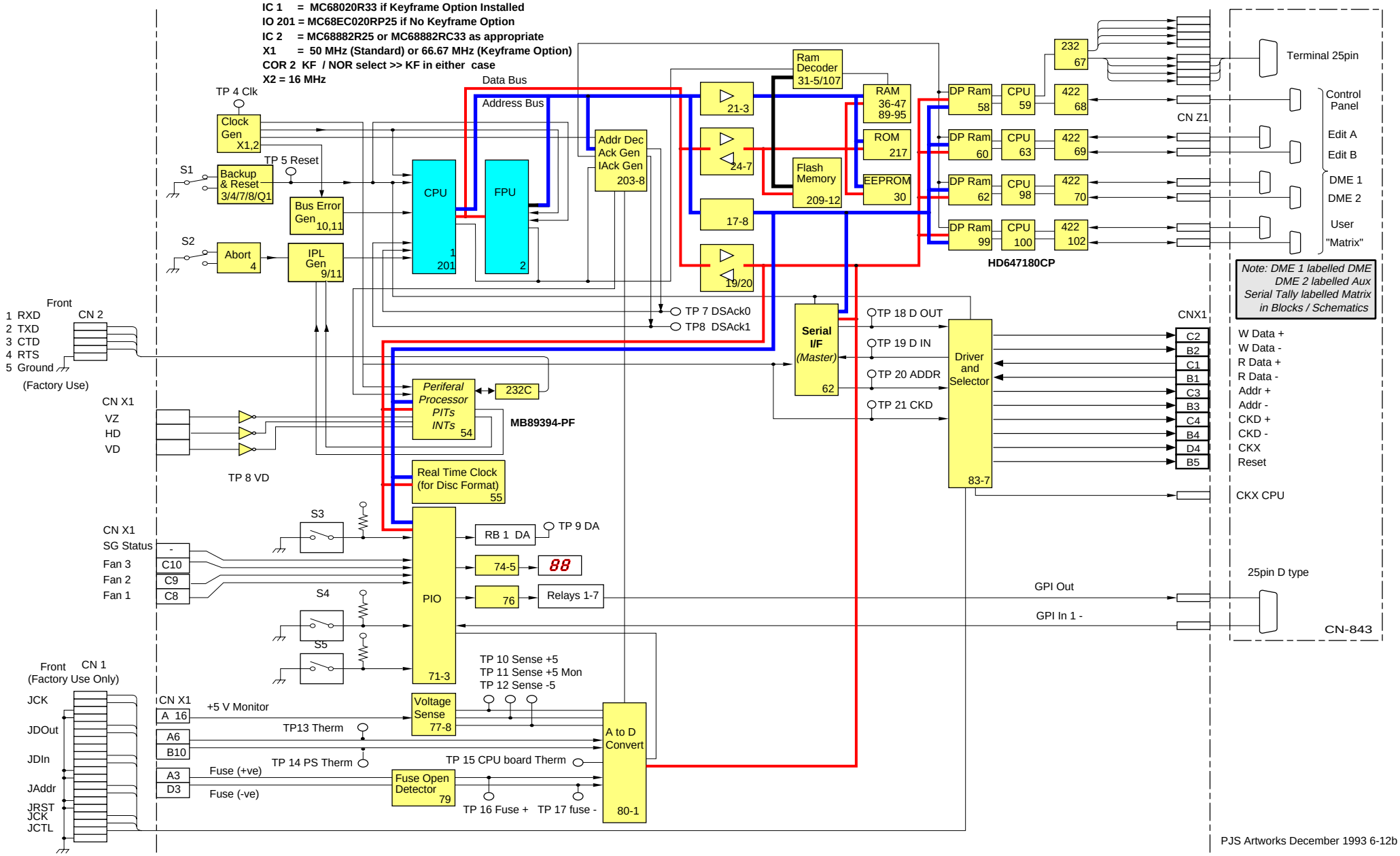
EEPROM

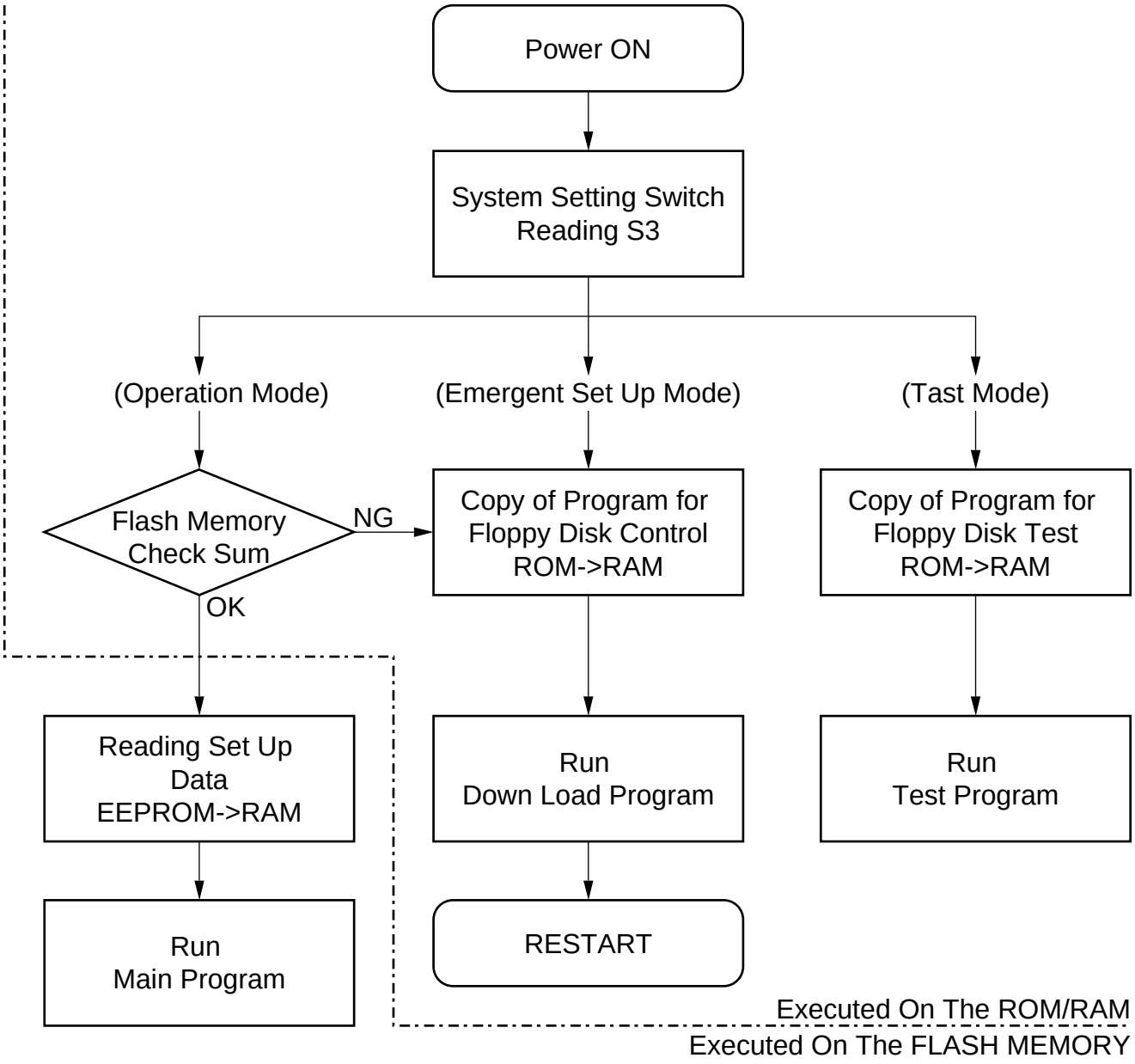


DVS-6000/C Memory Configuration



CPU-147 CPU Board (DVS-6000/C Mainframe)





Operation At Power-ON

Power Supply

CAUTION:

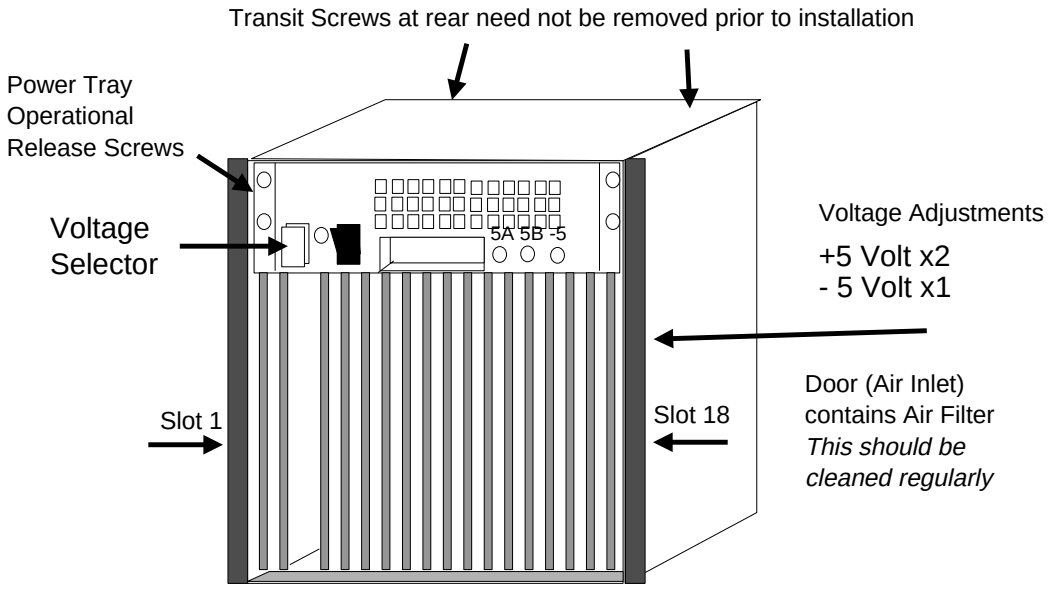
The DVS-6000C Mainframe Power supply is NOT Auto-range switching

SELECT the correct voltage setting BEFORE applying Power!

PDF Edition

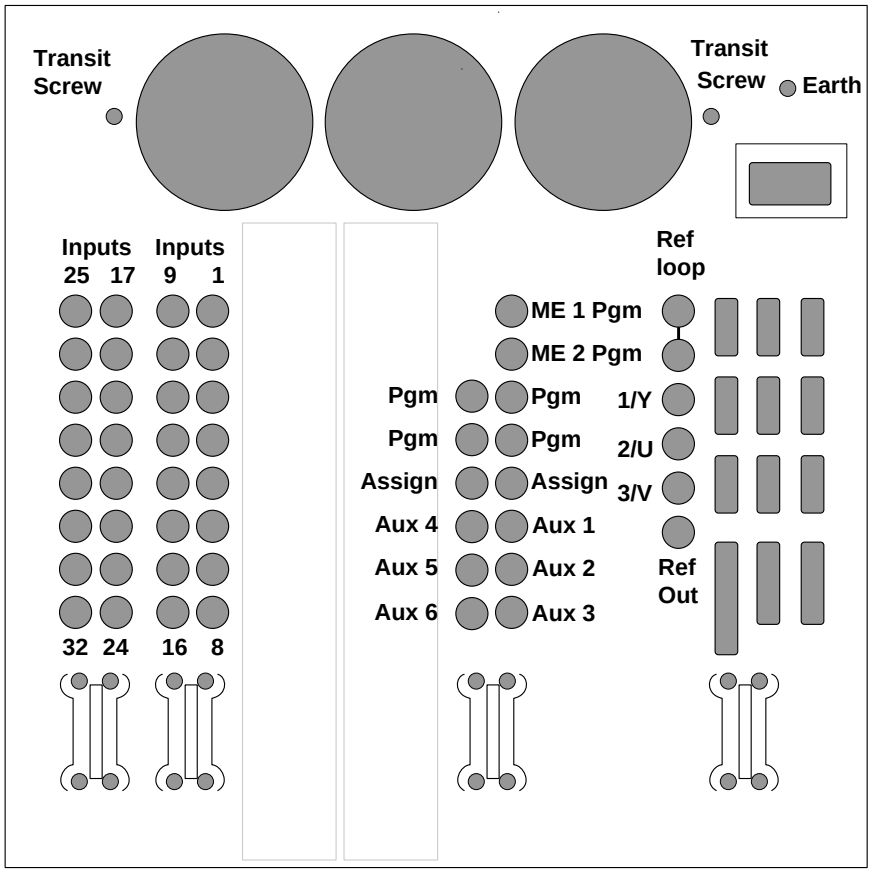
Power Tray and Voltage test slots

CAUTION: Check Voltage Range Selection prior to installation!



Two +5 Volt power supplies are provided: each supplying ½ the boards, and both monitored by the CPU board. The -5 volts supply is used by the ECL ICs including the SDI input and output ICs SBX1602A /1601A, and any analogue inputs / outputs.

Rear Connectors



IEC Mains Socket is attached to chassis, and not power tray

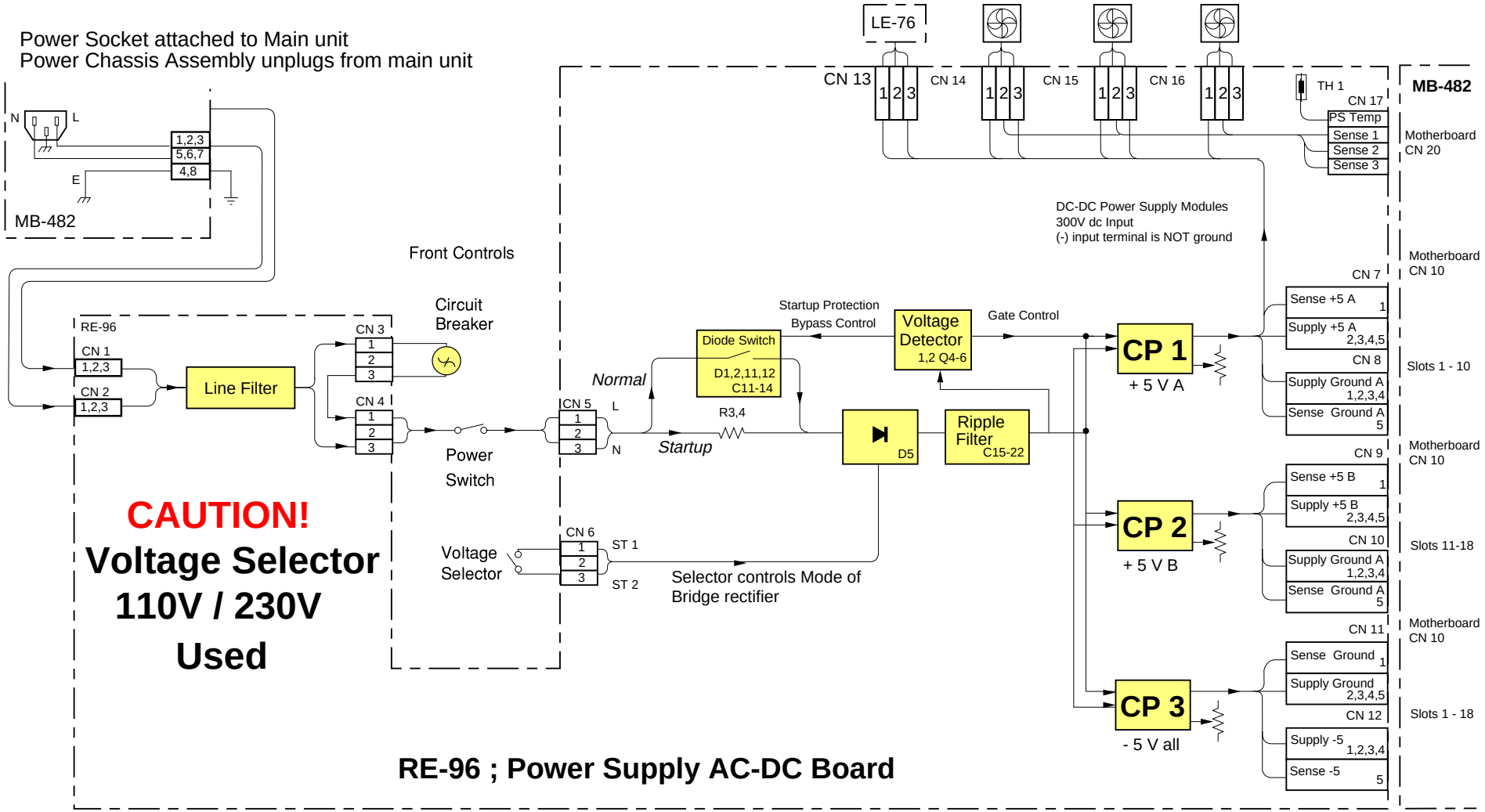
DME 1 (Aux)	**Edit A**	**Control Panel**
DME 2 (Aux)	**Edit B**	
User	**Serial Tally**	
"SCSI"	**GPI I/O**	**Terminal**

1/2/3 or YUV outputs are Analogue Edit Preview

Serial Tally labelled "Matrix" on schematics

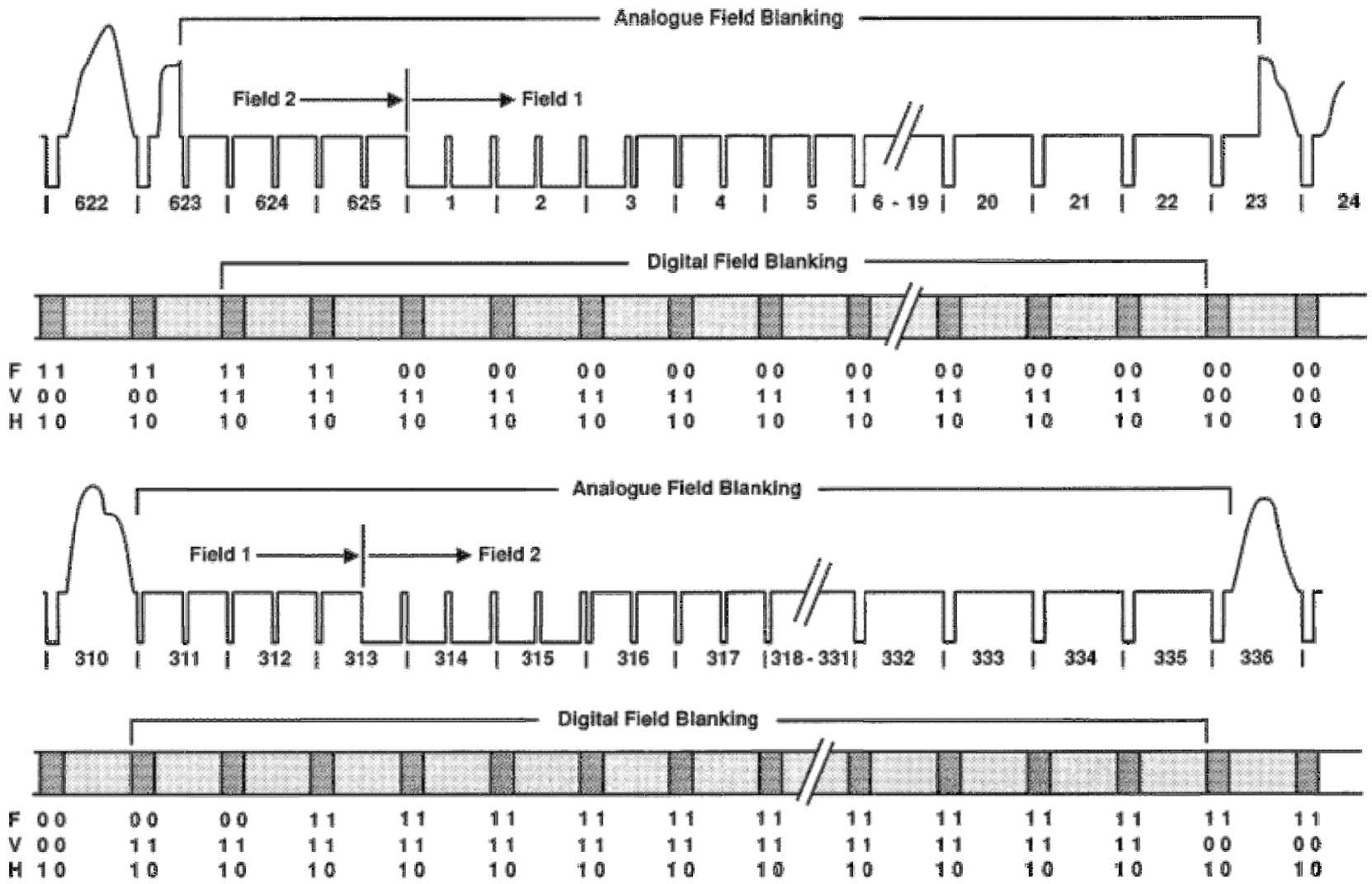
"SCSCI" interface intended for MY-67 via IF-499 on SG-211

Power Supply Assembly



Appendices

DIGITAL COMPONENT VIDEO



Appendix

Engineering Bulletins

Appendix

Engineering Bulletins

PDF Edition