

# Architecting and Operating PTP

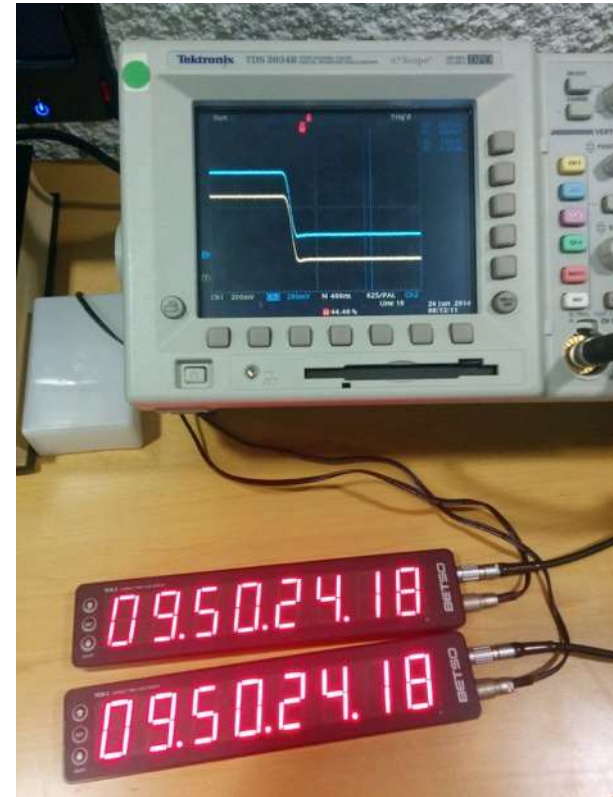
In IP based Production Facility

Rahul Parameswaran  
Sr. Technical Marketing Engineer  
[www.linkedin.com/in/rparames](https://www.linkedin.com/in/rparames)  
June 2020



# How do I generate a stable timing signal from an Ethernet port?

Source: an anonymous broadcast engineer



An abstract graphic on the left side of the slide, featuring a dark blue background with numerous small, colorful squares in shades of blue, green, yellow, and orange, arranged in a pattern that suggests a network or data flow.

## Agenda

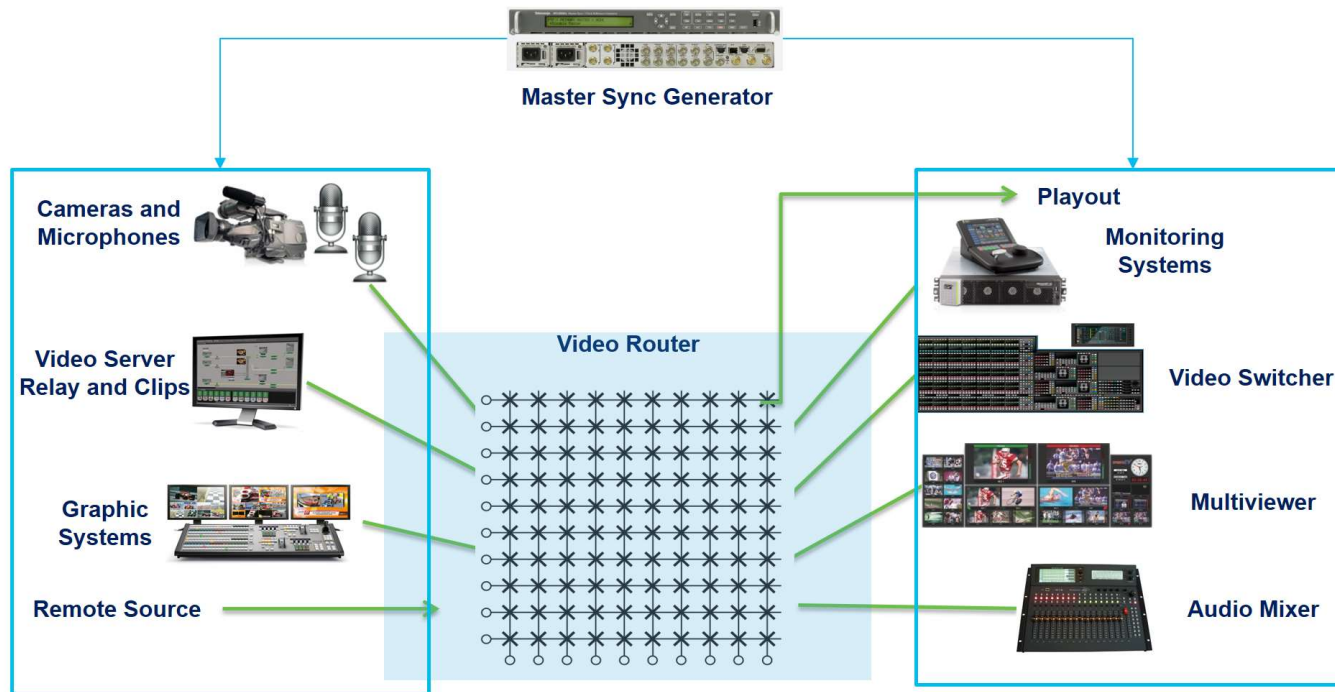
- How PTP works
- PTP Media Profiles
- Design Considerations
- Lessons Learnt from Deployments
- Troubleshooting tips
- Conclusion

The background of the slide is a dark blue field filled with numerous small, semi-transparent squares and dots. These elements are scattered across the frame, with a higher concentration of larger squares in the upper left and lower right areas. The colors of these elements include various shades of blue, green, yellow, orange, and red, creating a vibrant, pixelated effect.

# Introduction to PTP

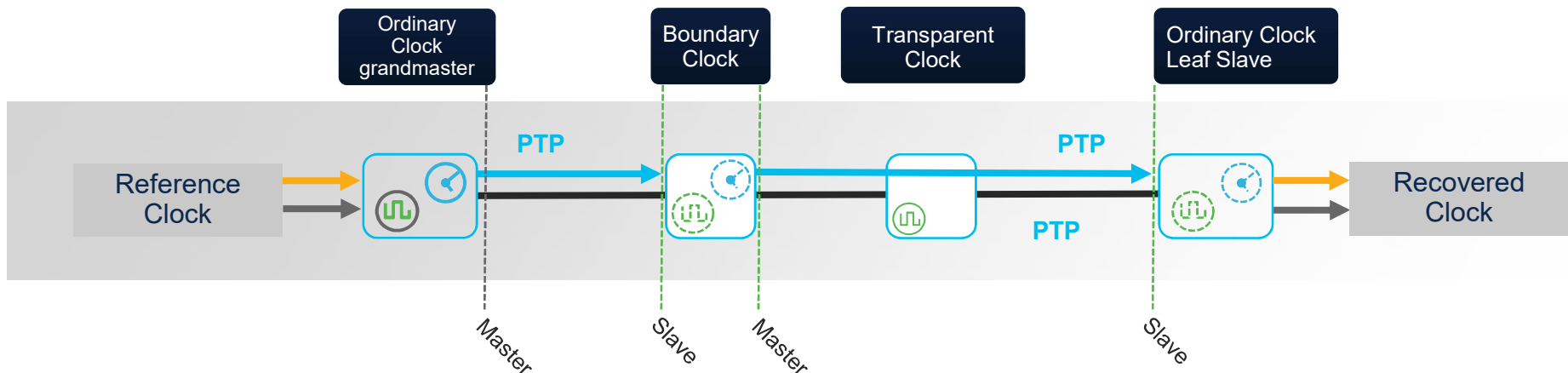


# Time Sync in SDI facility



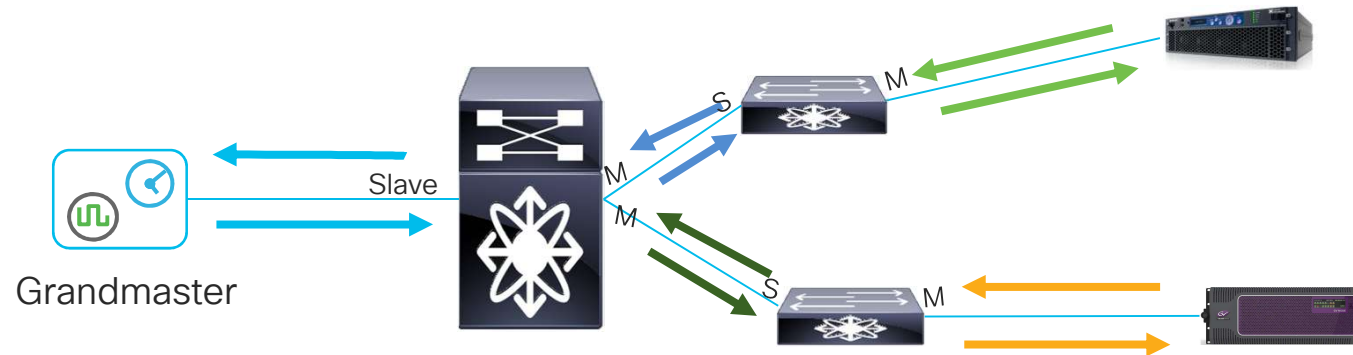
# Precision Time Protocol

- Two Way Time Transfer protocol (TWTT)
- Accuracy in a well designed E2E model in the nanosecond range
- Boundary Clocks (BC) and Transparent Clocks (TC) aim correcting delay variations, in both directions (asymmetry)



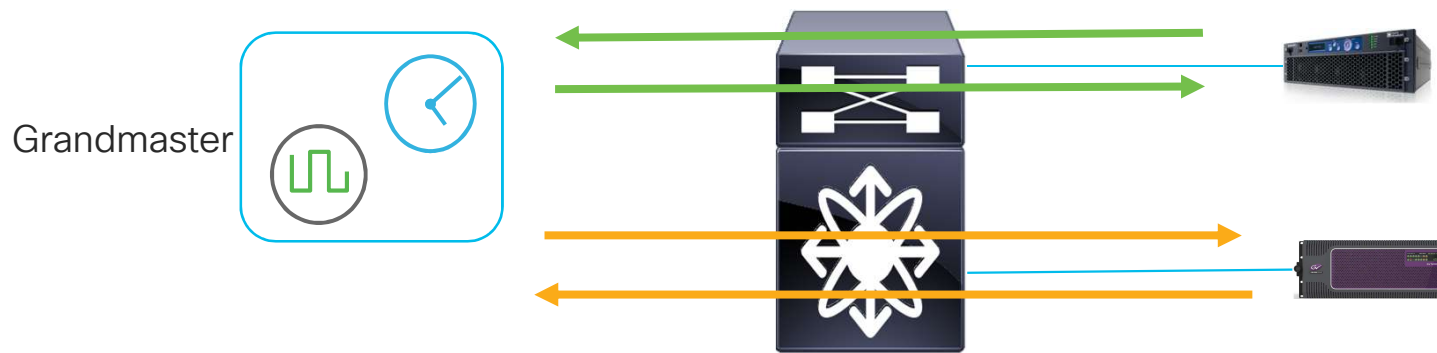
# Boundary Clock

- Boundary Clock
  - Has multiple PTP ports in a domain and maintains the timescale used in the domain. It has both master and slave ports.
  - It terminates the PTP flow, recovers the clock and timestamp, and regenerates the PTP flow



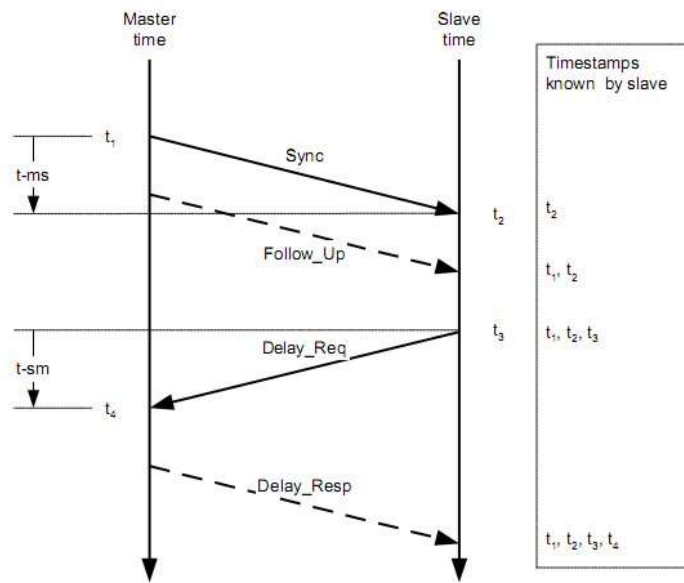
# Transparent Clock

- Transparent clock (TC)
  - A device that measures the time taken for a PTP event message to transit the device and compensate the packet delay by updating the timestamp.



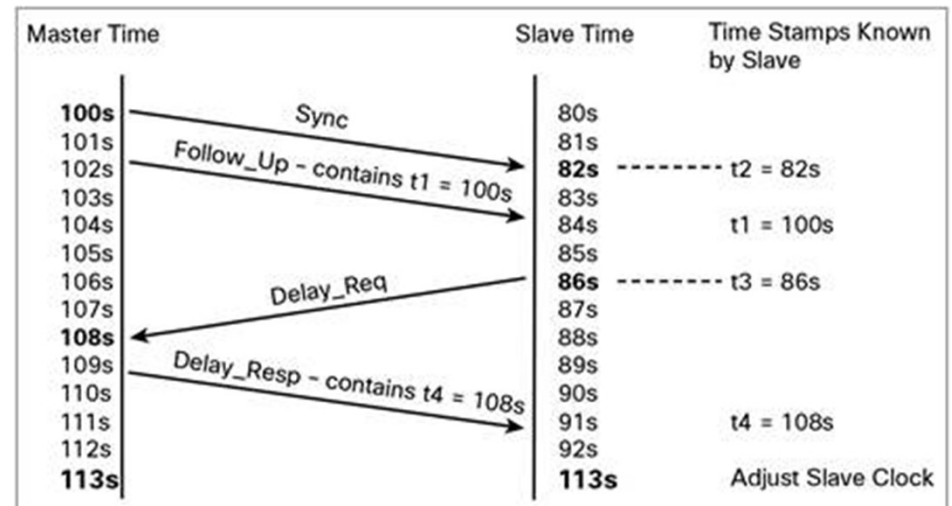


# How PTP Works?



## After the synchronization

Slave clock derives Time of Day, phase and frequency signals from the master



## Mean Path Delay

$$((t_2 - t_1) + (t_4 - t_3)) / 2$$

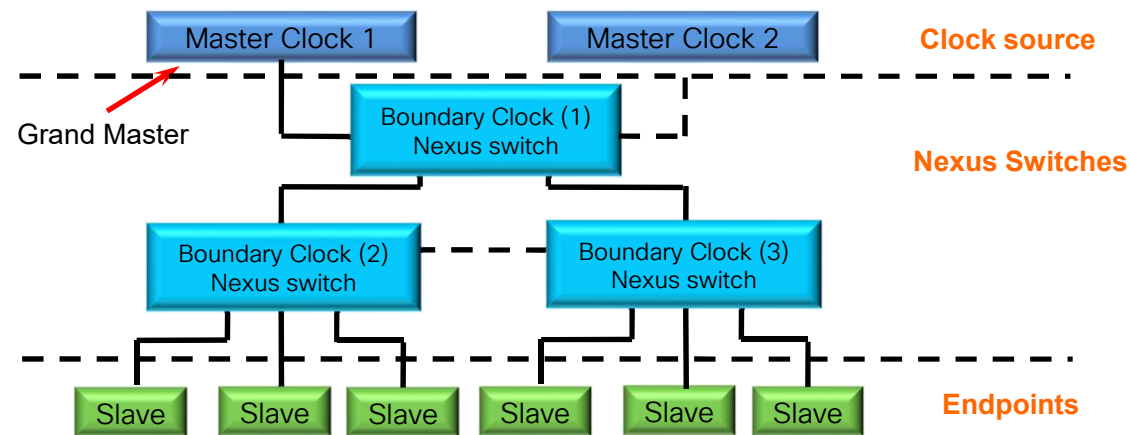
$$\begin{aligned} \text{Mean Path Delay} &= ((t_2 - t_1) + (t_4 - t_3)) / 2 \\ &= (-18 + 22) / 2 \\ &= 2 \end{aligned}$$

## Clock Offset

$$t_2 - t_1 - \text{mean path delay}$$

$$\begin{aligned} \text{Offset} &= t_2 - t_1 - \text{Mean Path Delay} \\ &= 82 - 100 - 2 \\ &= -20 \end{aligned}$$

# Hierarchy Network Clock Topology



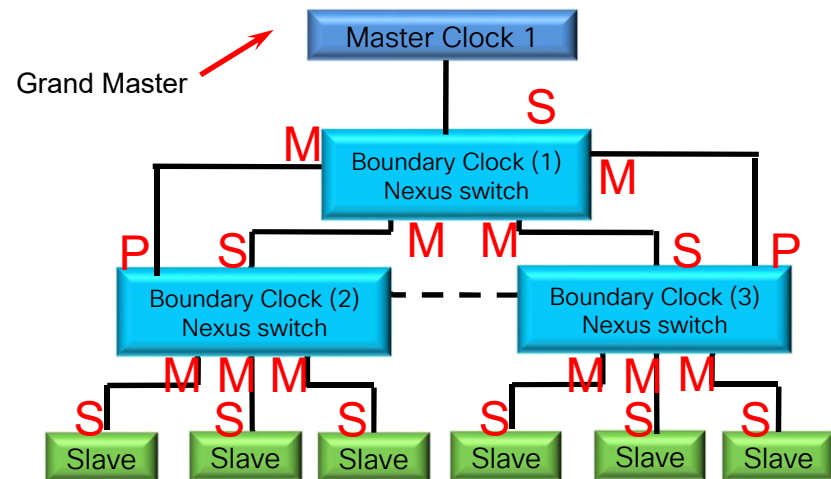
- 1 Elect the grand master, form a master-slave hierarchy. Grand master is selected based on Best Master Clock selection Algorithm (BMCA). (Master clock 1 is selected as Grand Master in the diagram)
- 2 Each slave clock synchronizes itself to the master clock

# Master Clock Selection

- BMCA (Best Master Clock Algorithm) runs locally on each port.
- It determines the best clock based on the attributes with following priority:
  1. **priority1**: User configurable designation that a clock belongs to an ordered set of clocks from which a master is selected
  2. **clockClass**: Defines a clock's TAI traceability
  3. **clockAccuracy**: Defines the accuracy of a clock
  4. **offsetScaledLogVariance**: Defines the stability of a clock
  5. **priority2**: User configurable designation providing finer grained ordering among otherwise equivalent clocks
  6. **clockIdentity**: A tie-breaker based on unique identifiers
  7. **StepsRemoved**: Selection of shortest path to the GrandMaster (for BC)
- BMCA determines the status of the port: **master, slave or passive**.
- BMCA runs continuously.

# PTP Port States

- MASTER: the port is advertising the time to a slave.
- SLAVE: the port is receiving the time from a master.
- PASSIVE: the port is connected to a master which is not the best clock.



The background of the slide is a dark blue field filled with numerous small, semi-transparent squares and dots. These elements are scattered across the frame, with a higher concentration of larger squares in the upper left and lower right areas. The colors of these elements include various shades of blue, green, yellow, orange, and red, creating a vibrant, pixelated effect.

# PTP Media Profiles

# PTP profiles for media & broadcast



- AES67 (Audio driven)
  - Based on IEEE 1588-2008 default profile /w specific message rates
    - Announce: 1 {0,4}
    - Sync: -3 {-4,1}
    - DelayReq: 0 {-3,Sync +5}\*
  - Allow all devices to be either Master or Slave
  - Multicast messages only
  - Default PTP domain: 0 {0-255}



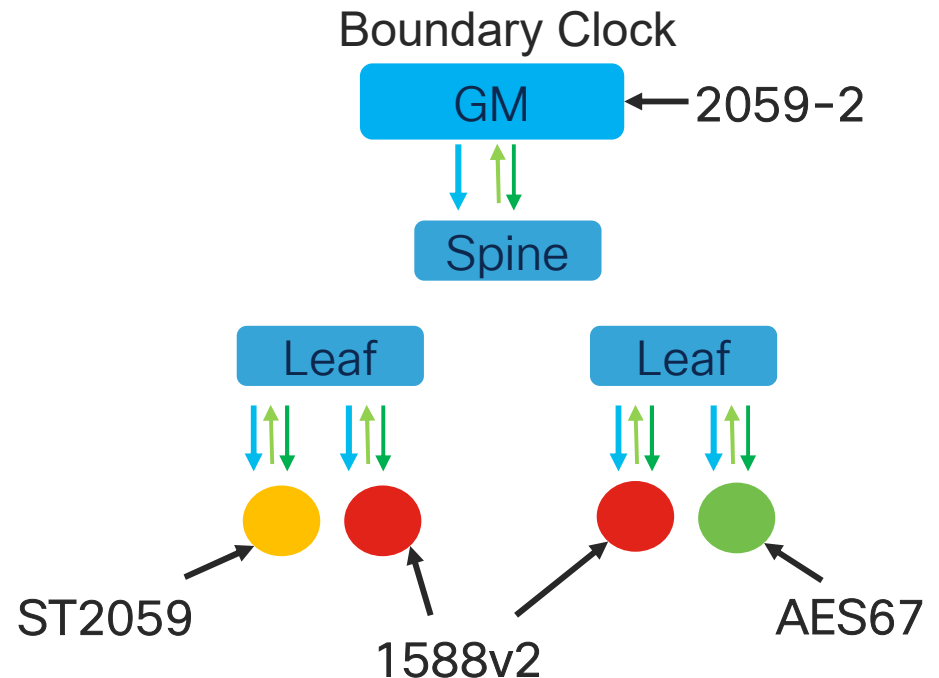
# PTP profiles for media & broadcast



- SMPTE 2059 (Video driven)
  - Based on a 5 sec fast locking requirement for endpoints /w spec rates
    - Announce: 1 {-3,1}
    - Sync: -3 {-7,-1}
    - DelayReq: 0 {Sync +0, Sync +5}
  - Default Slave mode unless can operate as Master
  - Additional PTP TLV with media specific information
    - Daily Jam Time, Default Frame rate, ...
  - Supports Multicast, Mixed (Mcast/Ucast) and Unicast modes
  - Default PTP domain: 127 {0-127}

# NX-OS implementation

- Support for AES67 message rates
  - ptp announce interval **aes67** <value>
  - ptp sync interval **aes67** <value>
  - ptp delay-request minimum interval **aes67** <value>
- Support for SMPTE 2059 message rates (and PTP mgmt TLV)
  - ptp announce interval **smpte-2059-2** <value>
  - ptp sync interval **smpte-2059-2** <value>
  - ptp delay-request minimum interval **smpte-2059-2** <value>



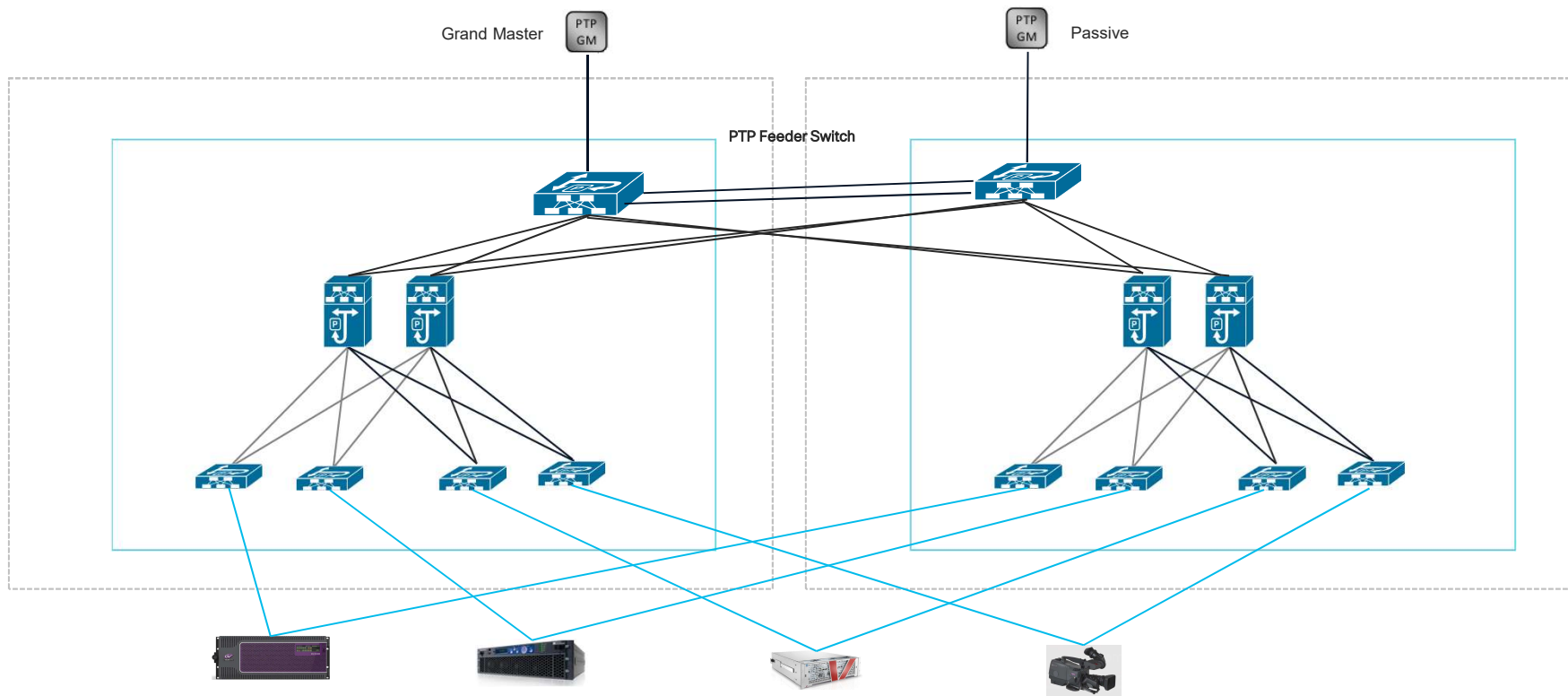
The background of the slide is a dark blue field filled with numerous small, semi-transparent squares and dots. These elements are scattered across the frame, with a higher concentration of larger squares in the upper left and lower right areas. The colors of these elements include various shades of blue, green, yellow, orange, and red, creating a vibrant, pixelated effect.

# Design Considerations

The background is a dark blue field filled with numerous small, semi-transparent squares and dots in various colors including light blue, green, yellow, orange, and red. These elements are scattered across the frame, with a higher concentration of orange and red squares forming a diagonal streak from the upper right towards the lower right. The text 'Studio Production' is overlaid in the lower-left area in a light blue, sans-serif font.

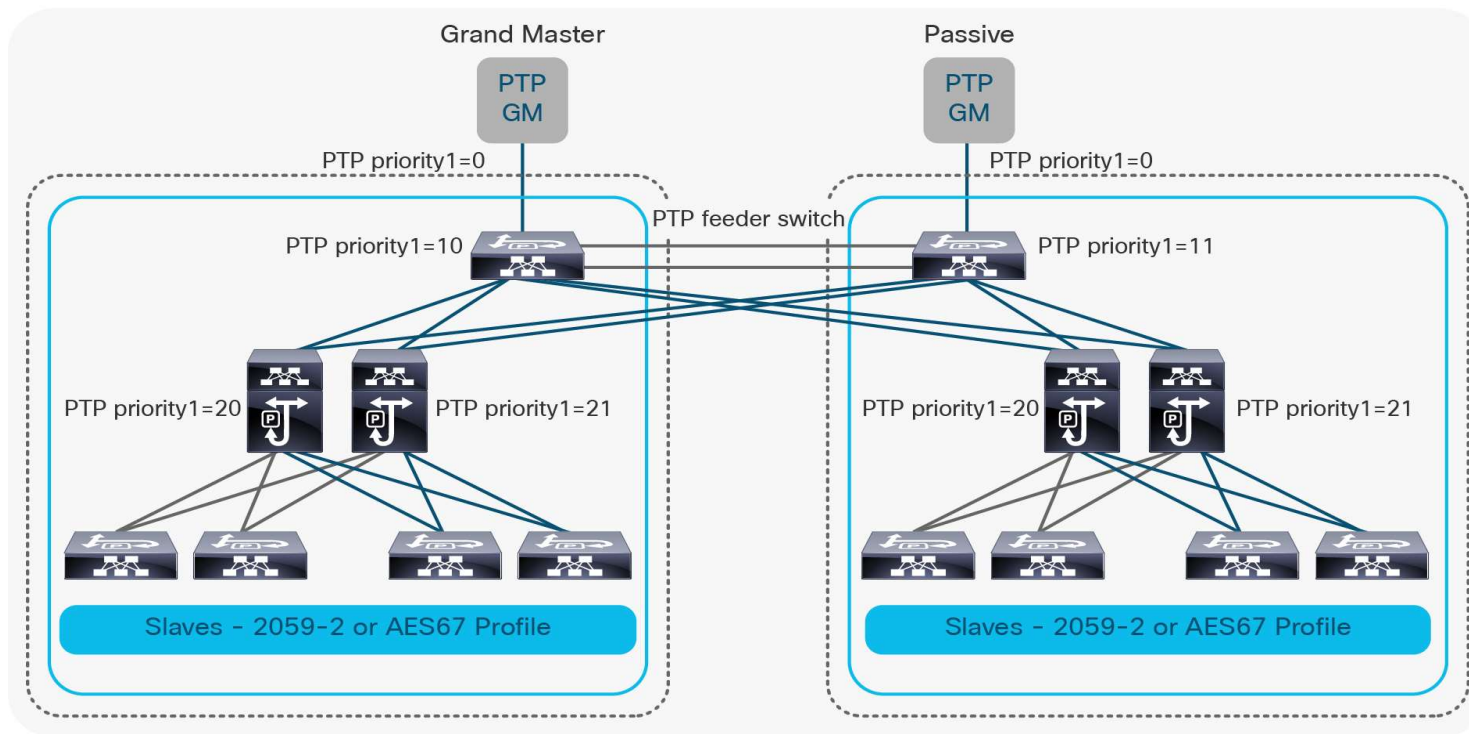
Studio Production

# 2020-7 and PTP design





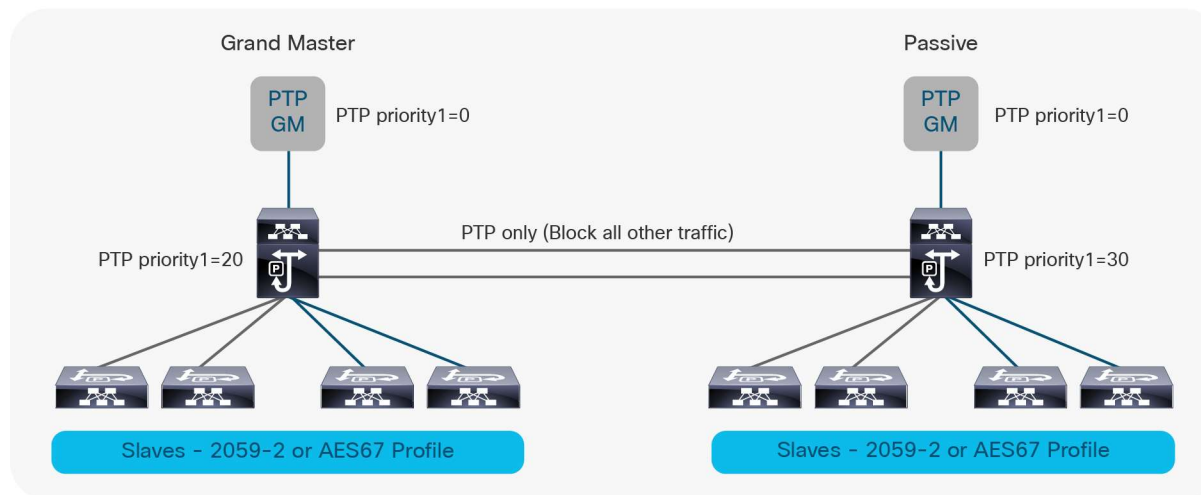
# Setting the Priority1 values



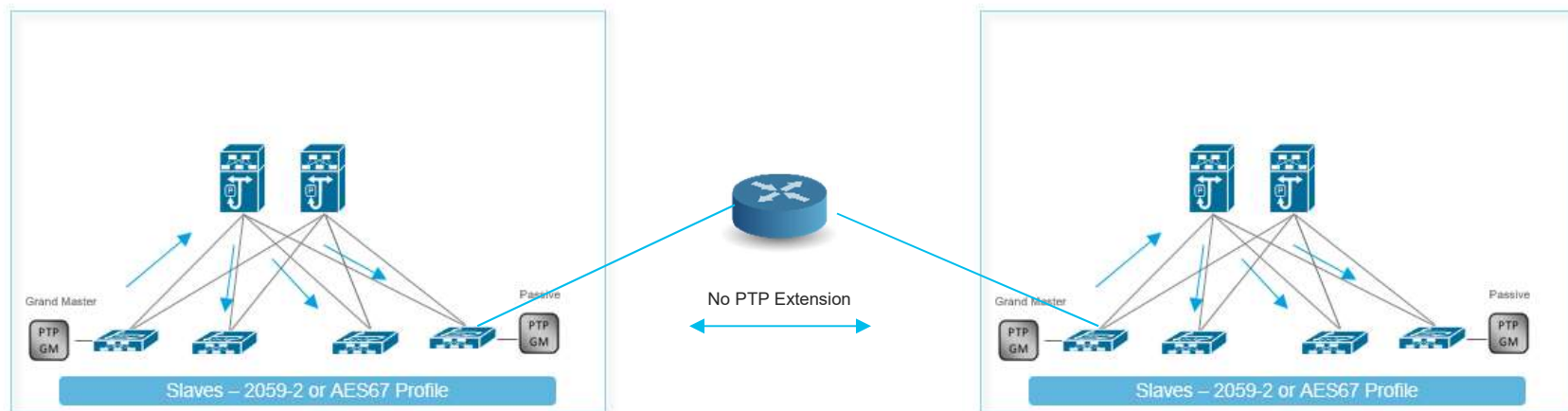


# Alternate designs

No PTP feeder switch



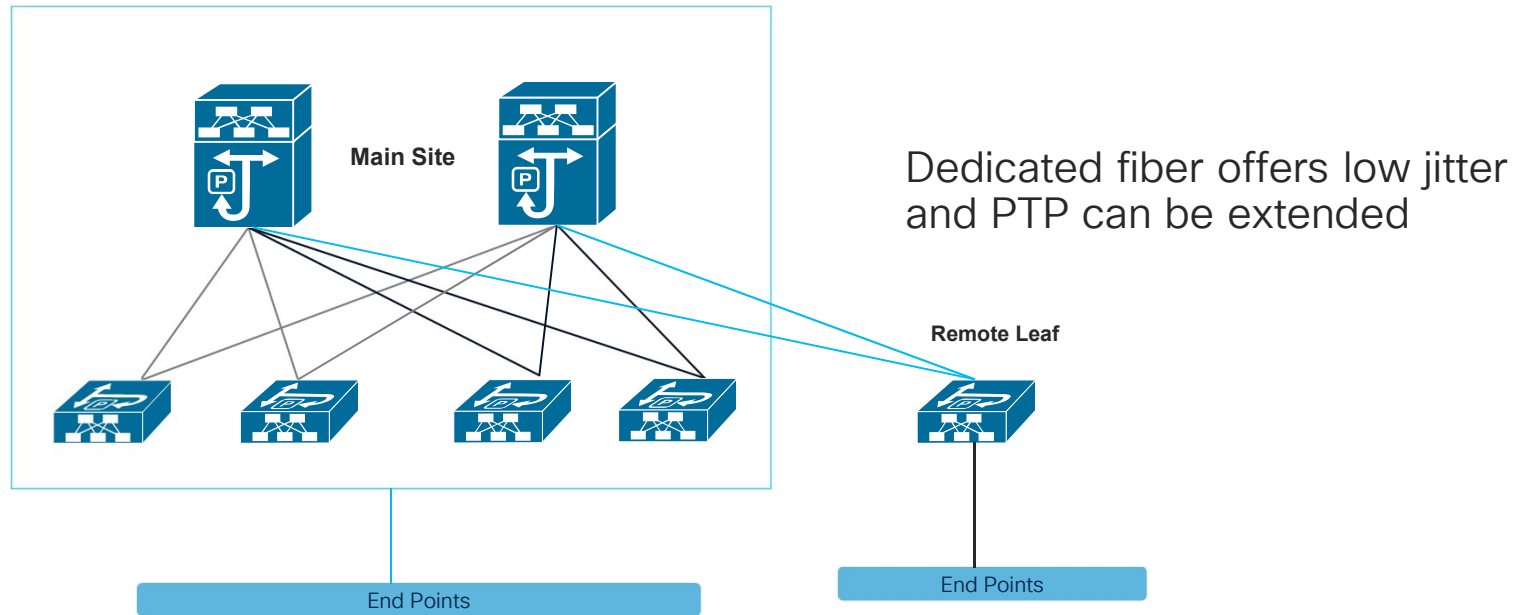
# PTP and Multi Site



- WAN could introduce high jitter that could result in high PTP offset
- Also PTP assumes symmetric delays in all calculations

# What about Remote Production

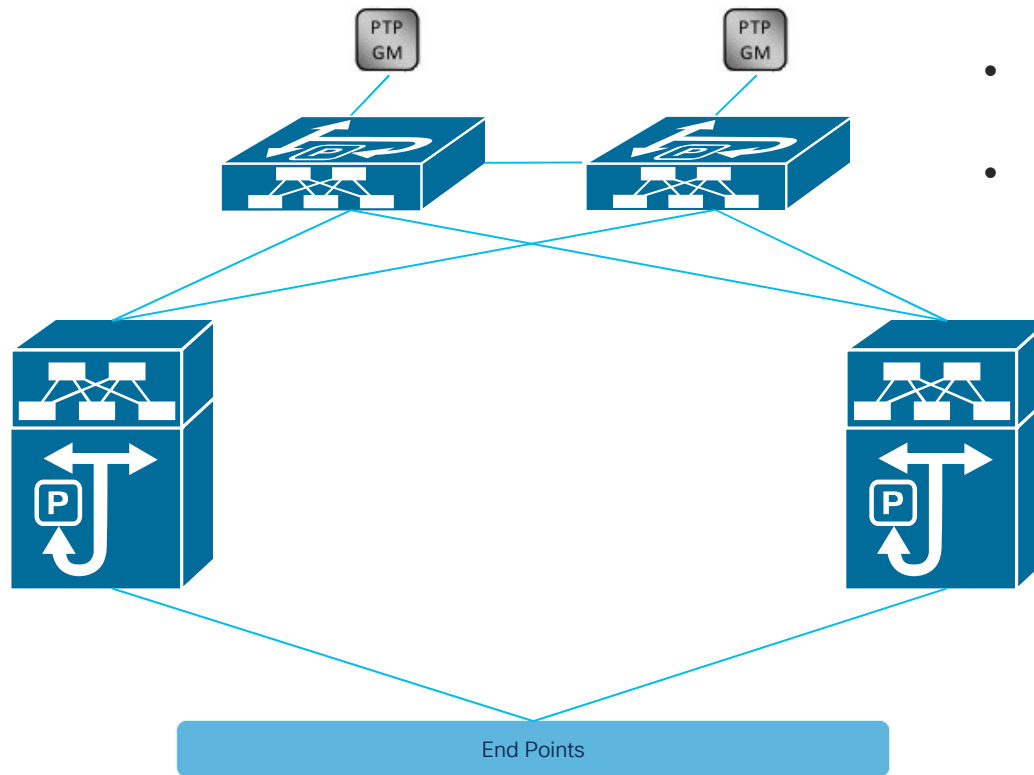
## Smaller Remote Studios





OBTrucks

# Obtruck Implementation



- PTP feeder switch also leveraged for control and audio
- Use different VLAN for control, audio
- PTP interfaces can be layer 3 point to point



What did we learn?



# PTP Boundary Clock and Scale

How do you measure Boundary Clock Performance

- Questions to ask you network vendor
  - How many interfaces can PTP be enabled on (master ports)?
  - How many slaves can each interface support?
  - How many slaves can the system itself support?
  - How do you qualify the above scale?

# Achieving PTP Scale on a Modular Chassis

Innovation through PTP Offload



- PTP Offloaded to Line card CPU
- Main Supervisor synchronizes the line card
- Each Line card services endpoints connected to it
- Results in increased scale with superior accuracy

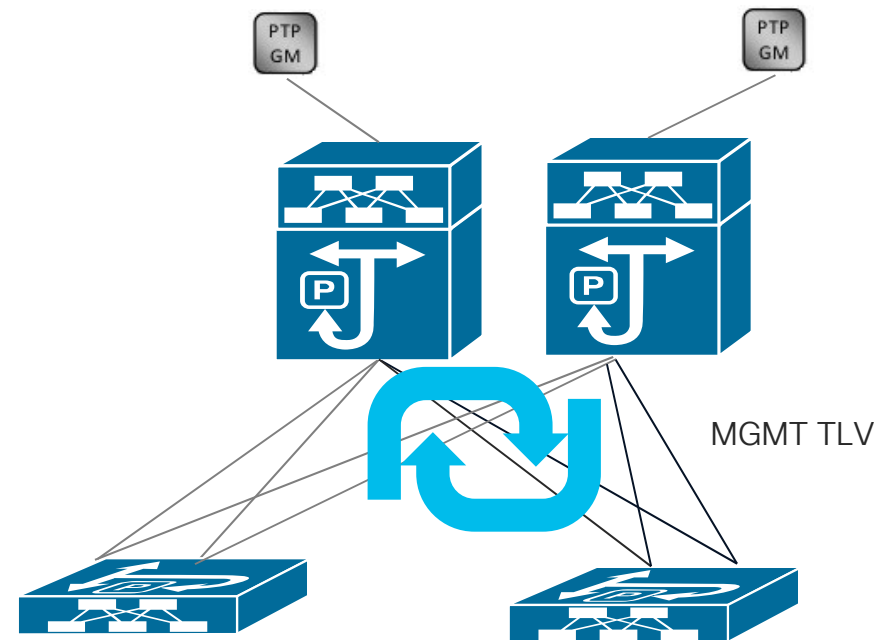
# Cisco Nexus 9000 PTP scale

- Fixed Platform Nexus 9300 EX, FX, FX2, FX3,GX
  - Max PTP interfaces : 64 (Shipping), 144 (NXOS 9.3(5) and later)
  - Max number of slaves behind each interface – 48
  - Max number of slaves – 256
- Modular Platform like 9500-R
  - Max PTP interfaces per line card: 64 (Shipping) , 144 (9.3(5) and later)
  - Max PTP interfaces per chassis : 512 ( future release can support 1152)
  - Max number of slaves behind each interface – 48
  - Max number of slaves per system – 1152

# ST2059-2 and Management TLV

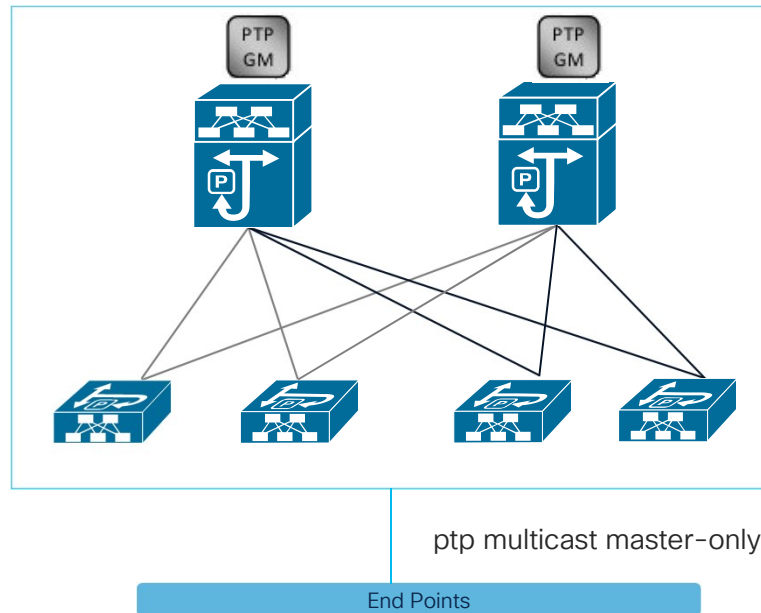
Watch out for those loops!

- During GM failure BMCA kicks in to elect new GM
- Interfaces state could go from slave to pre-master/master
- During that phase MGMT TLVs can loop
- NX-OS does not forward TLV on passive interfaces or pre-master



# Who becomes the Master?

## Basic Network Security for PTP

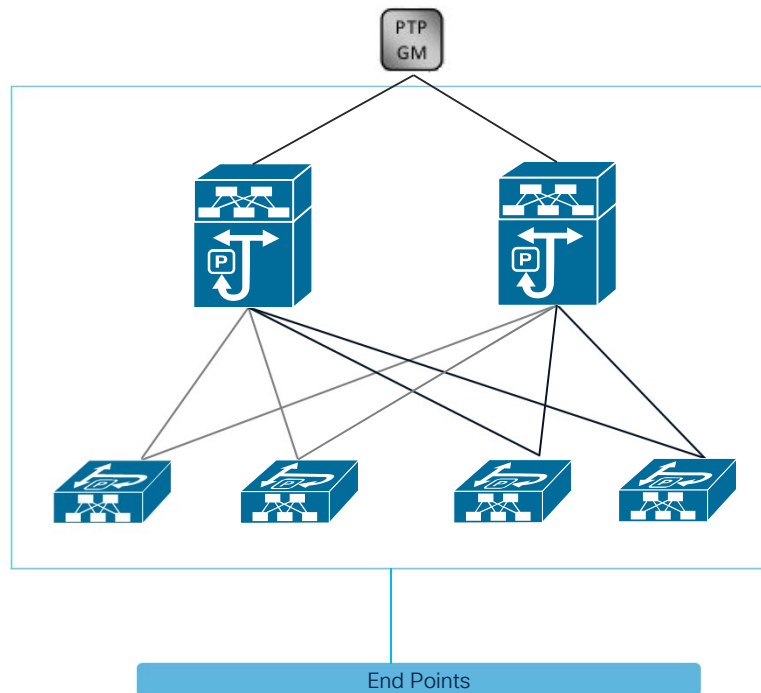


- PTP BMCA elects the GM
- Any device can send Announce messages with superior values
- Device can take over as GM!!

```
interface et1/1
description IPG
ptp
ptp multicast master-only
```

# Using Redundant interfaces on GM

Make sure they are isolated

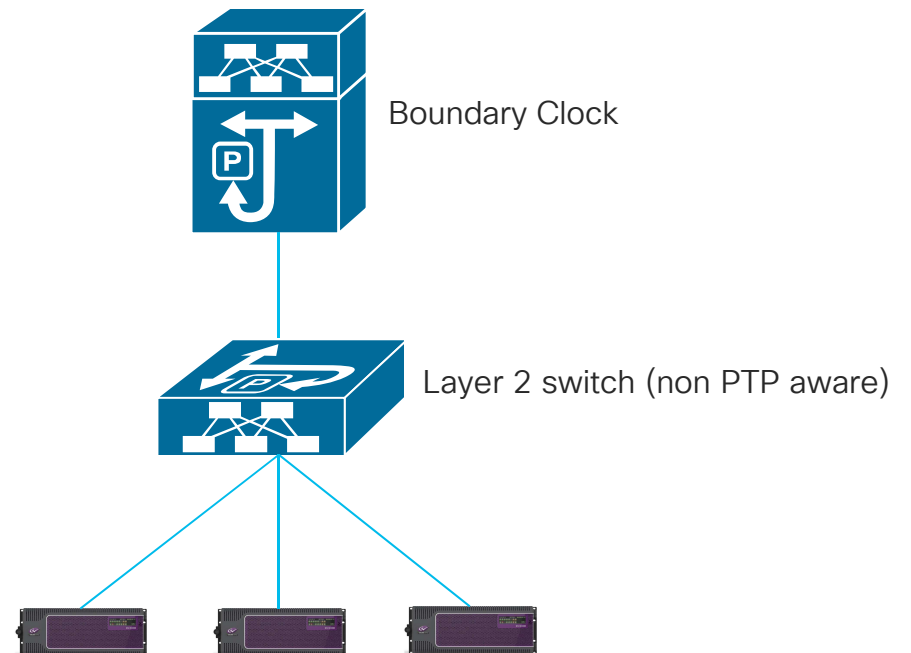


- Make sure different interfaces on the GM are in isolated mode
- This ensures the delay request sent from one system does not get forwarded to other



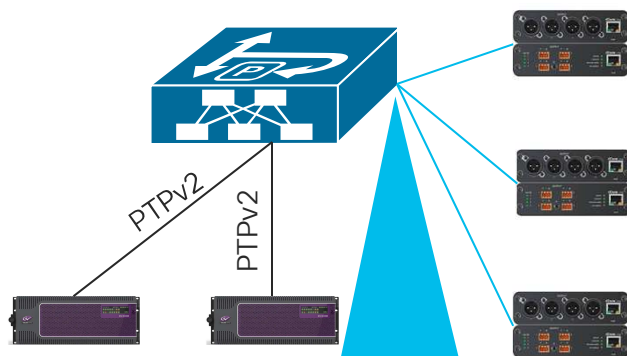
# Multicast mode vs Mixed Mode

- PTP multicast mode – all messages are multicast
- PTP mixed mode – Unicast delay request and response
- Mixed mode reduces the number of PTP packets hitting an endpoint
- Improved performance as a result of fewer PTP packets to be processed

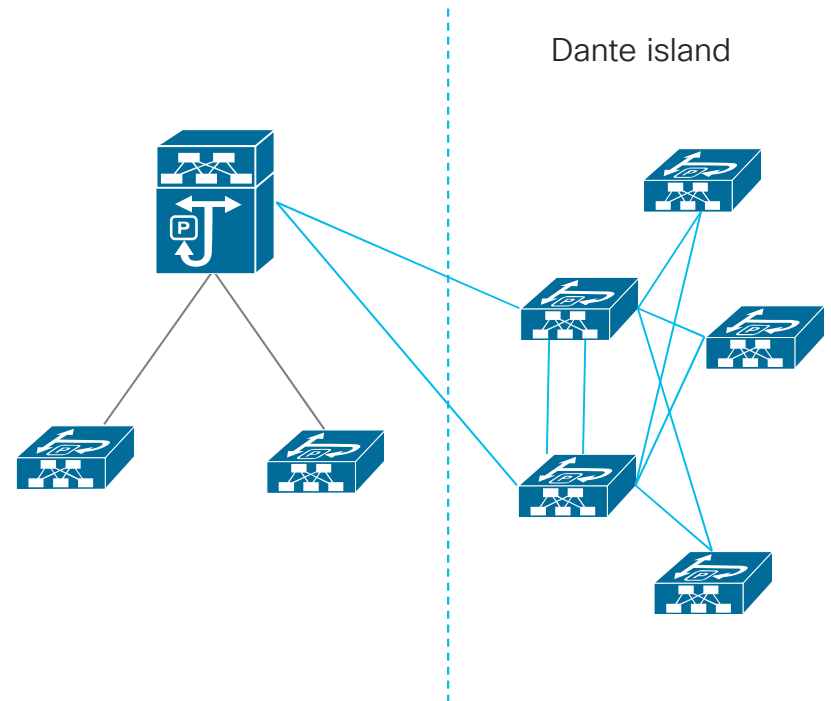


# Working with Dante (PTPv1)

How to onboard Dante endpoints



Place Dante endpoint in same vlan  
Do not enable PTP on these interfaces



# PTP and Control Plane Policing

## Modify Default CoPP

- CoPP protects CPU
- PTP rate limited by default to 128kbps
- Increase CIR to 1024 Kbps

```
Leaf-1 # show policy-map interface control-plane class nbm-copp-class-redirect
```

```
Control Plane
```

```
Service-policy input: nbm-copp-policy-strictv
```

```
class-map nbm-copp-class-redirect (match-any)
```

```
match access-group name nbm-copp-acl-ntp
```

```
match access-group name nbm-copp-acl-ntp-l2
```

```
match access-group name nbm-copp-acl-ntp-uc
```

```
set cos 1
```

```
police cir 1024 kbps , bc 32000 bytes
```

```
module 1 :
```

```
transmitted 1724750 bytes;
```

```
dropped 0 bytes;
```

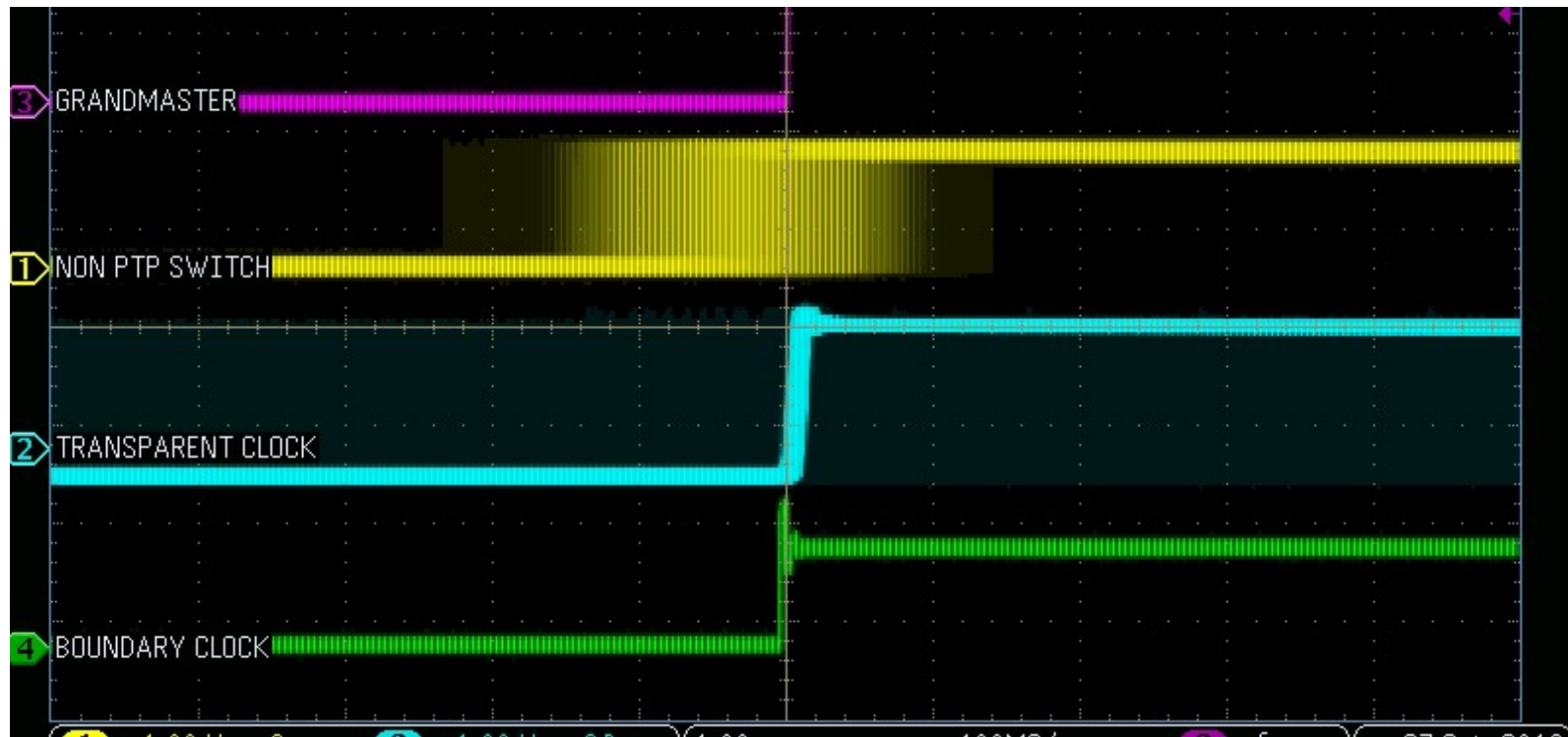
# PTP and Quality of Service

## Prioritizing PTP

- Ensure PTP is in highest Priority queue
- Nexus automatically places PTP in highest priority queue (control)



# Comparing PTP performance



SMPTE PTP Demo at Annual Tech Conference 2016

The background is a dark blue field filled with numerous small, semi-transparent squares and dots in various colors including light blue, green, yellow, orange, and red. These elements are scattered across the frame, with a higher concentration of orange and red squares forming a diagonal streak from the upper right towards the lower right. The overall effect is a dynamic, pixelated or digital aesthetic.

# Troubleshooting Tips



# Checking PTP at the Switch

- show ptp brief
- show ptp clock
- show ptp parent

Spine1# sh ptp brief

PTP port status

Port	State
Eth1/1	Master
Eth1/3	Master
Eth1/33	Slave
Eth1/34	Disabled
Eth1/35	Disabled
Eth1/36	Master

```
Spine1# show ptp clock
PTP Device Type : boundary-clock
PTP Device Encapsulation : layer-3
PTP Source IP Address : 172.16.1.1
Clock Identity : a8:b4:56:ff:fe:0c:f7:f3
Clock Domain: 100
Slave Clock Operation : Two-step
Master Clock Operation : Two-step
Slave-Only Clock Mode : Disabled
Number of PTP ports: 6
Priority1 : 255
Priority2 : 255
Clock Quality:
    Class : 248
    Accuracy : 254
    Offset (log variance) : 65535
Offset From Master : 40
Mean Path Delay : 176
Steps removed : 2
Correction range : 100000
MPD range : 1000000000
Local clock time : Tue Jun 11 19:39:37 2019
Hardware frequency correction : NA
```

Spine1# show ptp parent

## PTP PARENT PROPERTIES

```
Parent Clock:
Parent Clock Identity: 6c:b2:ae:ff:fe:9f:3e:1f
Parent Port Number: 208
Observed Parent Offset (log variance): N/A
Observed Parent Clock Phase Change Rate: N/A

Parent IP: 172.16.1.4
Grandmaster Clock:
Grandmaster Clock Identity: 00:04:b3:ff:fe:f0:19:ca
Grandmaster Clock Quality:
    Class: 6
    Accuracy: 45
    Offset (log variance): 16542
    Priority1: 1
    Priority2: 2
```

# Checking PTP Messages at the Switch Port

- sh ptp port interface ethernet 1/x counters
- sh ptp corrections

Spine1# sh ptp counters int e1/36

PTP Packet Counters of Interface Eth1/36:

Packet Type	TX	RX
Announce	66	0
Sync	523	0
FollowUp	523	0
Delay Request	0	131
Delay Response	131	0
PDelay Request	0	0
PDelay Response	0	0
PDelay Followup	0	0
Management	0	0

Spine1# sh ptp corrections

PTP past corrections

Slave Port	SUP Time	Correction(ns)	MeanPath Delay(ns)
Eth1/33	Tue Jun 11 19:37:08 2019 988176	24	184
Eth1/33	Tue Jun 11 19:37:08 2019 738202	2	184
Eth1/33	Tue Jun 11 19:37:08 2019 487105	16	184
Eth1/33	Tue Jun 11 19:37:08 2019 235536	16	176
Eth1/33	Tue Jun 11 19:37:07 2019 991135	56	176
Eth1/33	Tue Jun 11 19:37:07 2019 733451	-85	176
Eth1/33	Tue Jun 11 19:37:07 2019 486743	-12	176
Eth1/33	Tue Jun 11 19:37:07 2019 233045	40	180
Eth1/33	Tue Jun 11 19:37:06 2019 982194	16	180
Eth1/33	Tue Jun 11 19:37:06 2019 736855	-1	180
Eth1/33	Tue Jun 11 19:37:06 2019 481447	32	180
Eth1/33	Tue Jun 11 19:37:06 2019 230463	0	172
Eth1/33	Tue Jun 11 19:37:05 2019 979343	40	172
Eth1/33	Tue Jun 11 19:37:05 2019 733087	-57	172
Eth1/33	Tue Jun 11 19:37:05 2019 477642	8	172
Eth1/33	Tue Jun 11 19:37:05 2019 228712	24	188
Eth1/33	Tue Jun 11 19:37:04 2019 981574	16	188
Eth1/33	Tue Jun 11 19:37:04 2019 727055	-2	188
Eth1/33	Tue Jun 11 19:37:04 2019 476039	36	188

# Logging PTP state change

From Boundary Clock Switch

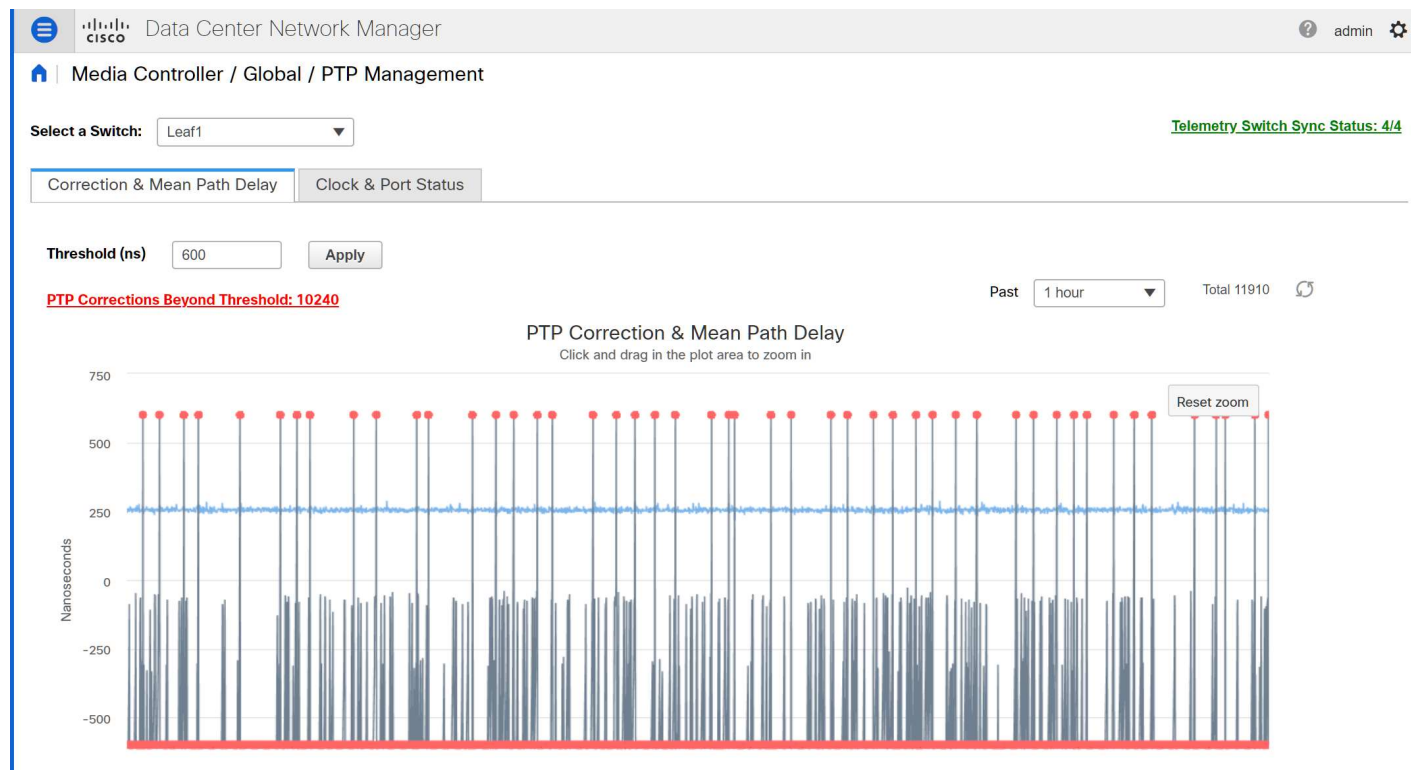
```
2020 Mar 3 13:48:57 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction -98302(nsec)
2020 Mar 3 13:48:57 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction 110720(nsec)
2020 Mar 3 14:14:45 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction -32759(nsec)
2020 Mar 3 14:14:45 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction 55334(nsec)
2020 Mar 3 14:14:46 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction -16304(nsec)
2020 Mar 3 14:18:57 PTPstackA %VSHD-5-VSHD_SYSLOG_CONFIG_I: Configured from vty by admin on 192.168.10.150@pts/0
2020 Mar 3 14:35:49 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction -32737(nsec)
2020 Mar 3 14:35:49 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction 55350(nsec)
2020 Mar 3 14:35:49 PTPstackA %PTP-2-PTP_HIGH_CORR: Slave port Eth1/1 High correction -16319(nsec)
PTPstackA#
```

```
2019-11-14 17:17:08,859 - Interface in use changed: ETH2
2019-11-14 17:17:08,859 - Grand master clock id changed: ec:46:70:ff:fe:0a:9b:19
2019-11-14 17:17:08,859 - Parent clock id changed: 00:3a:9c:ff:fe:6d:77:47
2019-11-14 17:17:08,859 - Steps removed changed: 5
2019-11-14 17:17:09,859 - Eth1 ptp status changed: Uncalibrated
2019-11-14 17:17:09,859 - Eth2 ptp status changed: Listening
2019-11-14 17:17:09,859 - Interface in use changed: ETH1
2019-11-14 17:17:09,859 - Grand master clock id changed: 08:00:11:ff:fe:23:19:66
2019-11-14 17:17:09,859 - Parent clock id changed: 00:3a:9c:ff:fe:6d:78:c7
2019-11-14 17:17:09,859 - Steps removed changed: 4
2019-11-14 17:17:10,958 - Eth1 ptp status changed: Listening
2019-11-14 17:17:10,958 - Eth2 ptp status changed: Uncalibrated
2019-11-14 17:17:10,958 - Interface in use changed: ETH2
2019-11-14 17:17:10,958 - Time source changed: Internal Oscillator
2019-11-14 17:17:10,959 - Grand master clock id changed: 00:3a:9c:ff:fe:6d:77:47
2019-11-14 17:17:10,959 - Parent clock id changed: 00:3a:9c:ff:fe:6d:77:47
```

From 2110 IPG

# DCNM PTP Monitoring

## Leveraging Streaming Telemetry



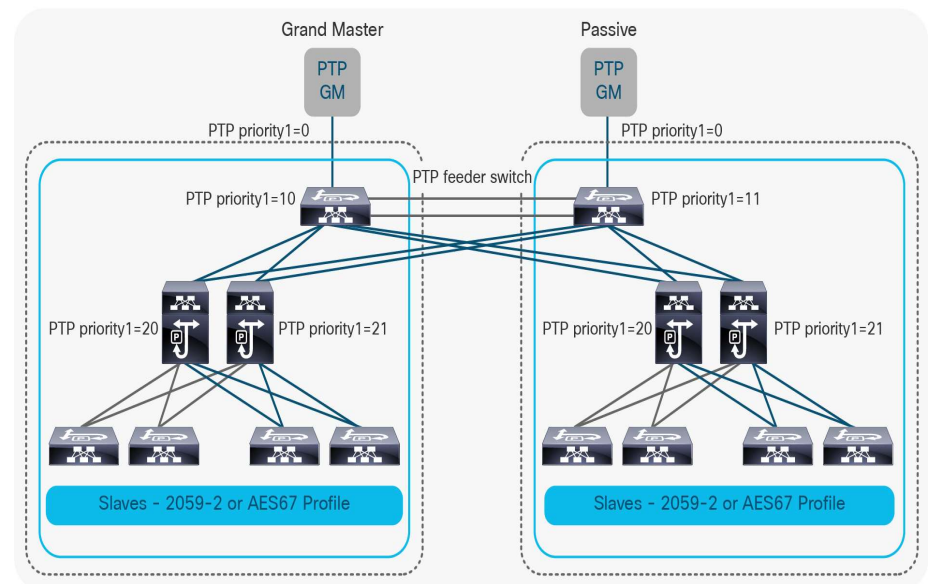


The background of the slide is a dark blue field filled with numerous small, semi-transparent squares and dots. These elements are scattered across the frame, with a higher concentration of larger squares in the upper left and lower right areas. The colors of these elements include various shades of blue, green, yellow, orange, and red, creating a vibrant, pixelated effect.

In Conclusion

# Conclusion

- PTP provides very precise and accurate time synchronization
- Boundary Clock enables distributed PTP architecture
- Ensure design accounts for failures
- Take Boundary Clock scale into consideration
- Ensure some amount of security is in place
- Leverage operations tools to monitor PTP performance



# Useful Links

## PTP Design Guide

<https://www.cisco.com/c/en/us/products/collateral/switches/nexus-9000-series-switches/guide-c07-742142.html>

## IPFM Design Guide

<https://www.cisco.com/c/en/us/products/collateral/switches/nexus-9000-series-switches/white-paper-c11-738605.html>