Rev. 1

Why Jitter matters in high resolution digital audio systems

A description of jitter analyses and jitter reduction in
a 24bit/96k Broadcast 4 channel D/A converter.

Peter Schut
Axon Digital Design BV
The Netherlands
peter.schut@axon.nl
www.axon.nl

Abstract

Although jitter is widely accepted as a common artifact in today's digital audio systems, the effect of real-world jitter contamination is often underestimated. The impact of jitter can be especially dramatic in a high density, large broadcast environment where long cable runs and impedance mismatches are common. By introducing a third generation converter that incorporates extreme low intrinsic jitter and excellent jitter attenuation capabilities, Axon Digital Design is trying to motivate the broadcast industry to adopt high speed coaxial interfaces instead of the common twisted pairs in order to reduce interface induced jitter.

Introduction

Jitter in digital audio interfaces is an artifact that can be induced at the source or generated by the interface itself. Clock jitter caused by the generation of an AES/EBU signal can be the start of a resolution decrease, but the bandwidth limitations of the interface itself is the main cause of jitter contamination at the point where it matters: the conversion to analog. A second misunderstanding is that sample-rate converters are a solution to interface jitter. Although the output of a sample-rate converter can have an extremely low clock jitter, the harm is already done in the conversion. Re-sampling audio data with the wrong timing information gives an error in the reconstructed data stream. The clock jitter will be low but the representation of the analog waveform is incorrect. A jitter analyzer looking at interface jitter has no means of determining what the analog waveform should look like. A low jitter figure after a sample-rate converter is no guarantee that the signal was not contaminated.

In the following discussion I will give practical examples of what a standard twisted pair can do to your D/A conversion process and how a low jitter dual PLL can correct this. Several plots of the high-resolution jitter analyzer used by Axon Digital Design will show how both data induced, and interface induced jitter artifacts, work their way through normal single PLL clock recovery circuits. Jitter in the D/A process can lower the resolution in the reconstructed analog domain to levels that are clearly audible and demonstrate to every audio engineer the harm to system integrity and system transparency.

Clock Jitter

The jitter responsible for the loss of resolution and distortion in the analog reconstructed signal is clock jitter. This clock jitter is either the wordclock or masterclock of the D/A converter chip. Depending on the conversion principle used by the actual converter, either the masterclock or wordclock needs to be jitter free. The jitter measured at this point is the timing deviation of the transitions compared to an ideal clock. These timing variations are divided into a jitter frequency and amplitude. Examining the eye pattern of these clocks with an oscilloscope can tell you something of the peak to peak value, but gives you no information of the jitter frequency. Using an oscilloscope for jitter amplitudes lower than 1ns is almost impossible. So we need a dedicated jitter analyzer. The unit Axon is using has an intrinsic jitter of 0.4 ps RMS for a clock frequency of 12.288 MHz (=256 x 48 kHz) and 1.2 ps for 192 kHz (=4 x 48 kHz).
The theoretical degradation for high frequencies (>5kHz) is shown in *table1*. This table tells nothing of the audibility of the jitter present, just the measurable artifact that jitter has on discrete frequencies.
If we look at the rise in noise floor we get the values shown in *table 2*.

jitter	8ps	16ps	32ps	64ps	128ps	256ps	05ns	1ns	2ns	4ns
Resolution in bits	20	19	18	17	16	15	14	13	12	11

Table 1: maximum jitter for a given resolution

jitter	1ns	2ns	4ns	8ns	16ns
Noise floor	-105dB	-97dB	-90dB	-84dB	-79dB

Table 2: maximum jitter for a given noise-floor

High frequency jitter causes more audible degradation than low frequency jitter. High frequency signals are also more degraded by a certain amount of jitter than low frequency signals.

Interface Jitter

Interface jitter is probably the biggest contributor to the overall jitter performance of a system. In particular, the bandwidth limitations of twisted pair digital audio connections can cause severe degradation of the overall performance in a D/A converter. Because of the inherent bandwidth limitation of the interface cable, the waveform change of the AES/EBU signal causes severe degradation of the timing resolution in commonly used receiver chips. The industry standard Crystal semiconductor CS8412 and CS8414 (for 96k) has a jitter attenuation frequency of 25kHz. This is the frequency at which the integral PLL starts to attenuate the incoming jitter. Baring in mind that the jitter frequency of any concern ranges up to 40kHz, we can conclude that the jitter attenuation capabilities of these chips are insignificant. The big advantage of these chips is the capability to reliably lock to difficult jittery signals of various amplitudes with good integrity. This is key to robust functioning of a D/A converter.

Dual PLL topology

The capability of reliable data recovery and jitter attenuation needs a dual approach. If a circuit is capable of doing one discipline correctly**,** it is not capable of performing the other task with high precision. Therefore, Axon decided to use a dual PLL topology in their latest ADA-524 4 channel audio D/A converter. The input stage is based on the above mentioned CS8414 together with a high bandwidth pulse transformer to incorporate a precise and reliable data recovery system. The second stage is a discrete PLL with custom made VCXOs. Two VCXOs are used per channel to decode the four most popular clock frequencies of 44.1 kHz and 88.2 kHz with the first VCXO and 48 kHz and 96 kHz with the second VCXO. 32 kHz will also work, but without jitter attenuation. A new highly improved phase comparator is used to perform a lock mechanism without the common “dead zone” found in most other phase comparators and PLL circuits. This also lowered the intrinsic jitter.

Intrinsic Jitter and Jitter attenuation

An essential characteristic of a high performance audio D/A converter is the intrinsic jitter of the device when a “jitter free” source is connected. The CS 8414 has an intrinsic jitter of approximately 150 ps RMS. To fully use the resolution of the 24 bit D/A converter chips in the ADA-524, the second PLL has an intrinsic jitter of 2 ps RMS. Together with a jitter attenuation frequency of 25 Hz and a jitter attenuation capability of over 60 dB, the ADA-524 can handle input signals with extreme jitter contamination without degradation of the total performance.

System performance degradation.

If we look at a test signal based on a normal AES/EBU data stream, but with the insertion of a normal 100-meter AES/EBU cable, the performance degradation of single PLL topologies becomes obvious.
In *figure 1* you see the eye pattern of an AES/EBU signal when it travels direct or through a 100-meter cable simulator.
In *figure 2* we look at the intrinsic jitter of both the first and the second PLL of the ADA-524.
Figure 3 displays the use of the 100-meter cable simulator and the degradation of the clock jitter performance induced by the frequency limitation of the cable's low-pass function. The increase in jitter is obvious and also the jitter attenuation characteristic of the second PLL. This second PLL starts attenuating the jitter at 25 Hz and rapidly lowers the jitter to insignificant values. The single bin residual jitter values are as low as 50 femto seconds (= 0.05 ps).

This is all nice, but what happens to the actual analog signal and how much degradation is caused by this added interface induced jitter?
In *figure 4* the THD+N function is plotted against frequency. Here the actual system degradation is obvious when no second PLL is used. It shows how effectively the dual PLL topology handles the severe input signal degradation that causes the THD+N plot to stick at -75dB. This is not only harmonic distortion but mainly noise. The increased noise floor lowers the effective resolution of the converter. The lower two traces are, in fact, identical and the system resolution is restored.
This plot also shows that there is a slight improvement over the intrinsic jitter when only the AP system 2 digital output is used. The improvement in intrinsic jitter from 150 ps to 2 ps has a measurable effect on this THD+N plot.
An FFT of an 11kHz signal with and without the cable simulator is shown in *figure 5*. You can actual see the rise in noise floor in this view. To show this more clearly I have used an 11 kHz sinewave to place the harmonic influence outside the scope of this figure.

System performance.

To further show the system performance of the Axon ADA-524, the linearity plot is shown in *figure 6*. This plot shows the deviation of the D/A converter chip used compared with a perfect one (which is a perfect straight horizontal line). The 3 dB error is at –132 dB which resembles 22 bit performance. In *figure 7* you can see the linearity of the unit when it is fed with 16 to 24 bit input word-length data.
The ADA-524 is a D/A converter capable of converting 96kHz digital audio. To show the frequency response of this unit I used a 96k capable A/D converter and measured within the analog to analog domain. (the AP system 2 was not capable of generating 96k digital stimuli at the time of this test) The outcome is plot in *figure 8*.
Optimized PCB lay-out is responsible for the very low cross-talk in this high density four channel design. See *figure 9*.
An 8 tone stress signal is used to define IMD artifacts. This signal produces several intermodulation products at multiple frequencies of 100 Hz. The outcome is shown in *figure 10*.

Conclusion.

Specifying an audio D/A converter with static signals with a measuring system like the Audio Precision system 2 is only useful when the used signal paths are short and the digital sources have very low intrinsic jitter (which is often not the case). Using 75 coaxial interconnections will degrade system performance less than a twisted pair does. When conversion to analog is necessary, an input stage with dual PLL topology (not any, but a high quality one) is capable of lowering the system degradation to insignificant values.

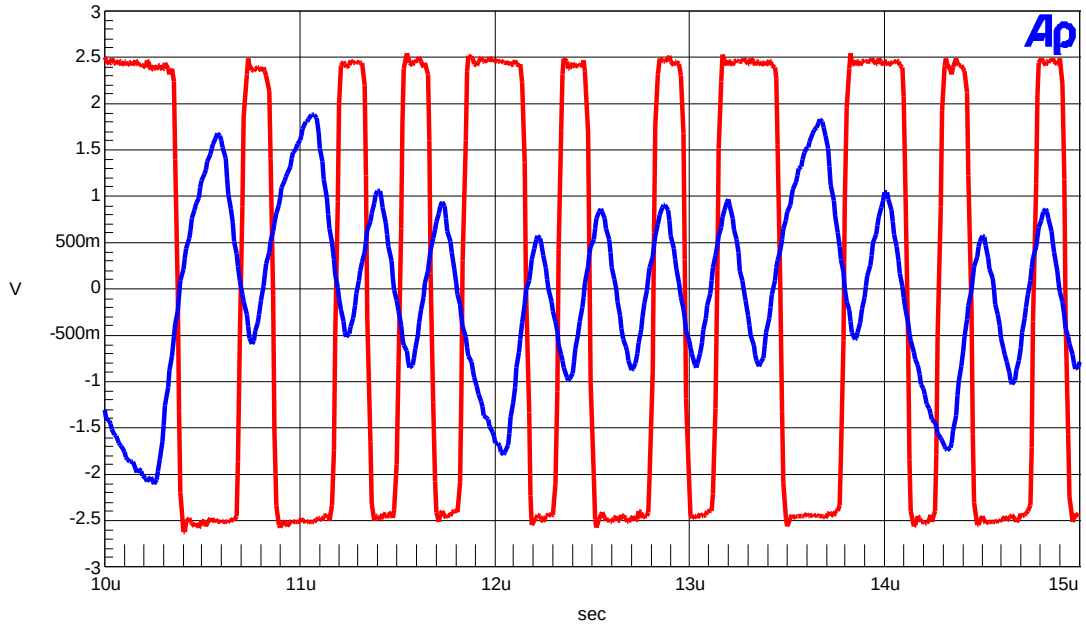

Figure 1:
AES/EBU signal before and after 100-meter twisted-pair

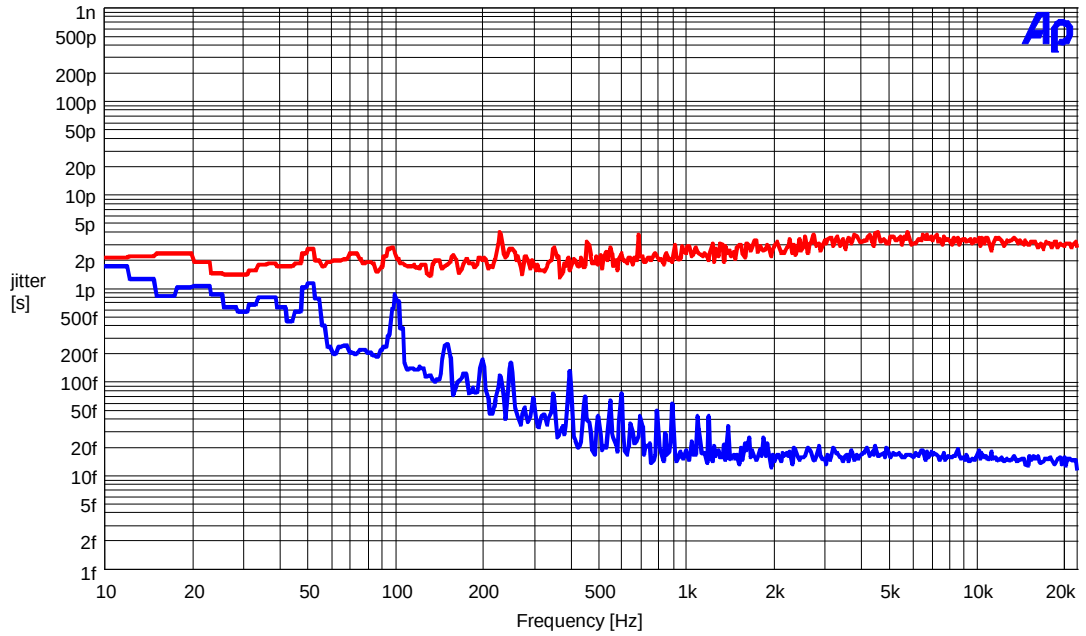

Figure 2:
Intrinsic jitter of ADA-524 top trace (red) first PLL bottom trace (blue) second PLL
The RMS values calculate to 150 ps and 2 ps respectively

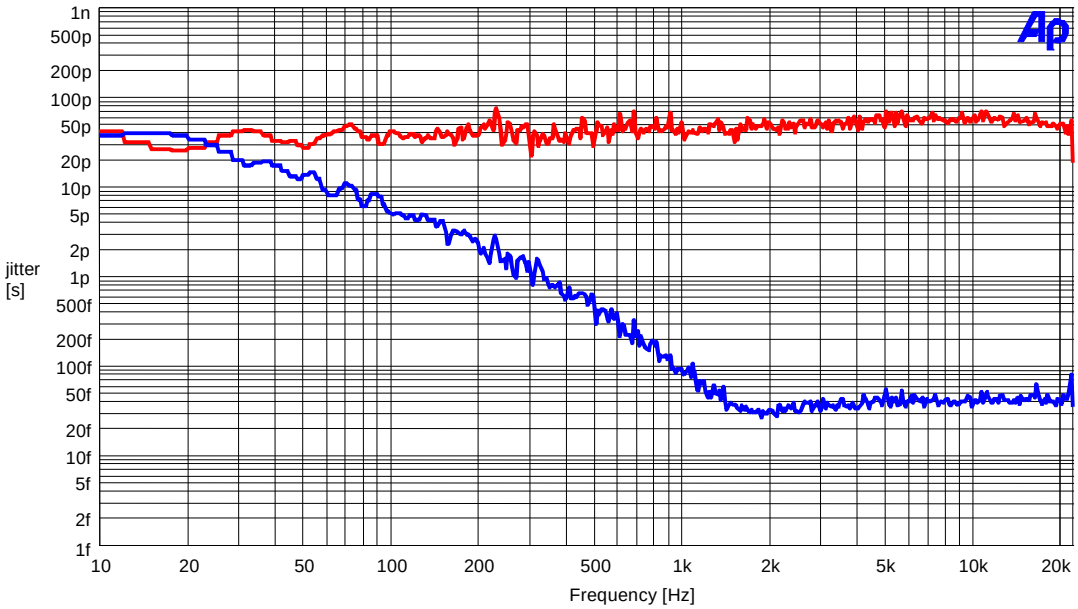

Figure 3:
jitter of ADA-524 top trace (red) first PLL bottom trace (blue) second PLL with use of a 100-meter cable simulator. The RMS values calculate to 2.7 ns and 35 ps respectively

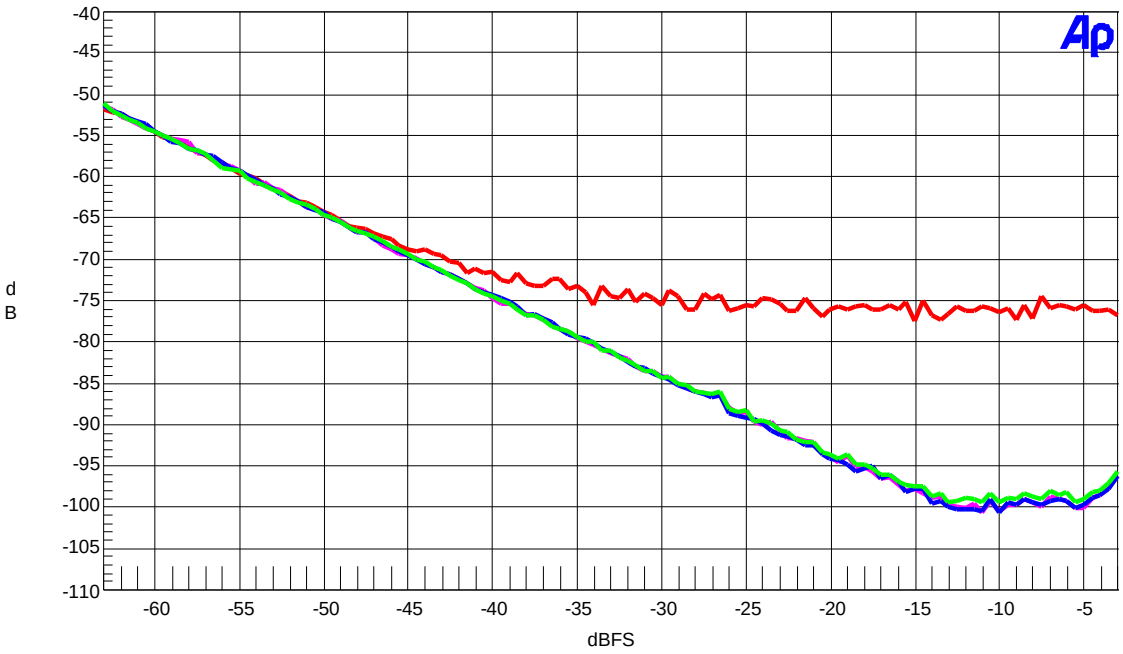

Figure 4:
THD+N versus frequency, from top to bottom (stimuli is sine-wave of 7kHz)

1. Top trace (red) is with 100-meter cable-simulator and only one PLL (CS8414)
2. Second trace (green) is one PLL with no cable-simulator
3. Third trace (blue) is dual PLL with cable simulator
4. Fourth trace (magenta) is dual PLL without cable simulator

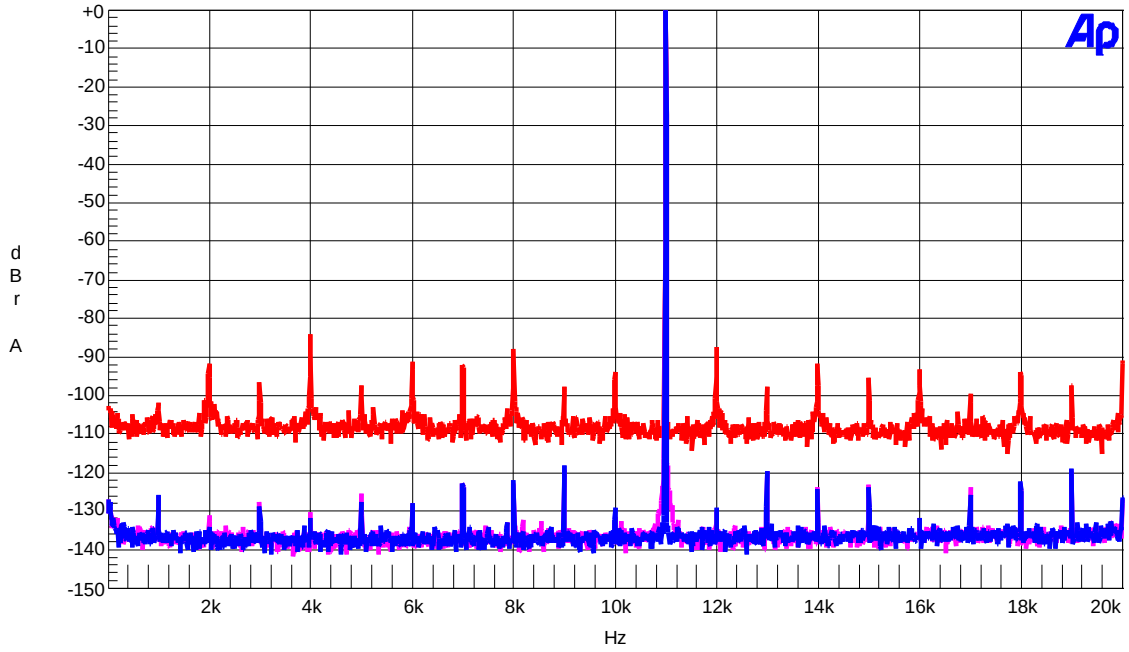

Figure 5:
THD+N versus frequency, from top to bottom (stimuli is sine-wave of 11kHz)

1. Top trace (red) is with 100-meter cable-simulator and only one PLL (CS8414)
2. Second trace (magenta) is one PLL with no cable-simulator
3. Third trace (blue) is dual PLL with cable simulator

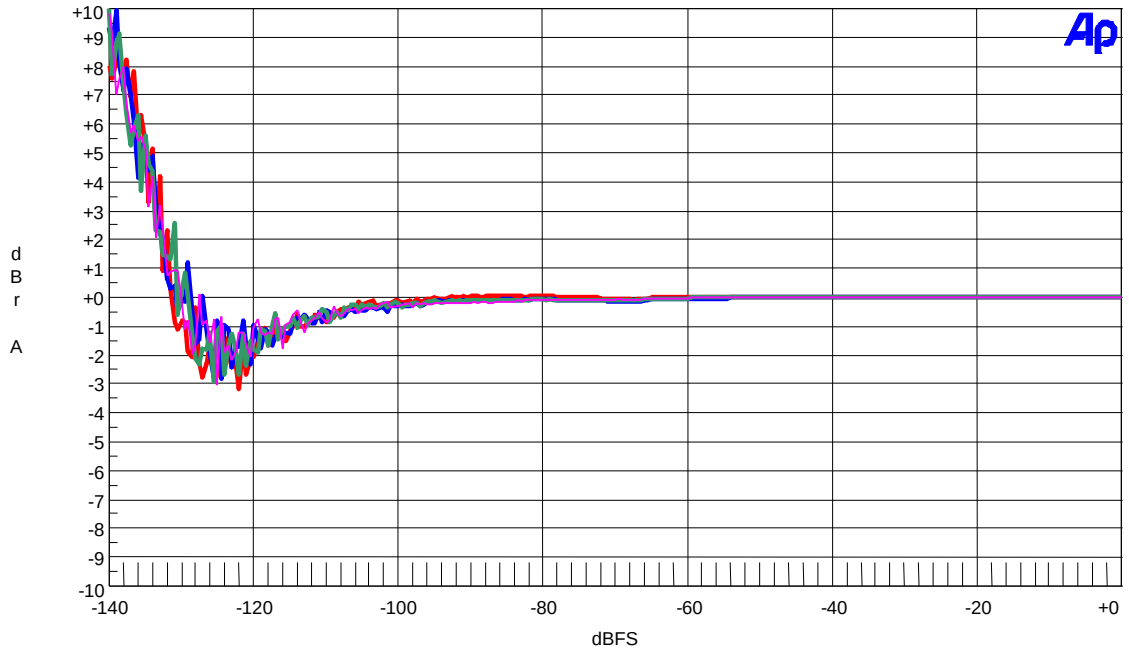

Figure 6:
Linearity plot (fade to noise)

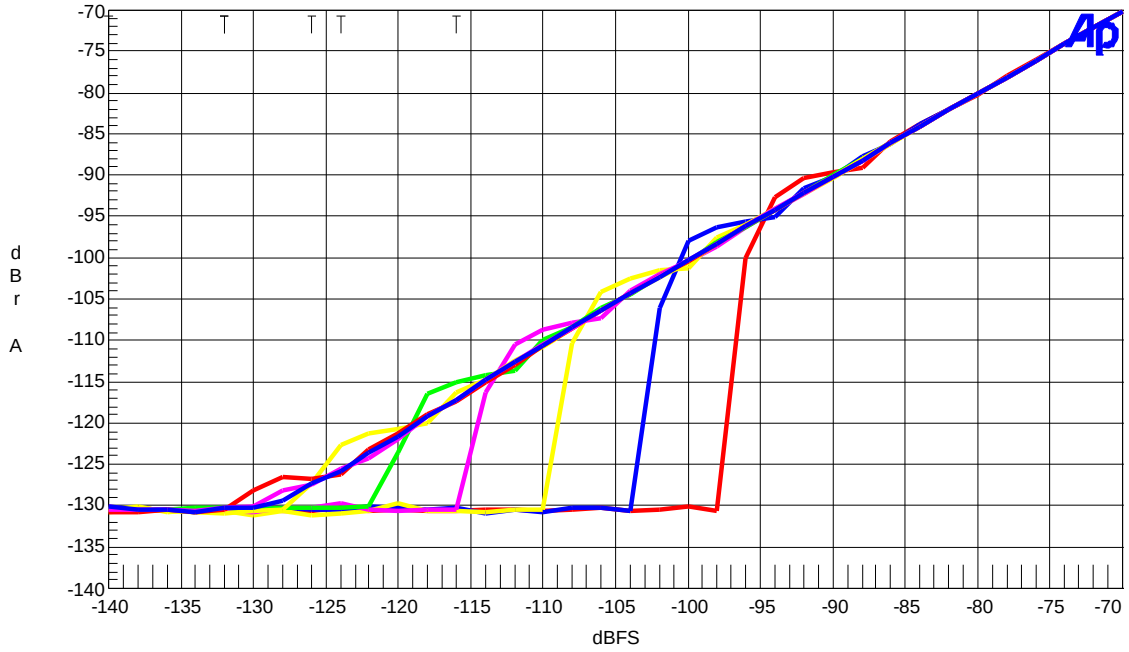

Figure 7:
Linearity plot, from right to left 16, 17, 18, 19, 20, 21, 22, 23, and 24 bit input word-length.

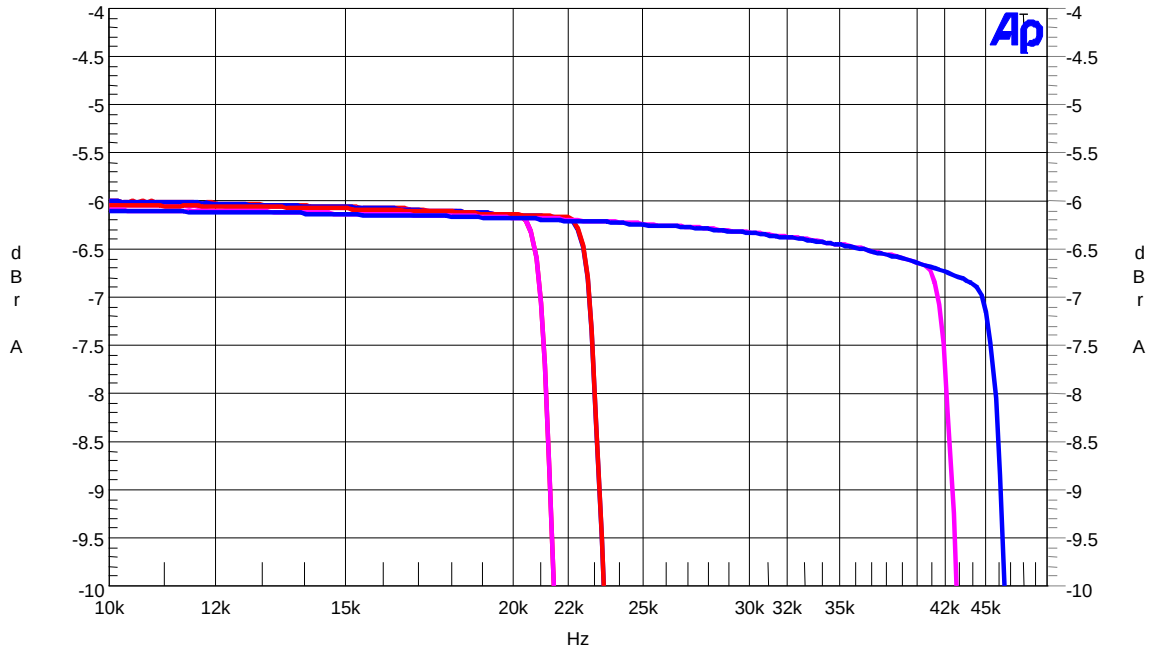

Figure 8:
Frequency response of a –6dB sinewave with 44.1, 48, 88.2, and 96k sampling frequency

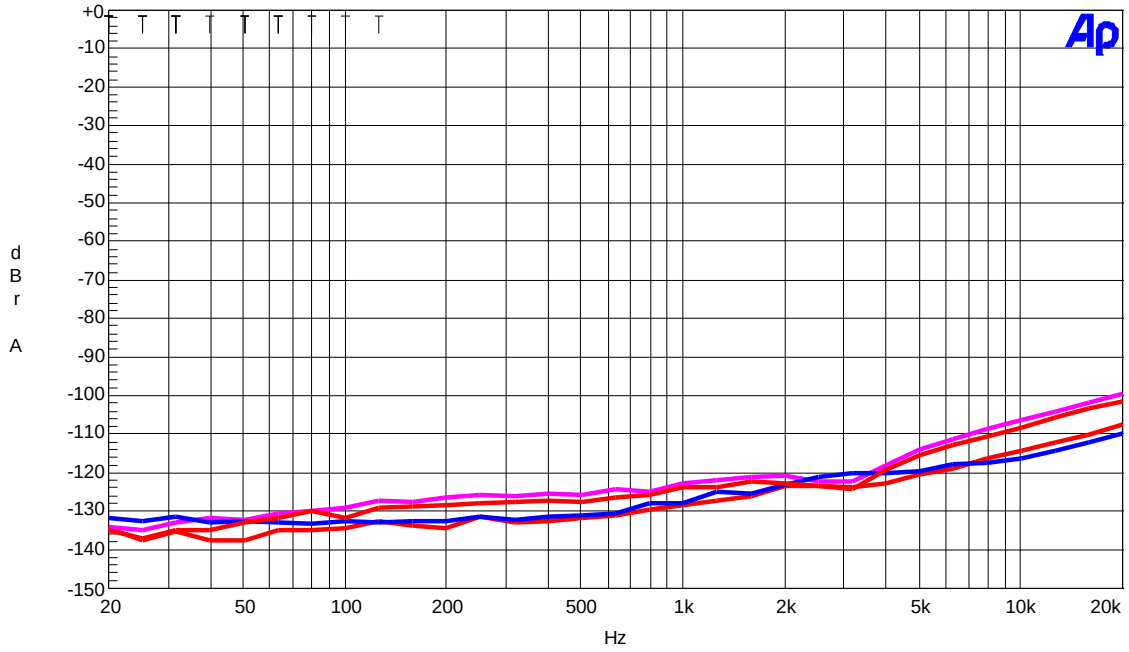

Figure 9:
Cross-talk

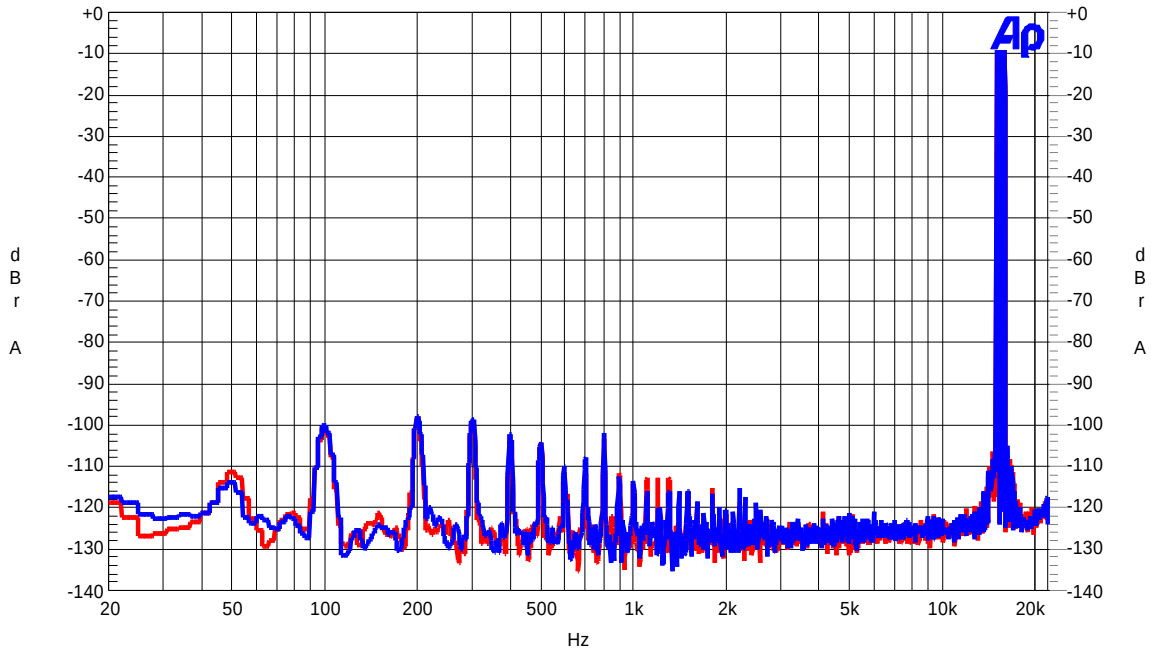

Figure 10:
IMD products with a stimuli multi tone of 15, 15.2, 15.3, 15,5, 15.6, 15.7, 15.8 and 16 kHz